LM516x、0.65A/0.3A、120V (絶対最大値)、降圧コンバータ、Fly-Buck™ コンバータ機能付き

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 高信頼性の堅牢なアプリケーション用に設計
  - 広い入力電圧範囲:6V～120V (絶対最大値)
  - 接合部温度範囲:-40℃～+150℃
  - 固定 3ms の内部ソフトスタート タイマ
  - ピークおよびバレー電流制限保護
  - 入力 UVLO およびサーマル シャットダウン保護機能
- スケーラブルな産業用電源およびバッテリ パック用に設計
  - 最小オンおよびオフ時間:50ns
  - 最大 1MHz まで可変のスイッチング周波数
  - ダイオード エミュレーションにより軽負荷時の効率を向上
  - 低静止電流 (10µA 未満) の自動モード
  - Fly-Buck コンバータ機能のための FPWM
  - シャットダウン時静止電流:3µA
  - LM5164-Q1、LM5163-Q1、LM5013-Q1 とピン互換
  - LM5017 および LM34927 と類似のピン配置と機能。
- 統合により設計のサイズとコストを低減
  - COT モード制御アーキテクチャ
  - 1.9Ω の NFET 降圧スイッチを内蔵
  - 0.71Ω の NFET 同期整流器を内蔵
  - 1.2V の内部基準電圧
  - ループ補償部品が不要
  - V_{CC} バイアス レギュレータとブート ダイオードを内蔵
  - オープンドレインのパワー グッド インジケータ
  - パッケージ オプション:SOIC PowerPAD™-8 IC パッケージまたは WSON-8 パッケージ

2 アプリケーション

- 通信–ブリック パワー モジュール
- 産業用バッテリ パック (≧ 10 個の直列)
- バッテリ パック:電動自転車、電動スクーター、軽電気自動車 (LEV)

3 概要

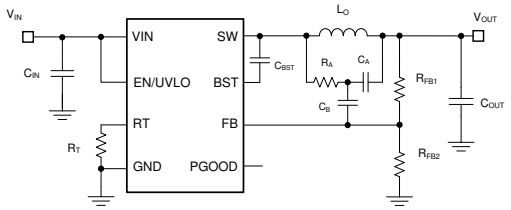
LM5169 および LM5168 同期整流降圧コンバータは、最小限の外部サージ抑制部品で、広い入力電圧範囲のレギュレーションを行えるよう設計されています。制御可能な最短のオン時間は 50ns で、大きな降圧率を使用できるため、48V 公称入力から低電圧レールへの直接降圧変換が可能になり、システムの複雑性と設計のコストを下げることができます。LM516x は最低 6V の入力電圧ディップ時でも、必要に応じて 100% に近いデューティ サイクルで動作するため、幅広い入力電源電圧範囲の産業用および多セルのバッテリ パック機器に理想的です。

ハイサイドおよびローサイドのパワー MOSFET を内蔵しているため、LM5169 は最大 0.65A、LM5168 は最大 0.3A の出力電流を供給します。コンスタント オン時間 (COT) 制御アーキテクチャにより、スイッチング周波数はほぼ一定で、負荷およびライン過渡応答が非常に優れています。LM516x は、FPWM または自動モード バージョンが利用できます。FPWM モードにより、負荷範囲の全体にわたって強制連続導通モード (CCM) で動作し、絶縁型 Fly-Buck コンバータ アプリケーションをサポートします。自動モードにより、非常に低い I_Q とダイオード エミュレーション モード動作が可能になり、軽負荷時に高効率です。

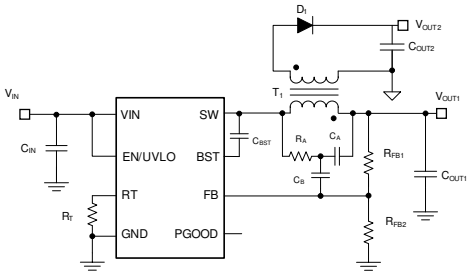
製品情報

部品番号 (3)	パッケージ (1)	パッケージ サイズ(2)
LM5169	DDA (HSOIC、8)	4.9mm × 6mm
	NGU (WSON、8)	4.00mm × 4.00mm
LM5168	DDA (HSOIC、8)	4.9mm × 6mm
	NGU (WSON、8)	4.00mm × 4.00mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) デバイス比較表を参照してください。



代表的な降圧アプリケーション回路



代表的な Fly-Buck™ コンバータ アプリケーション回路

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4 Device Comparison Table

DEVICE NUMBER	PACKAGE	DESCRIPTION	OUTPUT CURRENT	LIGHT LOAD MODE	CURRENT LIMIT
LM5168PDDAR	DDA (HSOIC, 8)	0.3 A, buck, AUTO, no-hiccup	0.3 A	PFM	0.42 A, no-hiccup
LM5168FDDAR		0.3 A, buck, FPWM, hiccup		FPWM	0.42 A, hiccup
LM5169PDDAR		0.65 A, buck, AUTO, hiccup	0.65 A	PFM	0.84 A, hiccup
LM5169FDDAR		0.65 A, buck, FPWM, hiccup		FPWM	0.84 A, hiccup
LM5168PNGUR	NGU (WSON, 8)	0.3 A, buck, AUTO, no-hiccup	0.3 A	PFM	0.42 A, no-hiccup
LM5168FNGUR		0.3 A, buck, FPWM, hiccup		FPWM	0.42 A, hiccup
LM5169PNGUR		0.65 A, buck, AUTO, hiccup	0.65 A	PFM	0.84 A, hiccup
LM5169FNGUR		0.65 A, buck, FPWM, hiccup		FPWM	0.84 A, hiccup

5 Pin Configuration and Functions

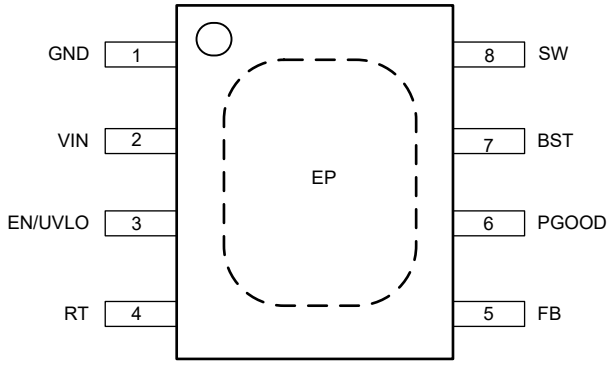


図 5-1. 8-Pin SO PowerPAD™ Integrated Circuit Package (Top View)

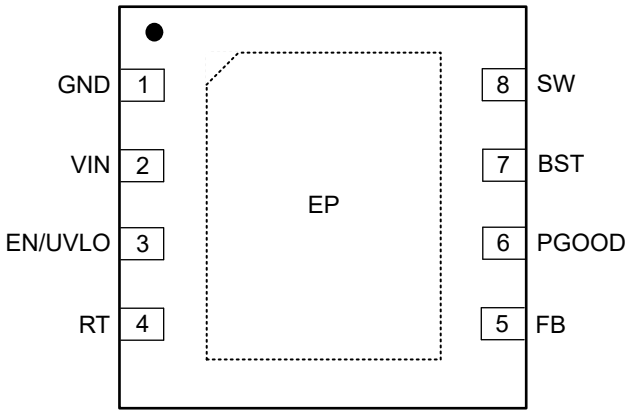


図 5-2. 8-Pin WSON NGU Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	GND	G	Ground connection for internal circuits
2	VIN	P/I	Regulator supply input pin to the high-side power MOSFET and internal bias regulator. Connect directly to the input supply of the buck converter with short, low impedance paths.
3	EN/UVLO	I	Precision enable and undervoltage lockout (UVLO) programming pin. If the EN/UVLO rising voltage is below 1.1 V, the converter is in shutdown mode with all functions disabled. If the UVLO voltage is greater than 1.1 V and below 1.5 V, the converter is in standby mode with the internal VCC regulator operational and no switching. If the EN/UVLO voltage is above 1.5 V, the start-up sequence begins.
4	RT	I	On-time programming pin. A resistor between this pin and GND sets the buck switch on time.
5	FB	I	Feedback input of voltage regulation comparator
6	PGOOD	O	Power-good indicator. This pin is an open-drain output pin. Connect to a source voltage through an external pullup resistor between 10 kΩ to 100 kΩ. Connect to GND if the PGOOD feature is not needed.
7	BST	P/I	Bootstrap gate-drive supply. Required to connect a high-quality 2.2-nF X7R ceramic capacitor between BST and SW to bias the internal high-side gate driver.
8	SW	P	Switching node that is internally connected to the source of the high-side NMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Connect to the switching node of the power inductor.
—	EP	—	Exposed pad of the package. No internal electrical connection. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	120	V
	SW	–1.5	120	
	SW, transient < 20 ns	–3		
	BST	–0.3	125.5	
	BST – SW	–0.3	5.5	
	EN	–0.3	120	
	FB	–0.3	5.5	
	RT	–0.3	5.5	
	PGOOD	–0.3	14	
Bootstrap Capacitor(3)	External BST to SW capacitance		2.5	nF
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See the Applications section for PCB layout recommendations (*Layout Guidelines*).
(3) Specification applies to FPWM and Fly-Buck operation.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Pin voltage	VIN	6		115	V
V_{EN}	Pin voltage	EN			115	V
I_{OUT}	Output current range	LM5169		0.65		A
		LM5168		0.3		A
C_{BST}	External BST to SW capacitance	FPWM Mode		2.2		nF
F_{SW}	Switching frequency		100		1000	kHz

6.4 Thermal Information

THERMAL METRIC[1]		LM516x DDA (SOIC) 8 PINS	LM516x NGU (WSON) 8 PINS	UNIT
$R_{\theta JA(EVM)}$	Junction-to-ambient thermal resistance for EVM[2]	22	15.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	41.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.1	16.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.1	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*
(2) This value is obtained on the LM5168PEVM and LM5169PEVM with approximately 49 cm^2 of copper area. See Thermal considerations section for more information.

6.5 Electrical Characteristics

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 24 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	V_{EN} = 2.5 V, PWM Operation		420	880	µA
		V_{EN} = 2.5 V, PFM Operation		10	25	µA
$I_{Q(STANDBY)}$	VIN standby current - LDO only	V_{EN} = 1.25 V		17	35	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0 V, Tj=25°C		3	6	µA
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.45	1.5	1.55	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	1.35	1.4	1.44	V
$V_{SD(R)}$	EN standby rising threshold	EN rising, enable internal LDO, no switching.			1.1	V
$V_{SD(F)}$	EN standby falling threshold	EN falling, disable internal LDO.	0.45			V
REFERENCE VOLTAGE						
V_{FB}	FB voltage	V_{FB} falling	1.181	1.2	1.218	V
STARTUP						
t_{SS}	Internal fixed soft-start time		1.75	3	4.75	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	I_{SW} = –100 mA		1.91		Ω
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	I_{SW} = 100 mA		0.74		Ω
$t_{ON(min)}$	Minimum ON pulse width			50		ns
$t_{ON(1)}$	On-time1	V_{VIN} = 6 V, R_{RT} = 75 kΩ		5000		ns
$t_{ON(2)}$	On-time2	V_{VIN} = 6 V, R_{RT} = 25 kΩ		1650		ns
$t_{ON(3)}$	On-time3	V_{VIN} = 12 V, R_{RT} = 75 kΩ		2550		ns
$t_{ON(4)}$	On-time4	V_{VIN} = 12 V, R_{RT} = 25 kΩ		830		ns
$t_{OFF(min)}$	Minimum OFF pulse width			50		ns
BOOT CIRCUIT						
$V_{BOOT-SW(UV\_R)}$	BOOT-SW UVLO rising threshold	$V_{BOOT-SW}$ rising		2.6	3.4	V
OVERCURRENT PROTECTION						
$I_{HS\_PK(OC)}$	High-side peak current limit	LM5168	0.356	0.42	0.484	A
		LM5169	0.71	0.84	0.94	A
$I_{LS\_PK(OC)}$	Low-side peak current limit	LM5168	0.356	0.42	0.484	A
		LM5169	0.71	0.84	0.94	A
$I_{DELTA(OC)}$	Min of $I_{HS\_PK(OC)}$ or $I_{LS\_PK(OC)}$ minus $I_{LS\_V(OC)}$	LM5168		0.084		A
		LM5169		0.168		A

6.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 24 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LS(NOC)}$	Low-side negative current limit	LM5169	1.05	1.5	1.90	A
		LM5168	0.4	0.75	1.1	A
$I_{LS\_V(OC)}$	Low-side valley current limit	LM5169 Low-side valley current limit on LS FET	0.569	0.672	0.775	A
		LM5168 Low-side valley current limit on LS FET	0.27	0.336	0.42	A
I_{ZC}	Zero-cross detection current threshold			0		A
T_W	Hiccup time before re-start			64		ms
POWER GOOD						
V_{PGTH}	Power Good threshold	FB falling, PG high to low	1.055	1.08	1.1	V
		FB rising, PG low to high	1.105	1.14	1.175	V
R_{PG}	Power Good threshold	VFB = 1 V		7		Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (1)	Temperature rising		175		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			10		°C

(1) Specified by design, not product tested

6.6 Typical Characteristics

Unless otherwise specified the following conditions apply: At T_A = 25°C, V_{IN} = 24 V

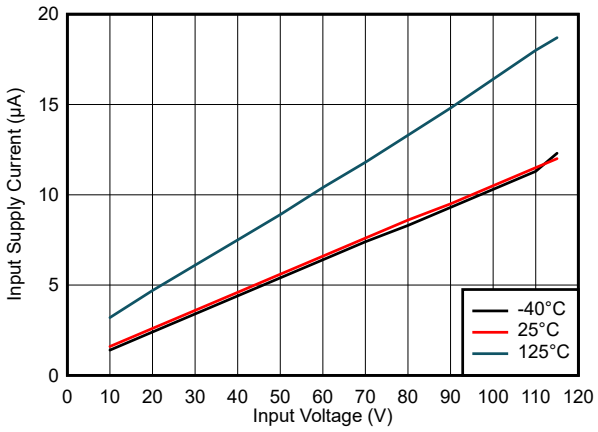


図 6-1. Shutdown Supply Current Versus Input Voltage

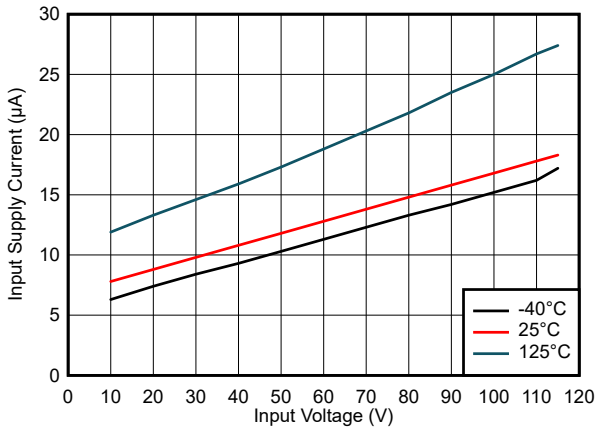


図 6-2. Sleep Mode Supply Current Versus Input Voltage (DEM, non-switching)

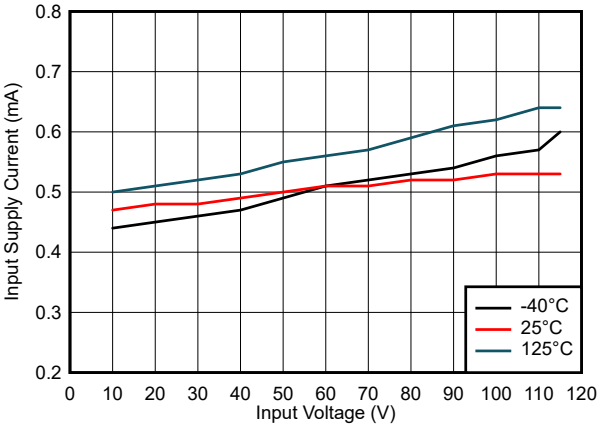


図 6-3. Active Mode Supply Current Versus Input Voltage (FPWM, non-switching)

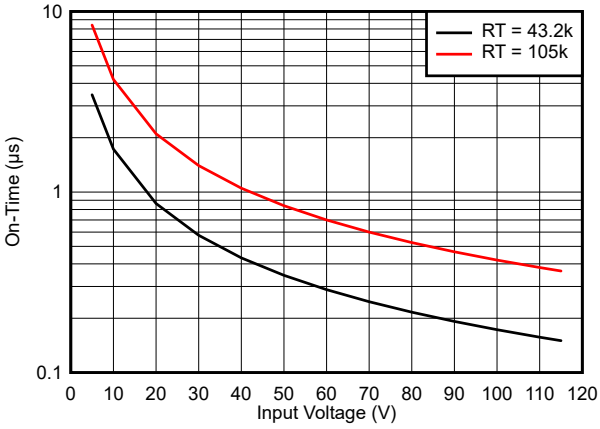


図 6-4. COT On Time Versus Input Voltage

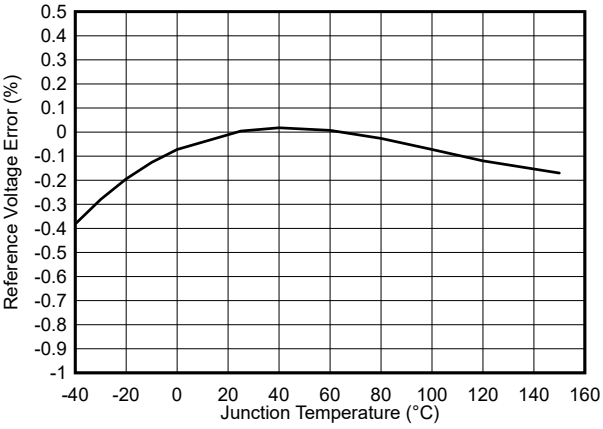


図 6-5. Feedback Comparator Threshold Versus Temperature

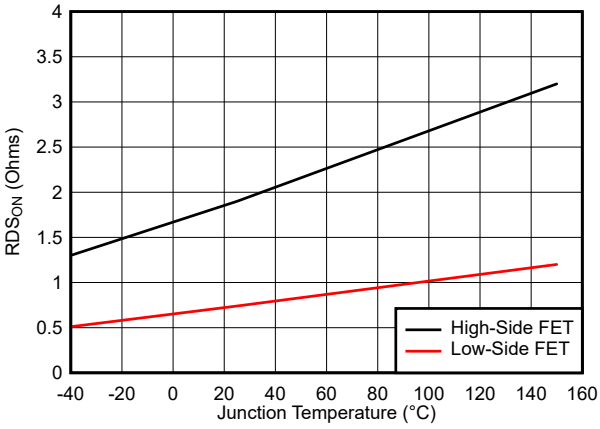


図 6-6. MOSFETs On-State Resistance Versus Temperature

7 Detailed Description

7.1 Overview

The LM5169 and LM5168 are easy-to-use, ultra-low I_Q constant on-time (COT) synchronous step-down buck regulators. With integrated high-side and low-side power MOSFETs, the LM516x is a low-cost, highly efficient, buck converter that operates from a wide input voltage of 6 V to 120 V absolute maximum, delivering up to 0.65-A or 0.3-A DC load current. The LM516x is available in an 8-pin SO PowerPAD integrated circuit package with 1.27-mm pin pitch for adequate spacing in high-voltage applications. There is also a smaller 8-pin WSON package option available to help achieve a compact design. This constant on-time (COT) converter is an excellent choice for low-noise, high-current, and fast load transient requirements, operating with a predictive on-time switching pulse. Over the input voltage range, input voltage feed-forward is employed to achieve a quasi-fixed switching frequency. A controllable on time as low as 50 ns permits high step-down ratios and a minimum forced off time of 50 ns provides extremely high duty cycles. This feature enables fixed frequency operation as VIN drops close to VOUT. After the forced off time of 50 ns is reached, the device enters frequency fold-back operation to maintain a constant output voltage. The LM516x implements a smart peak and valley current limit detection circuit to make sure of robust protection during output short circuit conditions. Control loop compensation is not required for this regulator, reducing design time and external component count.

The LM5169 and LM5168 are pre-programmed to operate in auto mode or FPWM mode. When configured to operate in auto mode, at light loads, the device transitions into an ultra-low I_Q mode to maintain high efficiency and prevent draining battery cells connected to the input when the system is in standby. When configured in FPWM mode, at light loads, the device maintains CCM operation, enabling Fly-Buck converter operation. The Fly-Buck converter configuration can be used to generate both a non-isolated primary output and an isolated secondary output.

The LM5169 and LM5168 incorporates additional features for comprehensive system requirements, including an open-drain power-good circuit for the following:

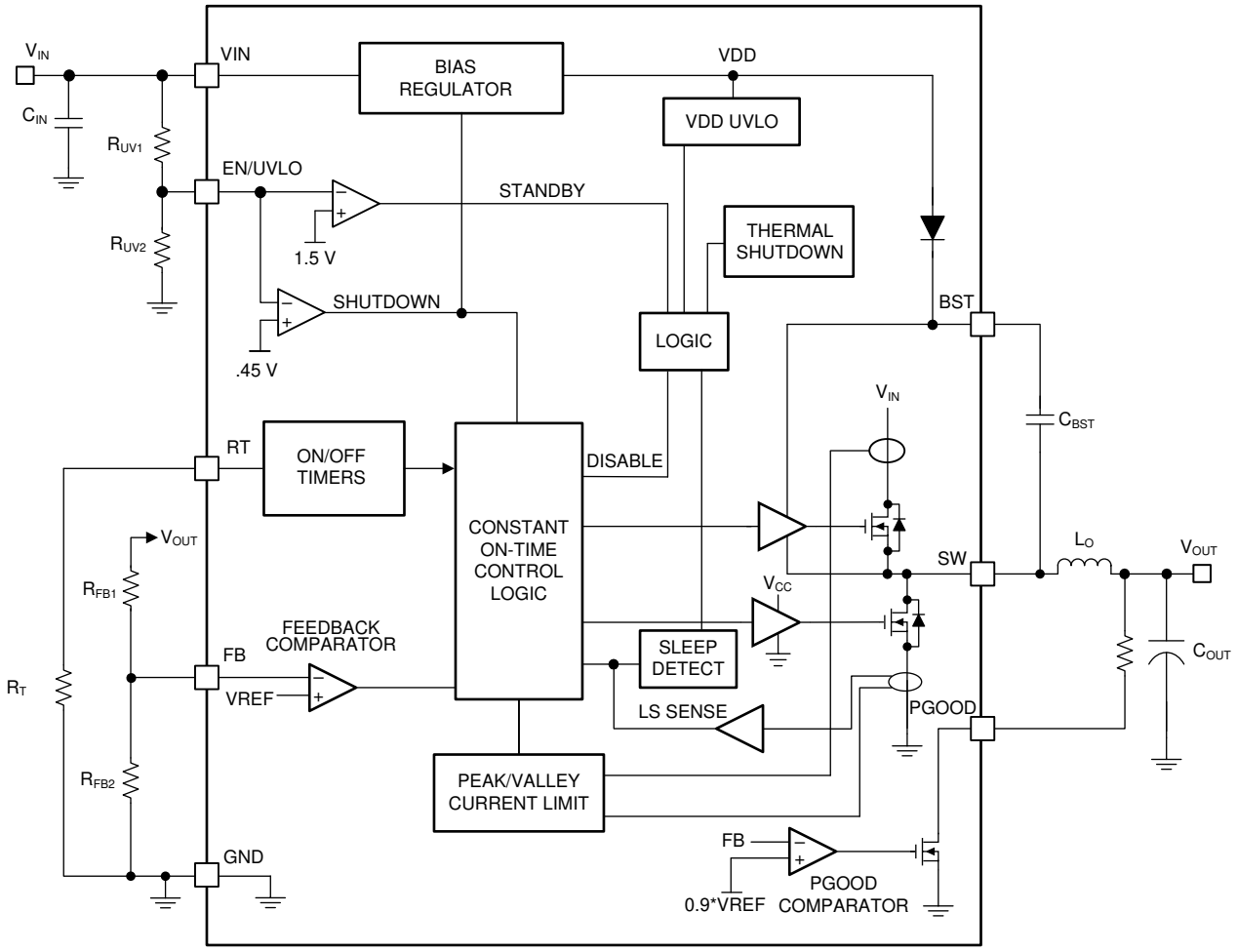
- Power-rail sequencing and fault reporting
- Internally fixed soft start
- Monotonic start-up into prebiased loads
- Precision enable for programmable line undervoltage lockout (UVLO)
- Smart cycle-by-cycle current limit for optimal inductor sizing
- Thermal shutdown with automatic recovery

The LM5169 and LM5168 support a wide range of end equipment requiring a regulated output from a high input supply where the transient voltage deviates from the DC level. Examples of such end equipment systems are the following:

- 48-V automotive systems
- High cell-count battery-pack systems
- 24-V industrial systems
- 48-V telecom and PoE voltage ranges

The pin arrangement is designed for a simple layout that requires only a few external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Architecture

The LM516x step-down switching converter employs a constant on-time (COT) control scheme. The COT control scheme sets a fixed on time, t_{ON}, of the high-side FET using a timing resistor (R_T). t_{ON} is adjusted as V_{IN} changes and is inversely proportional to the input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). After expiration of t_{ON}, the high-side FET remains off until the feedback pin is equal or below the reference voltage of 1.2 V. To maintain stability, the feedback comparator requires a minimal ripple voltage that is in-phase with the inductor current during the off time. Furthermore, this change in feedback voltage during the off time must be large enough to dominate any noise present at the feedback node. The minimum recommended ripple voltage is 20 mV. In some cases more ripple voltage can be needed for robust operation. This is especially true when there is excessive coupling from the SW pin or the BST pin to the FB pin. The Type 1 ripple generation method is more susceptible to noise injection than the other methods. See 表 7-1 for different types of ripple injection schemes that make sure of stability over the full input voltage range.

During a rapid start-up or a positive load step, the regulator operates with minimum off times until regulation is achieved. This feature enables extremely fast load transient response with minimum output voltage undershoot. When regulating the output in steady-state operation, the off time automatically adjusts to produce the SW pin duty cycle required for output voltage regulation to maintain a fixed switching frequency. In CCM, the switching frequency F_{SW} is programmed by the R_T resistor.

表 7-1. Ripple Generation Methods

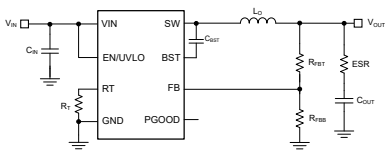
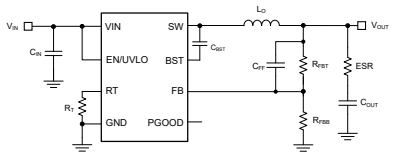
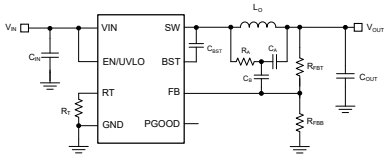
TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
		
$R_{ESR} \geq \frac{20\ mV \cdot V_{OUT}}{V_{FB} \cdot \Delta I_L}$ $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$	$R_{ESR} \geq \frac{20\ mV}{\Delta I_L}$ $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ $C_{FF} \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FBB} \| R_{FBT})}$	$C_A \geq \frac{10}{F_{SW} \cdot (R_{FBB} \| R_{FBT})}$ $\|R_A \cdot C_A \leq \frac{(V_{IN} - V_{OUT}) \cdot T_{ON}}{20\ mV}$ $C_B \geq \frac{T_{settle}}{3 \cdot R_{FBT}}$

表 7-1 presents three different methods for generating appropriate voltage ripple at the feedback node. The Type-1 ripple generation method uses a single resistor, R_{ESR}, in series with the output capacitor. The generated voltage ripple has two components: capacitive ripple caused by the inductor ripple current charging and discharging the output capacitor and resistive ripple caused by the inductor ripple current flowing into the output capacitor and through series resistance R_{ESR}. The capacitive ripple component is out-of-phase with the inductor current and does not decrease monotonically during the off time. The resistive ripple component is in-phase with the inductor current and decreases monotonically during the off time. The resistive ripple must exceed the capacitive ripple at V_{OUT} for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off time. The equations under Type 1 define the value of the series resistance R_{ESR} to make sure of sufficient in-phase ripple at the feedback node.

Type 2 ripple generation uses a C_{FF} capacitor in addition to the series resistor. As the output voltage ripple is directly AC-coupled by C_{FF} to the feedback node, the R_{ESR} and ultimately the output voltage ripple, are reduced by a factor of V_{OUT} / V_{FB}.

Type 3 ripple generation uses an RC network consisting of R_A and C_A, and the switch node voltage to generate a triangular ramp that is in-phase with the inductor current. This triangular wave is then AC-coupled into the feedback node with capacitor C_B. Because this circuit does not use output voltage ripple, this circuit isan excellent choice for applications where low output voltage ripple is critical. See the *Related Documentation* section for more details about COT control methods.

Light load mode operation can be set to PFM and DEM operation or FPWM operation as a factory option. Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains the highest efficiency at light load currents by decreasing the effective switching frequency. DEM operation occurs when the synchronous power MOSFET switches off as inductor valley current reaches zero. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and prevents negative current conduction reduces conduction loss. Power conversion efficiency is higher in a DEM converter than an equivalent forced-PWM CCM converter. With DEM operation, the duration that both power MOSFETs remain off progressively increases as load current decreases. When this idle duration exceeds 15 µs, the converter transitions into an ultra-low I_Q mode, consuming only 10-µA quiescent current from the input. In FPWM operation, the DEM feature is turned off. This means that the device remains in CCM under light loads, and the device is capable of operating in a Fly-Buck converter configuration.

7.3.2 Internal VCC Regulator and Bootstrap Capacitor

The LM516x contains an internal linear regulator that is powered from VIN with a nominal output of 5 V, eliminating the need for an external capacitor to stabilize the linear regulator. The internal VCC regulator supplies current to internal circuit blocks, including the synchronous FET driver and logic circuits. The input pin (VIN) can be connected directly to line voltages up to 120 V absolute maximum. Because the power MOSFET

has a low total gate charge, use a low bootstrap capacitor value to reduce the stress on the internal regulator. Selecting a high-quality 2.2-nF X7R ceramic bootstrap capacitor as specified in the *Absolute Maximum Ratings* is required. Selecting a higher value capacitance stresses the internal VCC regulator and can damage the device. An internal diode connects from the VCC regulator to the BST pin to replenish the charge in the high-side gate drive bootstrap capacitor when the SW voltage is low.

7.3.3 Internal Soft Start

The LM516x employs an internal soft-start control ramp that allows the output voltage to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. The soft-start feature produces a controlled, monotonic output voltage start-up. The soft-start time is internally set to 3 ms.

7.3.4 On-Time Generator

The on time of the LM516x high-side FET is determined by the R_T resistor and is inversely proportional to the input voltage, V_{IN}. The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. Use 式 1 to calculate the on time, where R_T is in kΩ.

$$T_{ON} = \frac{R_T}{2.5 \cdot V_{IN}} \ [\mu s] \tag{1}$$

Use 式 2 to determine the R_T resistor to set a specific switching frequency in CCM, where F_{SW} is in kHz.

$$R_T = \frac{2500 \cdot V_{OUT}}{F_{SW}} \ [k\Omega] \tag{2}$$

Select R_T for a minimum on time (at maximum V_{IN}) greater than 50 ns for proper buck operation and greater than 100 ns for proper Fly-Buck converter operation. In addition to this minimum on time, the maximum frequency for this device is limited to 1 MHz.

7.3.5 Current Limit

The LM5168P manages overcurrent conditions with cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared every switching cycle to the current limit threshold (0.42 A typical). To protect the converter from potential current runaway conditions, the LM5168P includes a fold-back valley current limit feature, set at 0.34 A, that is enabled if a peak current limit is detected. As shown in 図 7-1, if the peak current in the high-side MOSFET exceeds 0.42 A for the LM5168P (typical), the present cycle is immediately terminated regardless of the programmed on time (t_{ON}), the high-side MOSFET is turned off and the fold-back valley current limit is activated. The low-side MOSFET remains on until the inductor current drops below this fold-back valley current limit, after which the next on-pulse is initiated. This method folds back the switching frequency to prevent overheating and limits the average output current to less than 0.3 A for LM5168P to make sure of proper short-circuit and heavy-load protection.

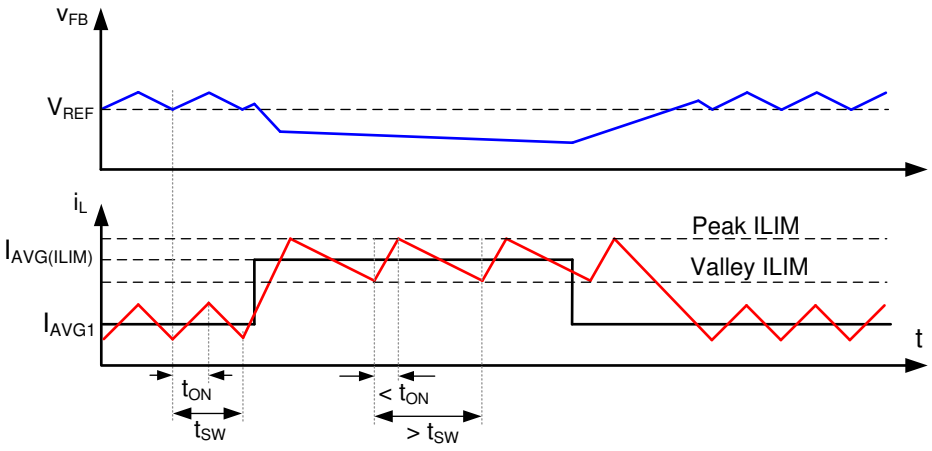


図 7-1. Current Limit Timing Diagram

Current is sensed after a leading-edge blanking time following the high-side MOSFET turn-on transition. The propagation delay of the current limit comparator is 100 ns. During high step-down conditions when the on time is less than 100 ns, a backup peak current limit comparator in the low-side FET also set at 0.84 A or 0.42 A, enables the foldback valley current limit set at 0.67 A or 0.34 A. This remarkable current limit scheme enables ultra-low duty-cycle operation, permitting large step-down voltage conversions while making sure of robust protection of the converter.

The LM5168F, LM5169F, and LM5169P implement a current limit off-timer and hiccup protection. If the current in the high-side MOSFET exceeds $I_{HS\_PK(OC)}$, the high-side MOSFET is immediately turned off and a non-resettable off-timer is initiated. The length of the off time is controlled by the feedback voltage and the input voltage. The off-timer make sure of safe short circuit operation in a Fly-Buck converter configuration. An overload current on the secondary output can result in the secondary voltage collapsing while the primary voltage remains in regulation. This action results in a possible condition where the secondary output voltage does not recover after the overload condition. Hiccup protection makes sure a soft-start counter enables both the secondary and primary output voltages to recover properly after an overcurrent event is detected for 16 consecutive current limit cycles. After four consecutive cycles without current limit detection, restart the hiccup protection counter. These devices attempt soft start after a "hiccup period" of 64 ms.

7.3.6 N-Channel Buck Switch and Driver

The LM516x integrates an N-channel buck switch and associated floating high-side gate driver. The gate-driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage bootstrap diode. A high-quality ceramic capacitor connected between the BST and SW pins provides the voltage to the high-side driver during the buck switch on time. See セクション 7.3.2 for limitations. During the off time, the SW pin is pulled down to approximately 0 V, and the bootstrap capacitor charges from the internal VCC through the internal bootstrap diode. The minimum off-timer, set to 50 ns (typical), makes sure of a minimum time each cycle to recharge the bootstrap capacitor. When the on time is less than 300 ns, the minimum off-timer is forced to 250 ns to make sure that the BST capacitor is charged in a single cycle. This is vital during wake-up from sleep mode when the BST capacitor is most likely discharged.

7.3.7 Synchronous Rectifier

The LM516x provides an internal low-side synchronous rectifier N-channel MOSFET. This MOSFET provides a low-resistance path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier operates in a diode emulation mode. Diode emulation enables the regulator to operate in a pulse-skipping mode during light load conditions. This mode leads to a reduction in the average switching frequency at light loads. Switching losses and FET gate driver losses, both of which are proportional to switching frequency, are significantly reduced at very light loads and efficiency is improved. This pulse-skipping mode also reduces the circulating inductor current and losses associated with conventional CCM at light loads.

7.3.8 Enable, Undervoltage Lockout (EN/UVLO)

The LM516x contains a dual-level EN/UVLO circuit. When the EN/UVLO voltage is below 0.45 V (typical), the converter is in a low-current shutdown mode and the input quiescent current (I_Q) is dropped down to 3 µA. When the voltage is greater than 1.1 V but less than 1.5 V (typical), the converter is in standby mode. In standby mode, the internal bias regulator is active while the control circuit is disabled. When the voltage exceeds the rising threshold of 1.5 V (typical), normal operation begins. Install a resistor divider from VIN to GND to set the minimum operating voltage of the regulator. If the user wishes to implement an input voltage UVLO, refer to 図 7-2, 式 3, and 式 4 for details. Typically, the user chooses a value for R_{UV1} and calculates the value of R_{UV2} using 式 3 based on a desired V_{ON}. Reasonable values for R_{UV1} are in the 1-MΩ range. 式 4 is then used to calculate the resulting V_{OFF}. V_{ON} and V_{OFF} are the input voltages where the device turns on and off, respectively.

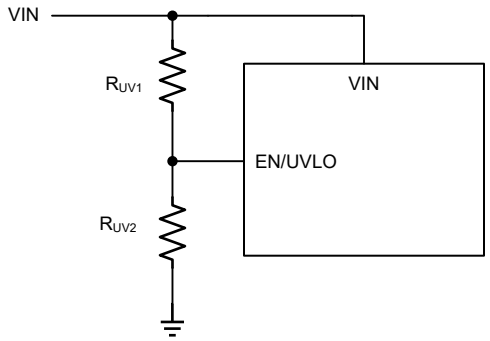


図 7-2. Input UVLO Connections

$$R_{UV2} = R_{UV1} \cdot \left(\frac{V_{EN(R)}}{V_{ON} - V_{EN(R)}} \right) \quad (3)$$

$$V_{OFF} = V_{EN(F)} \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}} \right) \quad (4)$$

If input UVLO is not required, the user can either drive EN/UVLO as an enable input driven by a logic signal or connect directly to VIN. If EN/UVLO is directly connected to VIN, the regulator begins switching as soon as the internal bias rails are active; about 4.5 V at VIN.

7.3.9 Power Good (PGOOD)

The LM516x provides a PGOOD flag pin to indicate when the output voltage is within the regulation level. Use the PGOOD signal for start-up sequencing of downstream converters or for fault protection and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 14 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail. When the FB voltage exceeds 95% of the internal reference V_{REF}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 90% of V_{REF}, an internal 7-Ω PGOOD switch turns on and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5 µs.

7.3.10 Thermal Protection

The LM516x includes an internal junction temperature monitor to protect the device in the event of higher than normal junction temperature. If the junction temperature exceeds 175°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The LM516x initiates a restart sequence when the junction temperature falls to 165°C, based on a typical thermal shutdown hysteresis of 10°C. This protection is a non-latching protection, so the device cycles into and out of thermal shutdown if the fault persists.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

EN/UVLO provides ON and OFF control for the LM516x. When $V_{EN/UVLO}$ is below approximately 0.45 V, the device is in shutdown mode. Both the internal linear regulator and the switching regulator are off. The quiescent current in shutdown mode drops to 3 µA at V_{IN} = 24 V. The LM516x also employs internal bias rail undervoltage protection. If the input voltage is below about 4.5 V, the regulator remains off.

7.4.2 Active Mode

The LM516x is in active mode when $V_{EN/UVLO}$ is above the precision enable threshold and the internal bias rail is above the UV threshold. In COT active mode, the LM516x is in one of the following modes depending on the load current:

1. CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
2. Auto mode (P device designator)– light load operation: Pulse skipping and diode emulation mode (DEM) when the load current is less than half of the peak-to-peak inductor current ripple in CCM operation.
3. FPWM mode (F device designator)– light load operation: Continuous conduction mode (CCM) throughout the entire load current range, including when the load current is lower than half of the inductor current ripple
4. Current limit CCM with peak and valley current limit protection when an over-current condition is applied at the output

7.4.3 Sleep Mode

Control Architecture gives a brief introduction to the LM516x diode emulation (DEM) feature. The converter enters DEM during light-load conditions when the inductor current decays to zero and the synchronous MOSFET is turned off to prevent negative current in the system. In the DEM state, the load current is lower than half of the peak-to-peak inductor current ripple and the switching frequency decreases when the load is further decreased as the device operates in a pulse skipping mode. A switching pulse is set when V_{FB} drops below 1.2 V.

As the frequency of operation decreases and V_{FB} remains above 1.2 V (V_{REF}) with the output capacitor sourcing the load current for greater than 15 µs, the converter enters an ultra-low I_Q sleep mode to prevent draining the input power supply. The input quiescent current (I_Q) required by the LM516x decreases to 10 µA in sleep mode, improving the light-load efficiency of the regulator. In this mode, all internal controller circuits are turned off to make sure of very low current consumption by the device. Such low I_Q renders the LM516x as the best option to extend operating lifetime for off-battery applications. The FB comparator and internal bias rail are active to detect when the FB voltage drops below the internal reference V_{REF} and the converter transitions out of sleep mode into active mode. There is a 9-µs wake-up delay from sleep to active states.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LM516x requires only a few external components to create a buck converter to step down from a wide range of supply voltages to a fixed output voltage. Several features are integrated in the device to meet system design requirements, including the following:

- Precision enable
- Input voltage UVLO
- Internal soft start
- Programmable switching frequency
- A PGOOD indicator

To expedite and streamline the process of designing a LM516x-based converter, a comprehensive LM516x quick-start calculator tool is available for download to assist the designer with component selection for a given application. This tool is complemented by the availability of an evaluation module and PSPICE models.

8.2 Typical Fly-Buck™ Converter Application

The LM516xF is designed for Fly-Buck converter applications by operating in FPWM mode. 図 8-1 shows the schematic for a 10-V output Fly-Buck regulator with a 10-V auxiliary output, capable of delivering 300 mA from each output, used as an example application for the LM5169F. Note that the secondary output ground can be floating with respect to the input supply ground. See 表 8-1 for a description of Fly-Buck converter terminology used in this example.

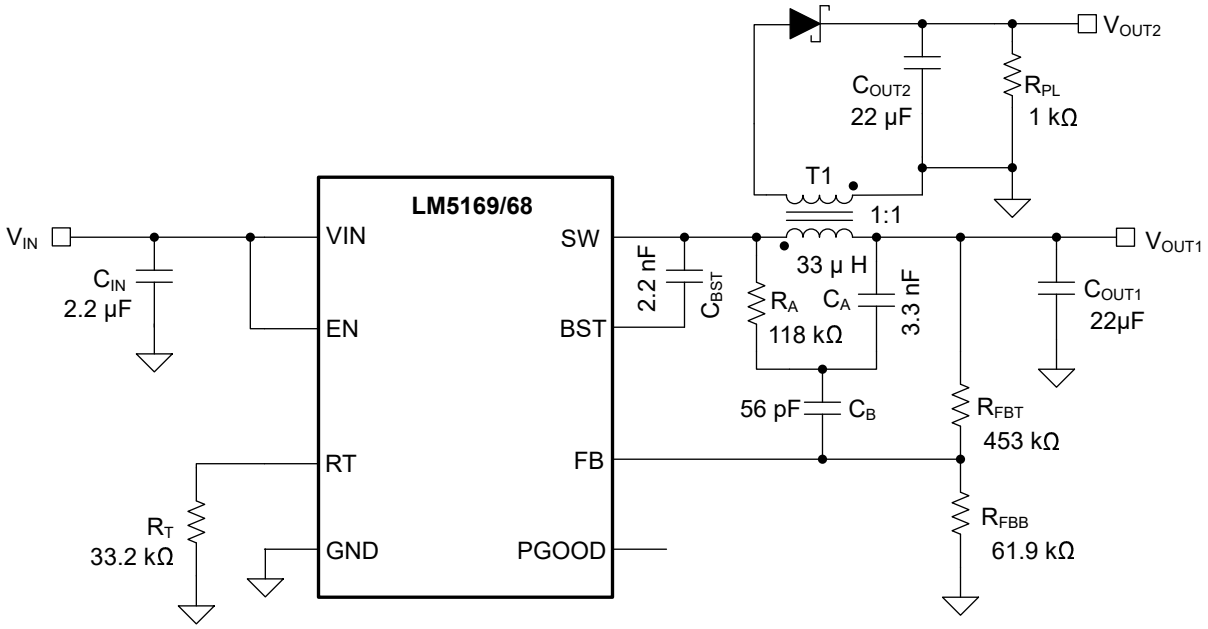


図 8-1. Example Fly-Buck™ Converter Application Circuit

表 8-1. Fly-Buck™ Converter Terminology

TERM	DESCRIPTION
V_{OUT1}	Primary output voltage, as for a buck regulator. This output is tightly regulated by the LM516x.
V_{OUT2}	Secondary output voltage from couple inductor secondary winding. This voltage is not tightly regulated, but depends on parasitic voltage drops on the primary and secondary sides.
I_{OUT1}	Primary output current, as for a buck regulator
I_{OUT2}	Secondary output current from coupled inductor secondary winding

注

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature, not the rated or nameplate values. Use high-quality, low ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

8.2.1 Design Requirements

表 8-2 lists the design requirements for a typical Fly-Buck converter application using the LM5169F.

表 8-2. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Nominal input voltage	24 V
Input voltage range	20 V to 60 V (operational to 115 V)
Primary output voltage	10 V
Secondary output voltage	10 V
Primary output current	0.3 A
Secondary output current	0.3 A
Switching frequency	750 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency (R_T)

The switching frequency of the LM516x is set by the on-time programming resistor connected to the RT pin. 式 5 is used to calculate R_T based on the desired switching frequency. For this example of 750 kHz, 33.2 kΩ is used.

$$R_T(K\Omega) = \frac{V_{OUT} \cdot 2500}{F_{SW}\ (kHz)} \tag{5}$$

Note that at very low duty cycles, the 50-ns minimum controllable on time of the high-side MOSFET, $t_{ON(min)}$, limits the maximum switching frequency. In CCM, $t_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. Use 式 6 to calculate the minimum controllable duty cycle.

$$D_{MIN} = t_{ON(min)} \cdot F_{SW} \tag{6}$$

Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size, and efficiency. Use 式 7 to calculate the maximum supply voltage for a given $t_{ON(min)}$ to maintain the full switching frequency.

$$V_{IN(max)} = \frac{V_{OUT}}{t_{ON(min)} \cdot F_{SW}} \tag{7}$$

8.2.2.2 Transformer Selection

For this Fly-Buck converter application, a coupled inductor (sometimes called a transformer) is required. The first step is to decide upon the turns ratio. In a Fly-Buck converter, the secondary output voltage is slightly less than the reflected primary output voltage scaled by the turns ratio. 式 8 can be used to calculate the turns ratio for a given V_{OUT1} and V_{OUT2}. The nearest integer ratio must be selected. V_{OUT2} is slightly less than calculated due to the secondary diode drop and other parasitic voltage drops in the secondary. Also, keep in mind that the secondary voltage is not fed back to the controller, and is, therefore, not well regulated. For this example, V_{OUT2} is equal to V_{OUT1}, therefore, use a 1:1 turns ratio.

$$\frac{V_{OUT2}}{V_{OUT1}} \cong \frac{N2}{N1} \tag{8}$$

Next, the primary inductance must be calculated. This is the same as calculating the inductance for an ordinary buck regulator, and is based on the desired primary ripple current. Typically, a ripple current of between 20% and 40% of the primary current is used. 式 9 gives the primary current in a Fly-Buck converter and 式 10 gives the

required primary inductance. Using an input voltage of 24 V and the other parameters in 表 8-2, the user arrives at a value of 38 µH. A standard value of 33 µH for this example is selected. Although the inductance can be selected based on the maximum input voltage and lower values of K, a somewhat smaller value of inductance is used in this example to save space on the PCB.

$$I_{PRI}=I_{OUT1}+I_{OUT2}\cdot\frac{N2}{N1} \tag{9}$$

$$L=\frac{(V_{IN}-V_{OUT1})}{K\cdot I_{PRI}\cdot F_{SW}}\cdot\frac{V_{OUT1}}{V_{IN}} \tag{10}$$

where

- K = ripple current factor = 20% to 40%

Finally, the maximum currents in the transformer must be checked. A transformer with a saturation current equal to or greater than the device current limit must be selected. Also, the maximum primary current, and, therefore, the output current, is limited by the current limit of the device. 式 11 can be used to calculate the maximum output current for a given inductance and application parameters.

The magnitude of the ripple current and peak current in the transformer are required to select the output capacitors. These are calculated using 式 12 and 式 13, respectively.

$$I_{PRI\text{-}max}=I_{CL}-\frac{1}{2}\cdot\frac{(V_{IN}-V_{OUT1})}{L\cdot F_{SW}}\cdot\frac{V_{OUT1}}{V_{IN}} \tag{11}$$

where

- I_{CL} = device current limit = $I_{HS\_PK(OC)}$

$$\Delta I=\frac{(V_{IN}-V_{OUT1})}{L\cdot F_{SW}}\cdot\frac{V_{OUT1}}{V_{IN}} \tag{12}$$

$$I_{PK}=I_{PRI}+\frac{(V_{IN}-V_{OUT1})}{L\cdot F_{SW}}\cdot\frac{V_{OUT1}}{V_{IN}} \tag{13}$$

8.2.2.3 Output Capacitor Selection

The primary output capacitor, C_{OUT1}, can be selected using either 式 14 or 式 15. For this design, an output voltage ripple of 5 mV and a load transient of 0.2 V is used. From this, a ripple current of 0.34 A at 60-V input, and a peak transformer current of 0.77 A at full load is calculated. The two output capacitor equations give values of 11 µF and 5 µF. Because of the large derating of ceramic capacitors, C_{OUT1} = 1 × 22 µF is used. Keep in mind that the equations give the minimum capacitance value and in no case must the capacitance of C_{OUT1} be less than 2.2 µF. More output capacitance can be used to improve load transient response. Also note that when using type 3 ripple injection, the actual ripple voltage appearing on the output can be kept small.

$$C_{OUT}>\frac{I_{PK}^2\cdot L}{2\cdot V_{OUT1}\cdot\Delta V_O} \tag{14}$$

where

- I_{PK} = peak transformer current from 式 13
- ΔV_O = output voltage load transient

$$C_{OUT} > \frac{\Delta I}{8 \cdot F_{SW} \cdot V_{ripple}} \quad (15)$$

where

- ΔI = ripple current from 式 12
- V_{ripple} = ripple voltage on primary output

C_{OUT2} is selected using 式 16. In this case, a ripple voltage on the secondary otuput of 20 mV is chosen. The minimum input voltage must be used in this equation. A value of 10 µF is calculated and 1 × 22 µF for C_{OUT2} is selected. Again, the equation gives the minimum capacitance value and in no case must the capacitance of C_{OUT2} be less than 2.2 µF.

$$C_{OUT2} > \frac{I_{OUT2} \cdot V_{OUT1}}{V_{ripple2} \cdot V_{IN} \cdot F_{SW}} \quad (16)$$

Both output capacitors must be X7R ceramics in a 1206 or 1210 case size, and rated for at least twice the output voltage.

8.2.2.4 Secondary Output Diode

The secondary output diode must block the maximum input voltage reflected to the secondary by the transformer turns ratio. 式 17 is used to determine the maximum reverse voltage on the diode. For this example, a value of 70 V is calculated and a 100-V diode is chosen. The diode current rating must be at least equal to the secondary output current with an appropriate factor of safety. Schottky diodes are the best choice for this application. Ultra-fast recovery diodes can also be used. In any case, choose a diode with the lowest turn-off time.

$$V_R > V_{IN} \cdot \frac{N2}{N1} + V_{OUT2} \quad (17)$$

8.2.2.5 Setting Output Voltage

The LM516x voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF} = 1.2 V (typical). A resistor divider programs the ratio from the output voltage V_{OUT1} to V_{REF}.

式 18 is used to calculate R_{FBT} based on a selected R_{FBB}.

$$R_{FBT} = R_{FBB} \cdot \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (18)$$

TI recommends selecting R_{FBB} in the range of 10 kΩ to 1 MΩ for most applications. A larger R_{FBB} consumes less DC current, which is mandatory if light-load efficiency is critical. TI does not recommend R_{FBB} larger than 1 MΩ as the feedback path becomes more susceptible to noise. For this example, R_{FBB} = 61.9 kΩ is chosen. This action gives R_{FBT} = 453 kΩ. Route the feedback trace away from the noisy area of the PCB and keep the feedback resistors close to the FB pin.

8.2.2.6 Input Capacitor

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 2.2 µF of ceramic capacitance is required on the input of the LM516x regulator, connected directly between VIN and GND. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. More input capacitance is required for larger output currents. Keep in mind that the value of 2.2 µF is the actual value after all derating is applied. For this example, 4x 1-µF, 250-V, X7R (or better) ceramic capacitors are chosen due to voltage derating. If larger case size, higher voltage capacitors, or both can be used, then the

total number can be reduced. Designs with reduce input voltage range can use capacitors with lower voltage ratings.

Many times, using an electrolytic capacitor on the input in parallel with the ceramics is desirable. This statement is especially true if long leads or traces (greater than about 5 cm) are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. Use 式 19 to calculate the approximate RMS current. This value must be checked against the manufacturers maximum ratings.

$$I_{RMS} \approx \frac{I_{PRI}}{2} \tag{19}$$

The input capacitor is part of the buck converter high di/dt current loop. The high di/dt current, together with excessive parasitic inductance between the IC and the input capacitor, can result in excessive voltage ringing on the SW node of the IC. The placement of the input capacitor on the board is critical for minimizing the parasitic inductance in the high di/dt loop and accordingly minimizing the SW node ringing at each switching.

For designs targeting the maximum operating voltage of the regulator, make sure that the ringing on the SW node must not exceed the abs max rating of the device. The SW node ringing is a function of how well the input capacitor is positioned with respect to the IC. Refer to the PCB layout examples in 図 8-41 and 図 8-42 for proper placement of the input capacitors.

8.2.2.7 Type-3 Ripple Network

A Type 3 ripple generation network uses an RC filter consisting of R_A and C_A across SW and V_{OUT1} to generate a triangular ramp that is in phase with the inductor current. This triangular ramp is then AC-coupled into the feedback node through capacitor C_B. Type 3 ripple injection is an excellent choice for applications where low output voltage ripple is crucial, and is chosen for this example.

式 20 is used to calculate C_A. With the values used in this example, C_A > 245 pF. A value of 3300 pF is selected to keep R_A within practical limits. In general, the user needs 20 mV of ripple at the feedback pin for reliable operation, calculated at nominal input voltage. The minimum value of ripple must not be less than 12 mV at minimum input voltage. Using 式 21 with nominal input voltage, a value of R_A > 117 kΩ was found and a value of 118 kΩ is selected.

$$C_A \geq \frac{10}{F_{SW} \cdot R_{FBB} || R_{FBT}} \tag{20}$$

$$R_A \geq \frac{(V_{IN} - V_{OUT1}) \cdot V_{OUT1}}{0.02 \cdot V_{IN} \cdot F_{SW} \cdot C_A} \tag{21}$$

While the magnitude of the generated ripple does not affect the output voltage ripple, the magnitude produces a DC error of approximately half the amplitude of the generated ripple, scaled by the feedback divider ratio. Therefore, the amount of DC offset, tolerable in the output voltage, imposes an upper bound on the feedback ripple.

Finally, 式 22 is used to calculate the coupling capacitance C_B. In the equation, T_R is the approximate settling time of the control loop to a load transient disturbance. This was taken as 50 µs.

$$C_B \geq \frac{T_R}{3 \cdot R_{FBT}} \tag{22}$$

where

- T_R = 50 µs (typical)

In this example, a value of > 37 pF was calculated for C_B and a value of 56 pF is selected. This value avoids excessive coupling capacitor discharge by the feedback resistors during sleep intervals when operating at light loads. Note that the minimum value of C_B is 47 pF.

8.2.2.8 C_{BST} Selection

The LM516x requires a bootstrap capacitor to be connected between the BST pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 2.2 nF is required. Be sure to take into account the D.C. bias derating of the capacitor. The value of C_{BST} must not exceed 2.5 nF.

8.2.2.9 Minimum Secondary Output Load

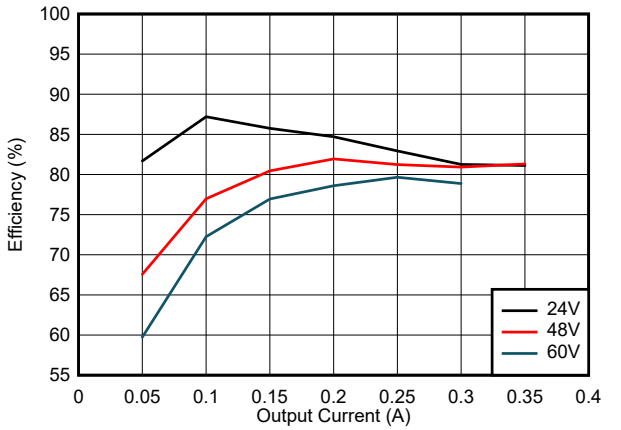
The secondary output must have a "dummy" load connected at all times to prevent the output voltage from rising too high under certain conditions. Because the secondary output is not tightly regulated by the control loop, and because of transformer and diode parasitics, C_{OUT2} can charge to high levels unless the energy is dissipated in the secondary output load. In this example, a 1-kΩ resistor is used as a minimum load on the secondary output. A Zener diode can also be used to clamp the secondary output voltage, if desired.

8.2.2.10 Example Design Summary

The preceding design procedure is typical of the steps needed to create a Fly-Buck converter with LM516x. Please see the *LM5168FEVM User's Guide* for a more detailed BOM example. Also, see the section *Related Documentation* for more information about designing Fly-Buck converter power stages.

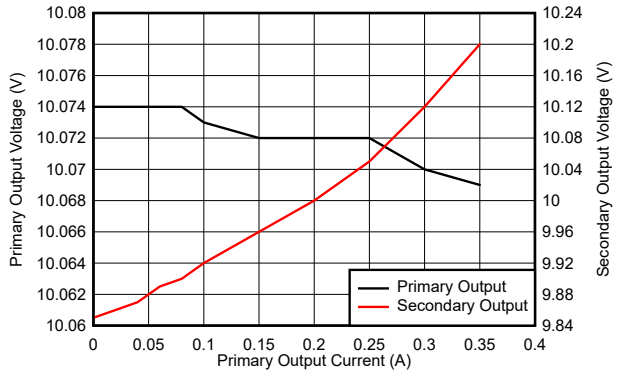
8.2.3 Application Curves

The curves in this section were taken using the LM5169FDDAR. For a detailed schematic pertaining to these curves, see the*LM5168FEVM User's Guide*. Unless otherwise specified the following conditions apply: T_A = 25°C.



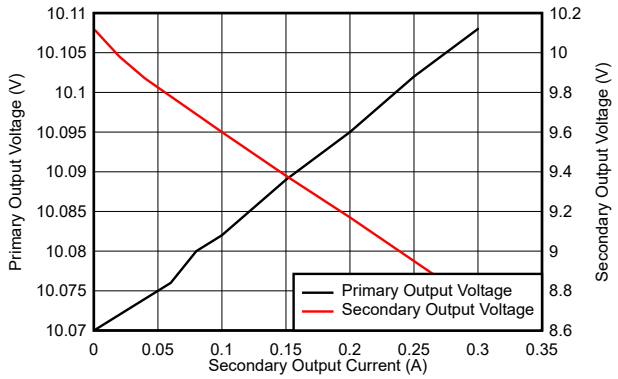
V_{OUT1} = V_{OUT2} = 10 V I_{OUT1} = I_{OUT2} F_{SW} = 750 kHz
Primary DCR = 0.62 Ω

図 8-2. Efficiency



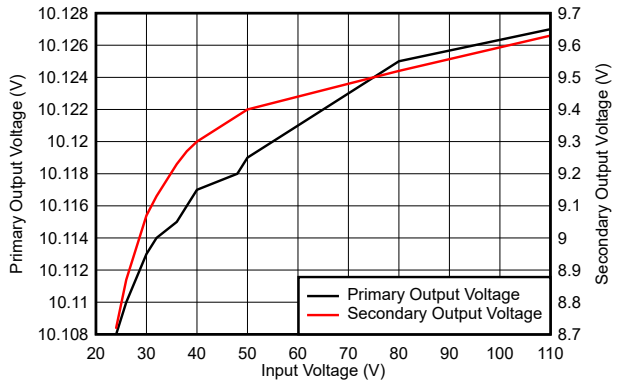
V_{IN} = 24 V I_{OUT2} = 10 mA

図 8-3. Load Regulation vs Primary Load Current



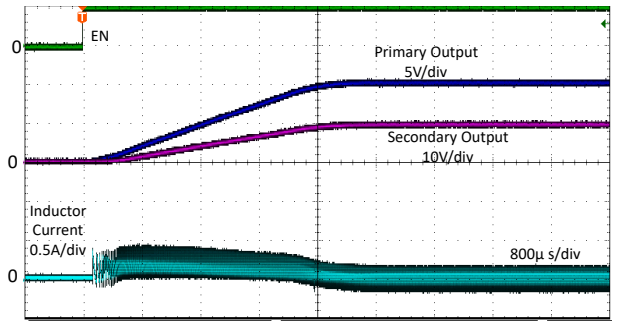
V_{IN} = 24 V I_{OUT1} = 0.3 A

図 8-4. Load Regulation vs Secondary Load Current



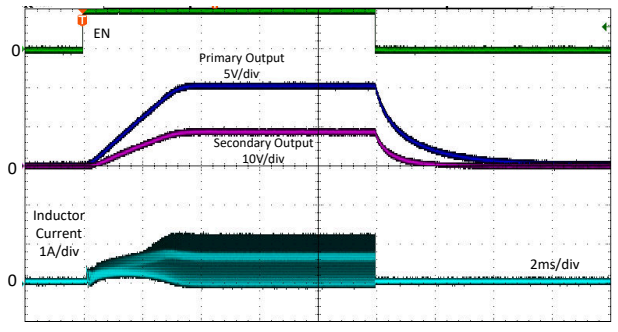
V_{IN} = 24 V I_{OUT1} = I_{OUT2} = 0.3 A

図 8-5. Line Regulation



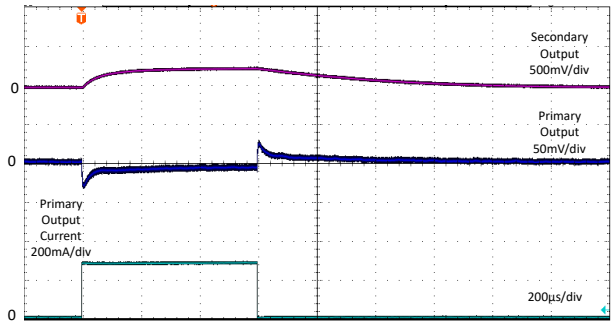
V_{IN} = 24 V I_{OUT1} = I_{OUT2} = 10 mA

図 8-6. Light Load Start-Up from EN



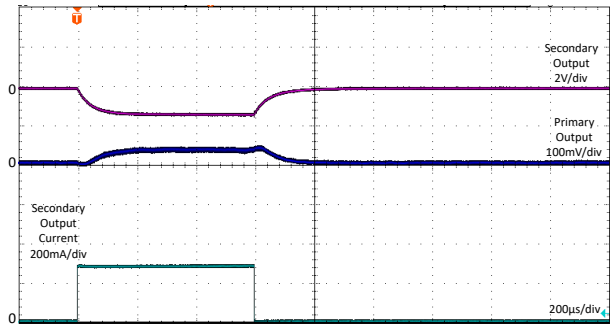
V_{IN} = 24 V I_{OUT1} = I_{OUT2} = 300 mA

図 8-7. Full Load Start-Up from EN



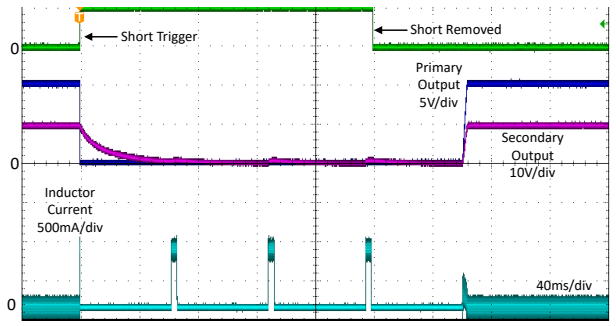
V_{IN} = 24 V I_{OUT2} = 10 mA
I_{OUT1} = 0 A to 300 mA

図 8-8. Load Transient on Primary Output



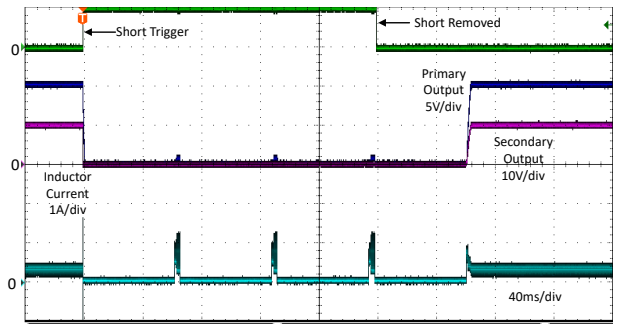
V_{IN} = 24 V I_{OUT1} = 10 mA
I_{OUT2} = 0 A to 300 mA

図 8-9. Load Transient on Secondary Output



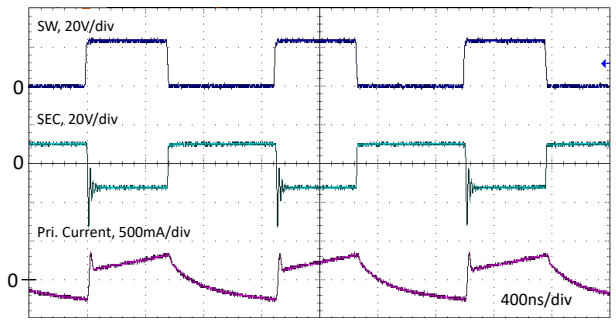
V_{IN} = 24 V I_{OUT2} = 10 mA

図 8-10. Short Circuit on Primary Output



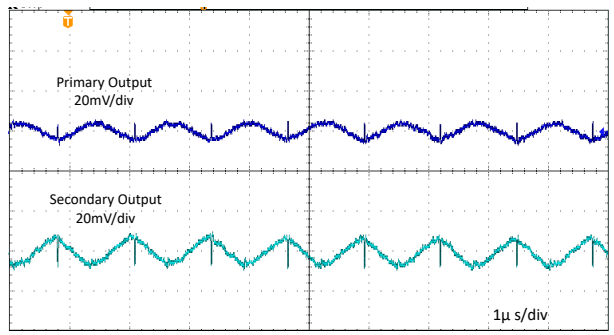
V_{IN} = 24 V I_{OUT1} = 0.3 A

図 8-11. Short Circuit on Secondary Output



V_{IN} = 24 V I_{OUT} = I_{OUT2} = 0.2 A

図 8-12. Typical Switching Waveforms



V_{IN} = 24 V I_{OUT} = I_{OUT2} = 0.2 A

図 8-13. Typical Output Ripple

8.3 Typical Buck Application

The LM5168P and LM5169P are designed for buck applications by operating in DEM mode, with light load PFM operation. 図 8-14 shows the schematic for a 5-V output buck regulator capable of delivering 300 mA of load current, using the LM5168P.

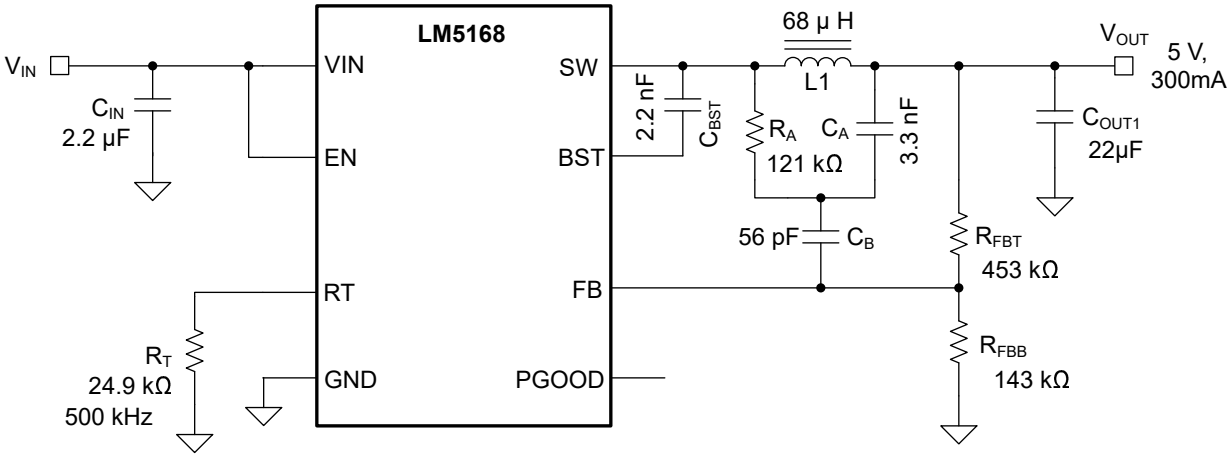


図 8-14. Example Buck Application Circuit

注

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature, not the rated or nameplate values. Use high-quality, low ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

8.3.1 Design Requirements

表 8-3 lists the design requirements for a typical buck application using the LM51698P.

表 8-3. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Nominal input voltage	24 V
Input voltage range	12 V to 115 V
Output Voltage	5 V
Output Current	0.3 A
Switching frequency	500 kHz

8.3.2 Detailed Design Procedure

8.3.2.1 Switching Frequency (R_T)

The switching frequency of the LM5168 is set by the on-time programming resistor connected to the R_T pin. 式 23 is used to calculate R_T based on the desired switching frequency and output voltage. For this example of 500 kHz and 5 V, 24.9 kΩ is used.

$$R_T(K\Omega) = \frac{V_{OUT} \cdot 2500}{F_{SW}\ (kHz)} \tag{23}$$

Note that at very low duty cycles, the 50-ns minimum controllable on time of the high-side MOSFET, $t_{ON(min)}$, limits the maximum switching frequency. In CCM, $t_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. Use 式 24 to calculate the minimum controllable duty cycle.

$$D_{MIN} = t_{ON(min)} \cdot F_{SW} \tag{24}$$

Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size, and efficiency. Use 式 25 to calculate the maximum supply voltage for a given $t_{ON(min)}$ to maintain the full switching frequency.

$$V_{IN(max)} = \frac{V_{OUT}}{t_{ON(min)} \cdot F_{SW}} \tag{25}$$

8.3.2.2 Buck Inductor Selection

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 50% of the rated load current at nominal input voltage. Use 式 26 to calculate the inductance. For this example, assume V_{IN} = 12 V, F_{SW} = 500 kHz, and a ripple current of 30% of 0.3A. This gives us an inductance of about 65 µH. Choose the next standard value of 68 µH for this design. Next, use 式 27 to calculate the actual inductor ripple current across the input voltage range. Finally, use 式 28 to determine the peak inductor current at our maximum input voltage and compare with the current limit of the LM5168. Arrive at a peak current of about 0.37 A at V_{IN} = 115 V, which is less than the current limit of the LM5168.

$$L = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{26}$$

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{27}$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{28}$$

Ideally, the saturation current rating of the inductor is at least as large as the peak current limit. This size makes sure that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, powered iron cores have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

8.3.2.3 Setting the Output Voltage

The LM516x regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF} = 1.2 V (typical). A resistor divider programs the output voltage based on 式 29 .

TI recommends selecting R_{FBB} in the range of 10 kΩ to 1 MΩ for most applications. A larger R_{FBB} consumes less DC current, which is mandatory if light-load efficiency is critical. TI does not recommend R_{FBB} larger than 1 MΩ as the feedback path becomes more susceptible to noise. For this example select R_{FBB} = 143 kΩ. This action gives R_{FBT} = 453 kΩ. Route the feedback trace away from the noisy area of the PCB and keep the feedback resistors close to the FB pin.

$$R_{FBT} = R_{FBB} \cdot \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{29}$$

8.3.2.4 Type-3 Ripple Network

A type 3 ripple injection network is selected for this example. This network uses an RC filter consisting of R_A and C_A across SW and V_{OUT} to generate a triangular ramp that is in phase with the inductor current. This triangular ramp is then AC-coupled into the feedback node through capacitor C_B. Type 3 ripple injection is an excellent choice for applications where low output voltage ripple is crucial, and allows the use of low ESR ceramic output capacitors.

式 30 is used to calculate C_A. With the values used in this example, C_A > 184 pF. A value of 3300 pF is selected to keep R_A within practical limits. In general, the user needs 20 mV of ripple at the feedback pin for reliable operation, calculated at nominal input voltage. The minimum value of ripple must not be less than 12 mV at minimum input voltage. Using 式 31 with nominal input voltage, a value of R_A > 120 kΩ was found and a value of 121 kΩ is selected.

$$C_A \geq \frac{10}{F_{SW} \cdot R_{FBB} || R_{FBT}} \tag{30}$$

$$R_A \geq \frac{(V_{IN} - V_{OUT1}) \cdot V_{OUT1}}{0.02 \cdot V_{IN} \cdot F_{SW} \cdot C_A} \tag{31}$$

While the magnitude of the generated ripple does not affect the output voltage ripple, the magnitude produces a DC error of approximately half the amplitude of the generated ripple, scaled by the feedback divider ratio. Therefore, the amount of DC offset, tolerable in the output voltage, imposes an upper bound on the feedback ripple.

Finally, 式 32 is used to calculate the coupling capacitance C_B. In the equation, T_R is the approximate settling time of the control loop to a load transient disturbance. This was taken as 50 µs.

$$C_B \geq \frac{T_R}{3 \cdot R_{FBT}} \tag{32}$$

where

- T_R = 50 µs (typical)

In this example, a value of > 37 pF was calculated for C_B and a value of 56 pF is selected. This value avoids excessive coupling capacitor discharge by the feedback resistors during sleep intervals when operating at light loads. Note that the minimum value of C_B is 47 pF.

8.3.2.5 Output Capacitor Selection

The type 3 ripple injection network allows the use of small, low ESR, ceramic output capacitors, while the ripple injection network provides the proper signal to the regulation comparator.

One way to select the value of output capacitance is with the help of 式 33. This equation sizes the output capacitor based on a specified load current transient and output voltage transient.

$$C_{OUT} > \frac{L \cdot \left(I_{OUT} + \frac{\Delta I_L}{2}\right)^2}{2 \cdot \Delta V \cdot V_{OUT}} \tag{33}$$

Where:

- ΔV = Change in output voltage during load transient.
- ΔI_L = inductor ripple current from 式 27

For this example we specify ΔV = 50 mV for a full load transient of 300 mA. I_{peak} is calculated using 式 28. Arrive at C_{OUT} greater than about 17 µF. With voltage coefficients of ceramic capacitors taken in consideration, a 22-µF, 25-V rated capacitor with X7R dielectric is selected. More output capacitance can be used to provide smaller load transients or lower output voltage ripple. Keep in mind that the minimum output capacitance must be > 2.2 µF. 式 34 can be used to estimate the switching frequency output ripple, assuming that the output capacitor ESR is not dominant.

$$V_r \cong \frac{\Delta I_L}{8 \cdot F_{SW} \cdot C_{OUT}} \tag{34}$$

Where:

- V_r = peak-to-peak output voltage ripple at the switching frequency
- ΔI_L = inductor ripple current from 式 27.

8.3.2.6 Input Capacitor Considerations

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 2.2 µF of ceramic capacitance is required on the input of the LM516x regulator, connected directly between VIN and GND. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. More input capacitance is required for larger output currents. Keep in mind that the value of 2.2 µF is the actual value after all derating is applied. For this example, 4x 1-µF, 250-V, X7R (or better) ceramic capacitors are chosen due to voltage derating. If larger case size, higher voltage capacitors, or both can be used, then the total number can be reduced. Designs with reduced input voltage range can use capacitors with lower voltage ratings.

Many times, it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces (greater than about 5 cm) are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. Use 式 35 to calculate the approximate RMS current. This value must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \quad (35)$$

The input capacitor is part of the buck converter high di/dt current loop. The high di/dt current, together with excessive parasitic inductance between the IC and the input capacitor, can result in excessive voltage ringing on the SW node of the IC. The placement of the input capacitor on the board is critical for minimizing the parasitic inductance in the high di/dt loop and accordingly minimizing the SW node ringing at each switching.

For designs targeting the maximum operating voltage of the regulator, it is important to ensure the ringing on the SW node must not exceed the abs max rating of the device. The SW node ringing is a function of how well the input capacitor is positioned with respect to the IC. Refer to the PCB layout examples in 図 8-41 and 図 8-42 for proper placement of the input capacitors.

8.3.2.7 C_{BST} Selection

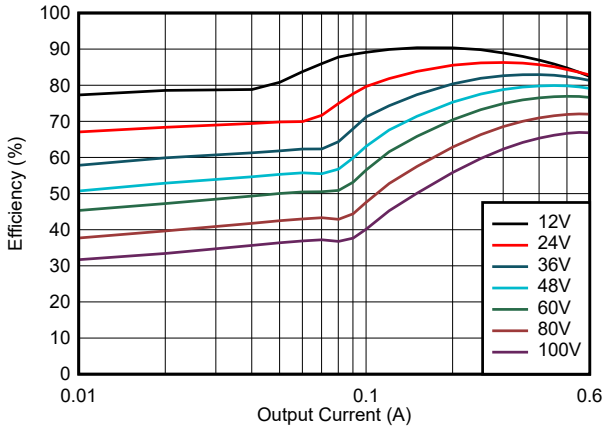
The LM516x requires a bootstrap capacitor to be connected between the BST pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 2.2 nF is required. Be sure to take into account the D.C. bias derating of the capacitor. The value of C_{BST} must not exceed 2.5 nF.

8.3.2.8 Example Design Summary

The preceding design procedure is typical of the steps needed to create a buck regulator with LM516x. For another example of designing a buck regulator with the LM516x see the *LM56168PEVM User's Guide*. Also, see the section *Related Documentation* for more information about designing COT buck converters.

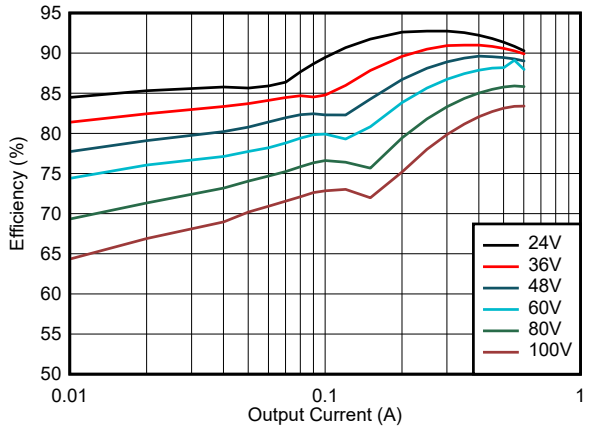
8.3.3 Application Curves

The curves in this section were taken using the LM5169PDDAR. Unless otherwise specified the following conditions apply: T_A = 25°C.



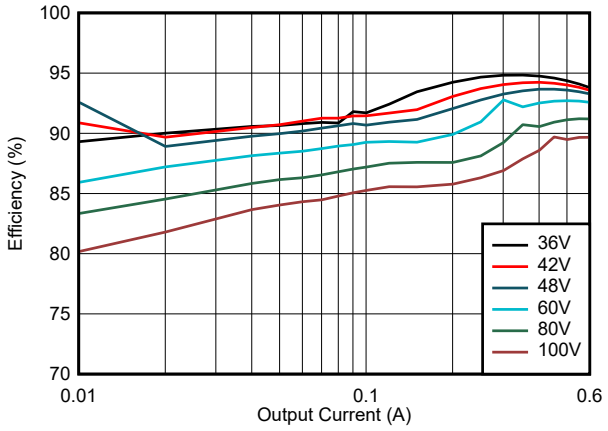
V_{OUT} = 5 V F_{SW} = 500 kHz

図 8-15. Efficiency: V_{OUT} = 5 V



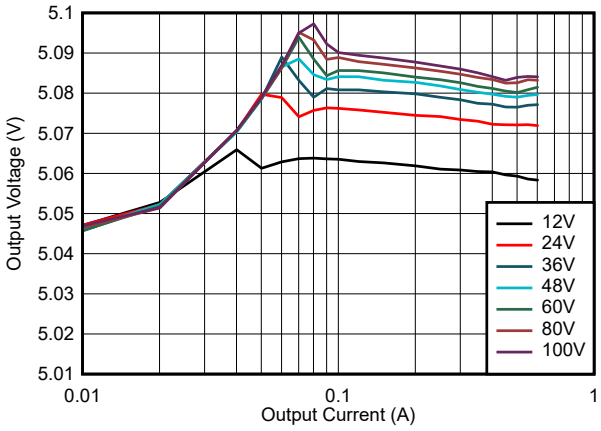
V_{OUT} = 12 V F_{SW} = 500 kHz

図 8-16. Efficiency: V_{OUT} = 12 V



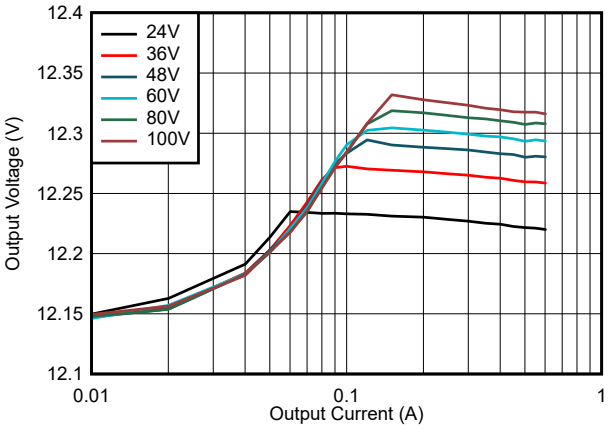
V_{OUT} = 24 V F_{SW} = 500 kHz

図 8-17. Efficiency: V_{OUT} = 24 V



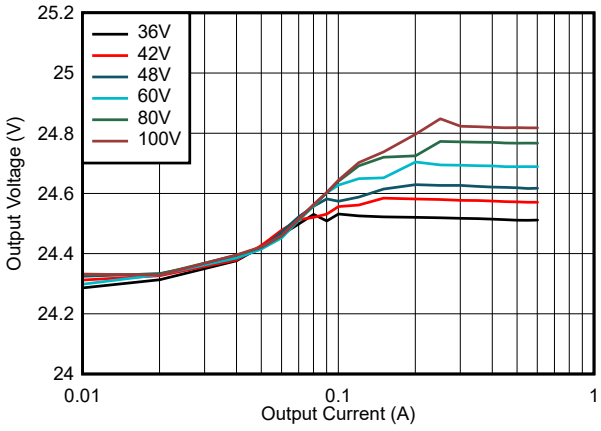
V_{OUT} = 5 V F_{SW} = 500 kHz

図 8-18. Line and Load Regulation: V_{OUT} = 5 V



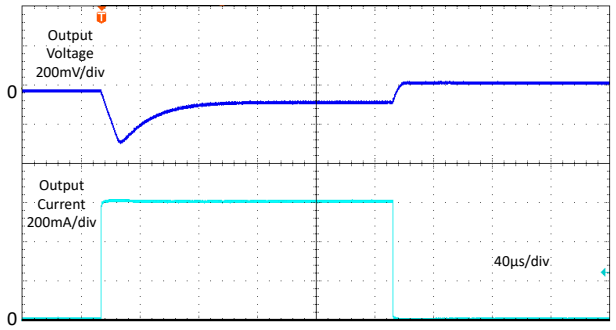
V_{OUT} = 12 V F_{SW} = 500 kHz

図 8-19. Line and Load Regulation: V_{OUT} = 12 V



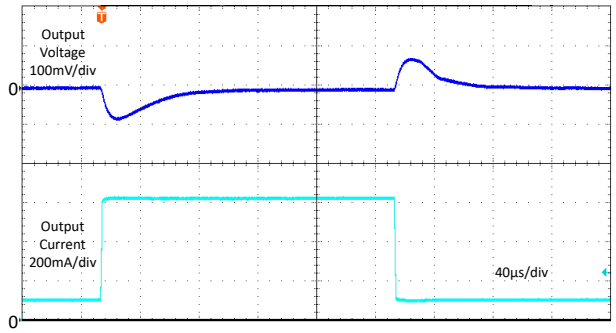
V_{OUT} = 24 V F_{SW} = 500 kHz

図 8-20. Line and Load Regulation: V_{OUT} = 24 V



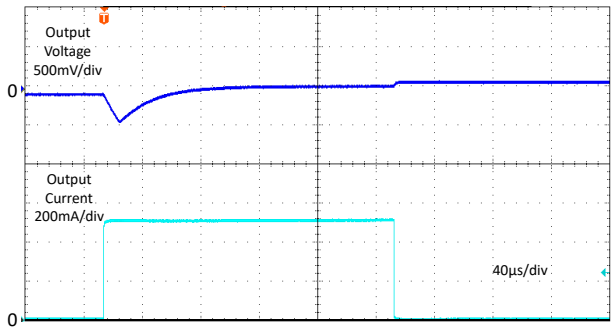
V_{IN} = 48 V I_{OUT} = 0 A to 0.6 A
$T_R = T_F$ = 1 µs

図 8-21. Load Transient: V_{OUT} = 5 V



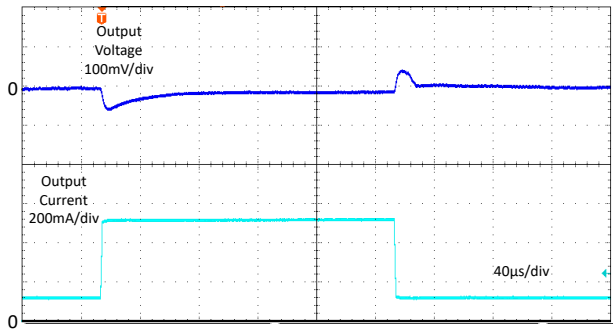
V_{IN} = 48 V I_{OUT} = 0.1 A to 0.6 A
$T_R = T_F$ = 1 µs

図 8-22. Load Transient: V_{OUT} = 5 V



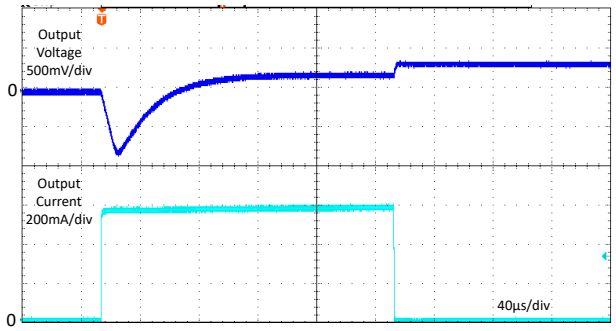
V_{IN} = 48 V I_{OUT} = 0 A to 0.5 A
$T_R = T_F$ = 1 µs

図 8-23. Load Transient: V_{OUT} = 12 V



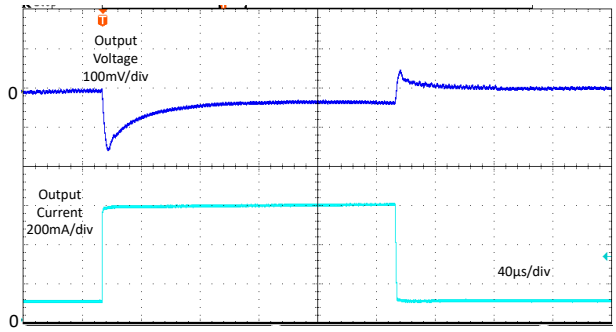
V_{IN} = 48 V I_{OUT} = 0.1 A to 0.5 A
$T_R = T_F$ = 1 µs

図 8-24. Load Transient: V_{OUT} = 12 V



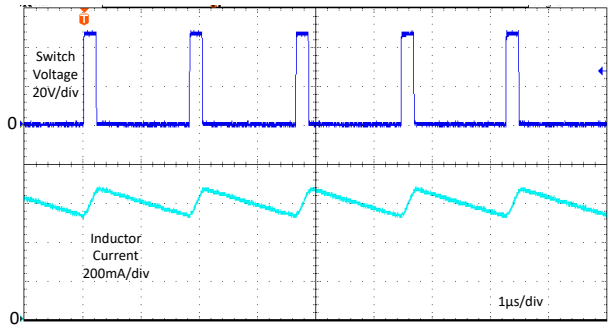
V_{IN} = 36 V I_{OUT} = 0 A to 0.6 A
$T_R = T_F$ = 1 µs

図 8-25. Load Transient: V_{OUT} = 24 V



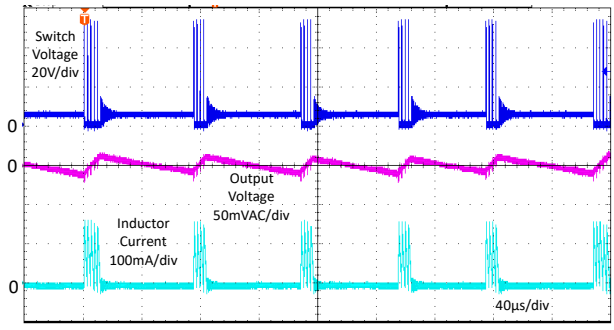
V_{IN} = 36 V I_{OUT} = 0.1 A to 0.6 A
$T_R = T_F$ = 1 µs

図 8-26. Load Transient: V_{OUT} = 24 V



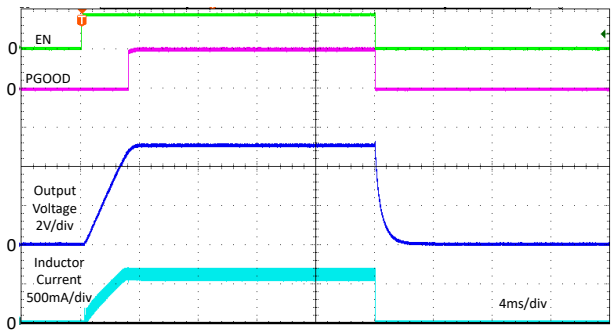
V_{IN} = 48 V V_{OUT} = 5 V
I_{OUT} = 600 mA F_{SW} = 500 kHz

図 8-27. Typical Switching Waveforms



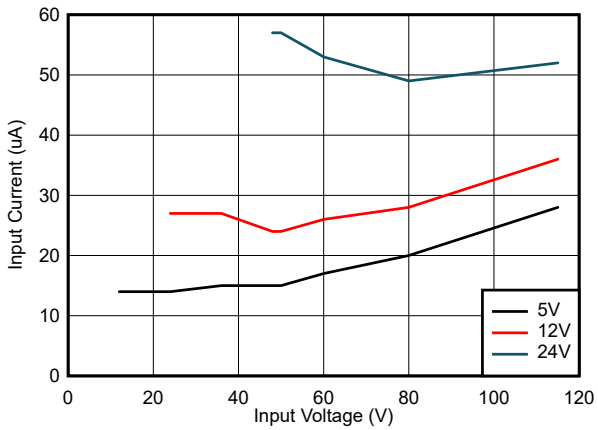
V_{IN} = 48 V V_{OUT} = 5 V
I_{OUT} = 10 mA

図 8-28. Typical Switching Waveforms



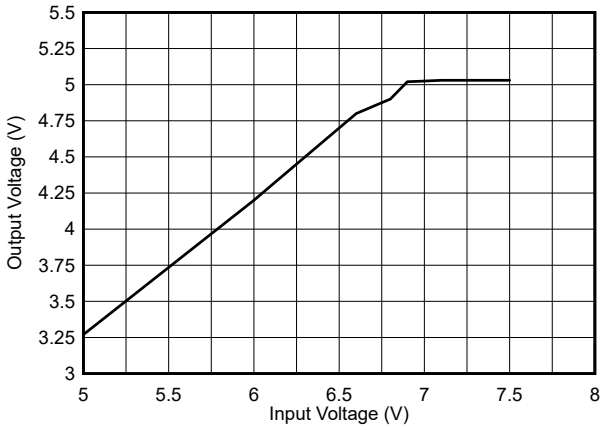
V_{IN} = 48 V V_{OUT} = 5 V
I_{OUT} = 600 mA

図 8-29. Typical Start-up Waveforms



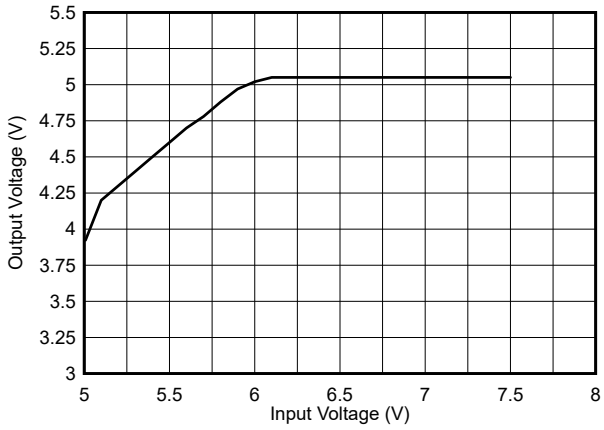
I_{OUT} = 0 A LM5169P

図 8-30. No-Load Input Supply Current



I_{OUT} = 600 mA V_{OUT} = 5 V

図 8-31. Drop-Out Response



I_{OUT} = 300 mA

図 8-32. Drop-Out Response

表 8-4. BOM for Application Curves

V_{OUT}	R_A	R_{FBB}	R_{FBT}	C_A	C_B	C_{OUT}	L
5 V	121 kΩ	143 kΩ	453 kΩ	3300 pF	56 pF	2x 22 µF	68 µH, 0.17 Ω
12 V	182 kΩ	49.9 kΩ	453 kΩ	3300 pF	56 pF	2x 22 µF	68 µH, 0.17 Ω
24 V	243 kΩ	23.7 kΩ	453 kΩ	3300 pF	56 pF	2x 22 µF	68 µH, 0.17 Ω

8.4 Power Supply Recommendations

The LM516x buck converter is designed to operate from a wide input voltage range between 6 V and 115 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use 式 36 to estimate the average input current.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{36}$$

where

- η = efficiency

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, the parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the converter is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps to damp the input resonant circuit and reduce any voltage overshoots. A 10-µF electrolytic capacitor with a typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *Simple Success with Conducted EMI for DC-DC Converters Application Report* provides helpful suggestions when designing an input filter for any switching regulator.

8.5 Layout

8.5.1 Thermal Considerations

As with any power conversion device, the LM516x dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$, of the application
- PCB layout

The maximum internal die temperature for the LM516x must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 37 shows the relationships between the important parameters. Seeing that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. Note that these curves include the power loss in the inductor. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics application report*, the value of $R_{\theta JA}$ given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. The data given for $R_{\theta JC(bott)}$ and Ψ_{JT} can be useful when determining thermal performance. The value of $R_{\theta JA(EVM)}$ is applicable to the LM5168PEVM and is given for reference only. See the *Semiconductor and IC Package Thermal Metrics application report* for more information and the resources given at the end of this section.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (37)$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature, flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The LM516x features a die attach paddle, or "thermal pad" (EP), to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Typical examples of $R_{\Theta JA}$ can be found in 図 8-33 and 図 8-34. The copper area given in the graph is for each layer. The top and bottom layers are 2-oz copper each, while the inner layers are 1 oz.

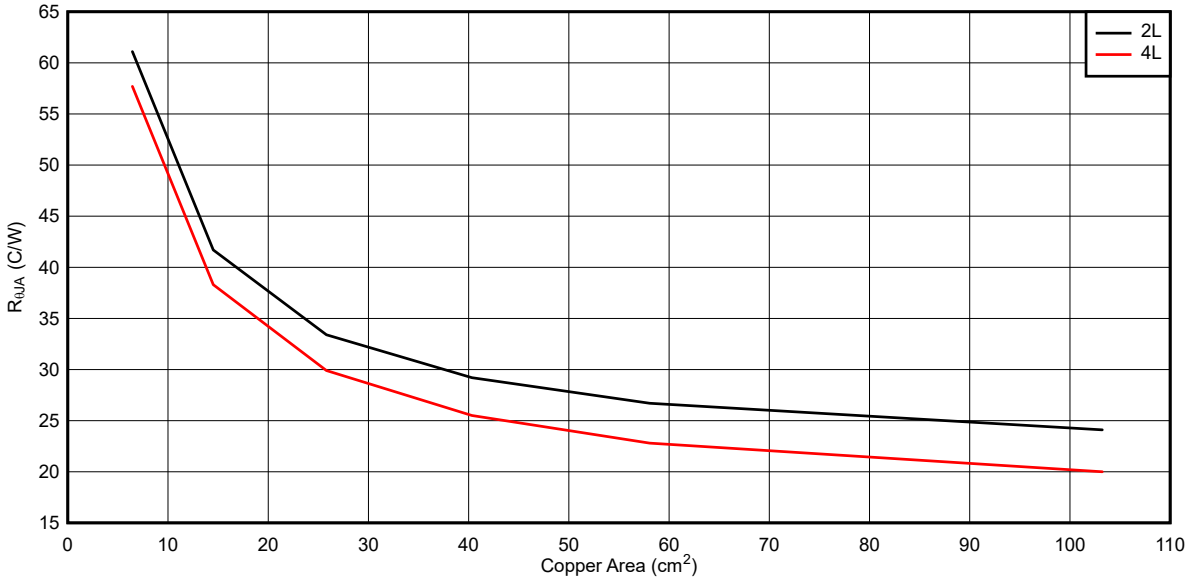


図 8-33. Typical $R_{\Theta JA}$ Versus Copper Area for DDA package

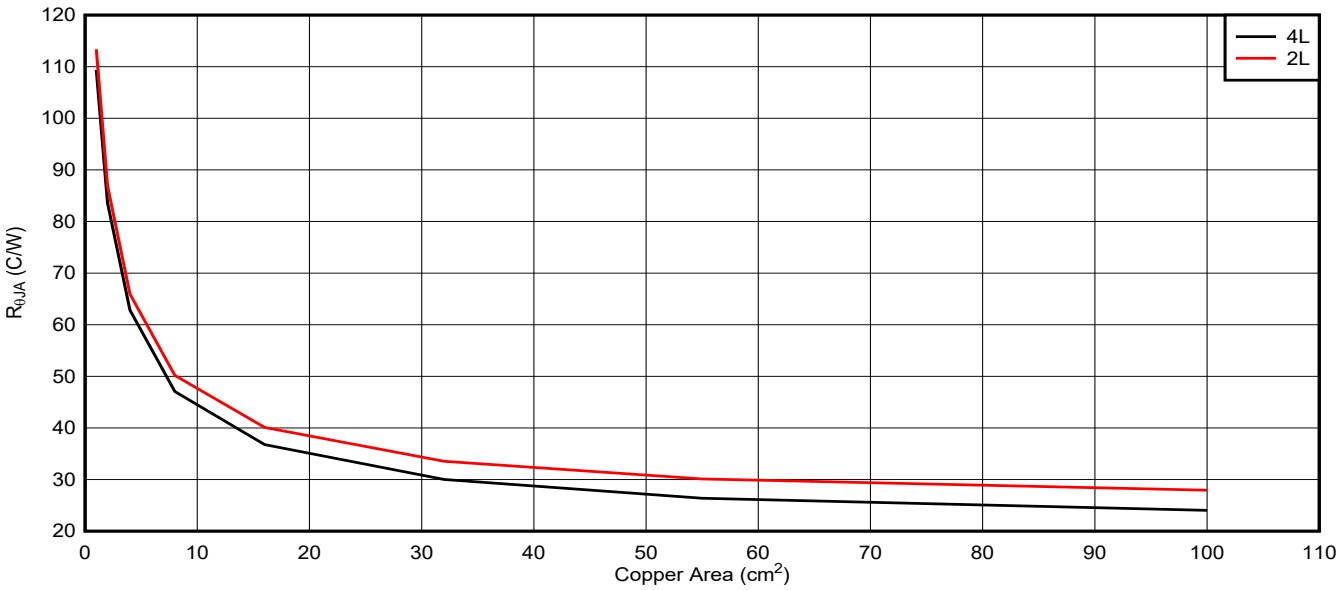
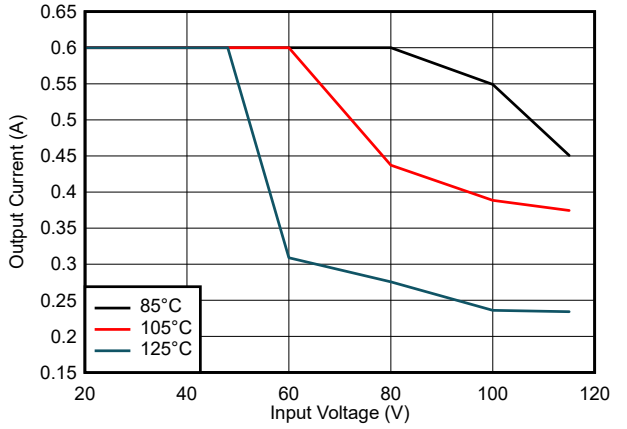


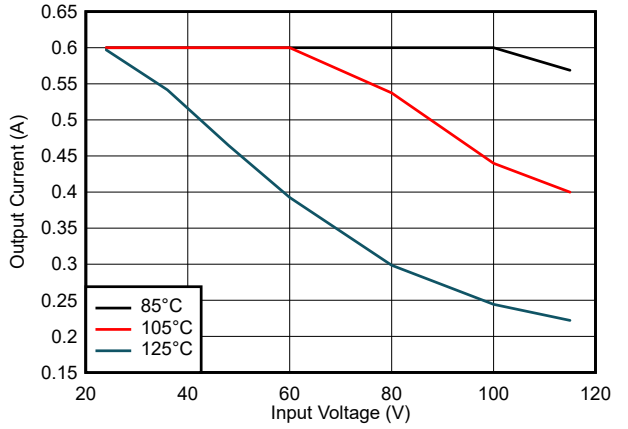
図 8-34. Typical $R_{\Theta JA}$ Versus Copper Area for NGU package

The data in 図 8-35 and 図 8-36 can be used as a guide to determine the maximum output current for a given set of conditions. The particular conditions under which these graphs were taken are indicated in the notes below each graph.



V_{OUT} = 5 V L = 68 µH F_{SW} = 500 kHz
$R_{\Theta JA}$ = 24 °C/W

図 8-35. Maximum Output Current: VOUT = 5 V



V_{OUT} = 12 V L = 68 µH F_{SW} = 500 kHz
$R_{\Theta JA}$ = 24 °C/W

図 8-36. Maximum Output Current: VOUT = 12 V

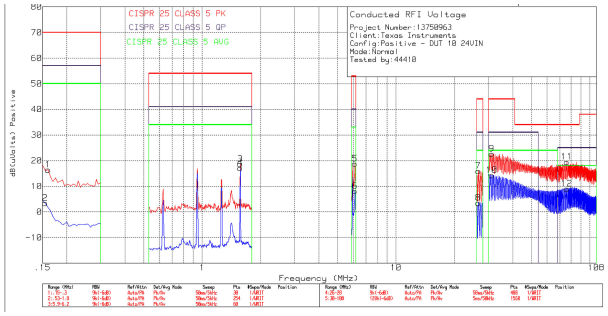
Remember that the data given in 図 8-33 through 図 8-36 is for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

The following resources can be used as a guide to excellent thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *LM5013 Thermal Optimization and Example PCB design application note*
- *Semiconductor and IC Package Thermal Metrics application report*
- *AN-2020 Thermal Design By Insight, Not Hindsight application report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages application report*
- *Using New Thermal Metrics application report*
- *PCB Thermal Design Tips for Automotive DC/DC Converters application report*

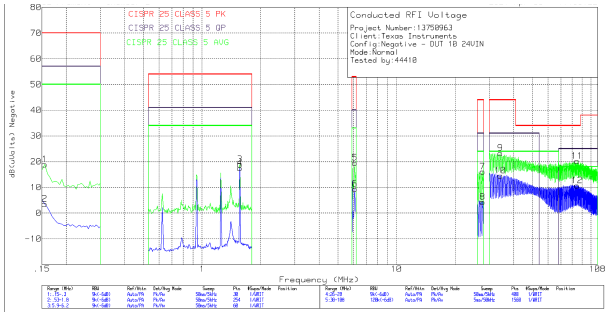
8.5.2 Typical EMI Results

図 8-37 and 図 8-38 show typical conducted EMI results for the LM5169PDDAR using the LM5168PEVM. See the *LM5168PEVM User's Guide* for details regarding the EMI input filter BOM. 図 8-37 through 図 8-39 show typical conducted EMI results for the LM5169PNGUR using the LM5169PEVM. A series RC snubber was used on the SW node to GND consisting of a 470-pF capacitor and 1-Ω resistor. The results given here are typical and are provided for informational purposes only. EMI results depend critically on PCB layout and test setup. The figures indicate the test parameters.



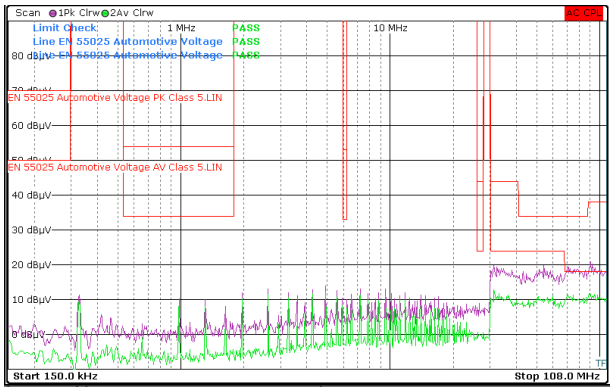
V_{IN} = 24 V V_{OUT} = 12 V I_{OUT} = 600 mA
F_{SW} = 300 kHz

図 8-37. LM5169PDDAR Conducted EMI (Positive Rail)



V_{IN} = 24 V V_{OUT} = 12 V I_{OUT} = 600 mA
F_{SW} = 300 kHz

図 8-38. LM5169PDDAR Conducted EMI (Negative Rail)



V_{IN} = 24 V V_{OUT} = 12 V I_{OUT} = 600 mA
F_{SW} = 300 kHz

図 8-39. LM5169PNGUR Conducted EMI (Positive Rail)

8.5.3 Layout Guidelines

PCB layout is a critical portion of good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power supply performance.

- Bypass the VIN pin to GND with a low-ESR ceramic bypass capacitor with a high-quality dielectric to help eliminate these problems. Place C_{IN} as close as possible to the LM516x VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top-side planes that connect to the GND pin and GND PAD.
- Minimize the loop area formed by the input capacitor connections to the VIN and GND pins. The input capacitor is part of the buck converter high di/dt current loop. The high di/dt current, together with excessive parasitic inductance between the IC and the input capacitor, can result in excessive voltage ringing on the SW node of the IC. The placement of the input capacitor on the board is critical for minimizing the parasitic

inductance in the high di/dt loop and accordingly minimizing the SW node ringing at each switching. For designs targeting the maximum operating voltage of the regulator, make sure the ringing on the SW node must not exceed the abs max rating of the device. The SW node ringing is a function of how well the input capacitor is positioned with respect to the IC. Refer to the PCB layout examples in 図 8-41 and 図 8-42 for proper placement of the input capacitors.

- Locate the inductor close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive capacitive coupling.
- Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
- Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
- Have a single-point ground connection to the plane. Route the ground connections for the feedback, and enable components to the ground plane. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
- Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Minimize trace length to the FB pin. Place both feedback resistors, R_{FB1} and R_{FB2}, close to the FB pin. Place C_{FF} (if used) directly in parallel with R_{FB1}. If output set-point accuracy at the load is important, connect the V_{OUT} sense at the load. Route the V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a grounded shielding layer.
- Note that the R_T pin is sensitive to noise. Thus, locate the R_T resistor as close as possible to the device and route with minimal lengths of trace. The parasitic capacitance from RT to GND must not exceed 20 pF.
- Provide adequate heat sinking for the LM516x to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad to the PCB ground plane. If the PCB has multiple copper layers, these thermal vias must also be connected to inner layer heat-spreading ground planes.

8.5.3.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger the area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimizing radiated EMI is to identify the pulsing current path and minimize the area of that path. 図 8-40 denotes the critical switching loop of the buck converter power stage in terms of EMI. The topological architecture of a buck converter means that a particularly high di/dt current path exists in the loop comprising the input capacitor and the integrated MOSFETs of the LM516x, and reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory.

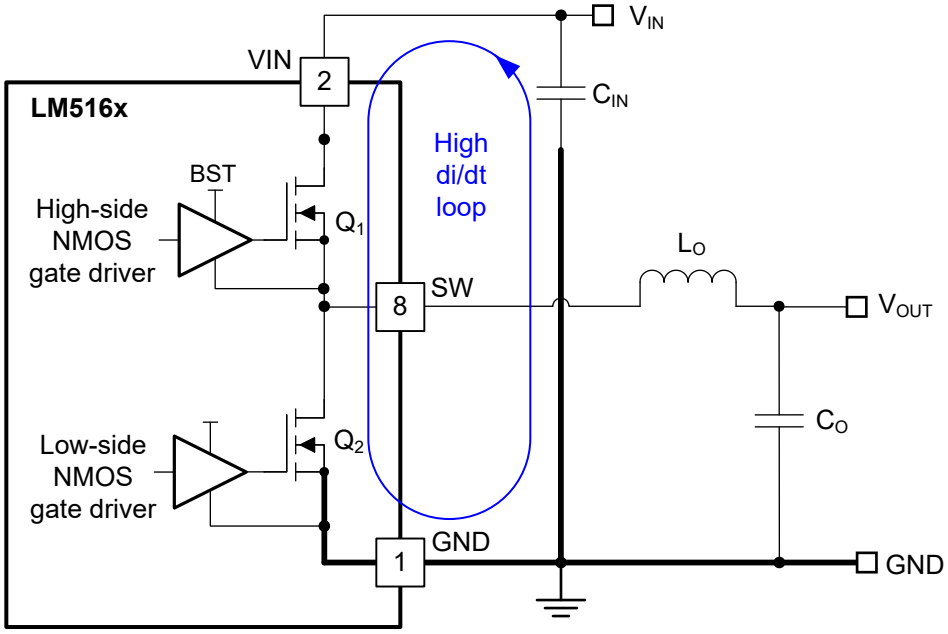


図 8-40. Critical Current Loops in the Buck Converter

The input capacitor provides the primary path for the high di/dt components of the current of the high-side MOSFET. Placing a ceramic capacitor as close as possible to the VIN and GND pins is the key to EMI reduction. Keep the trace connecting SW to the inductor as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitor close to the V_{OUT} side of the inductor, and connect the return terminal of the capacitor to the GND pin and exposed PAD of the LM516x.

8.5.3.2 Feedback Resistors

Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the trace length of FB signal and noise coupling. The FB pin is the input to the feedback comparator, and as such, is a high impedance node sensitive to noise. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if a short path is not available.

Route the voltage sense trace from the load to the feedback resistor divider, keeping away from the SW node, the inductor, and V_{IN} to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high feedback resistances greater than 100 kΩ are used to set the output voltage. Also, route the voltage sense trace on a different layer from the inductor, SW node, and V_{IN} so there is a ground plane that separates the feedback trace from the inductor and SW node copper polygon. This provides further shielding for the voltage feedback path from switching noise sources.

8.5.4 Layout Example

図 8-41 shows an example layout using DDA package for the PCB top layer with essential components placed on the top side. 図 8-42 shows an example layout using NGU package for the PCB top layer with essential components placed on the top side.

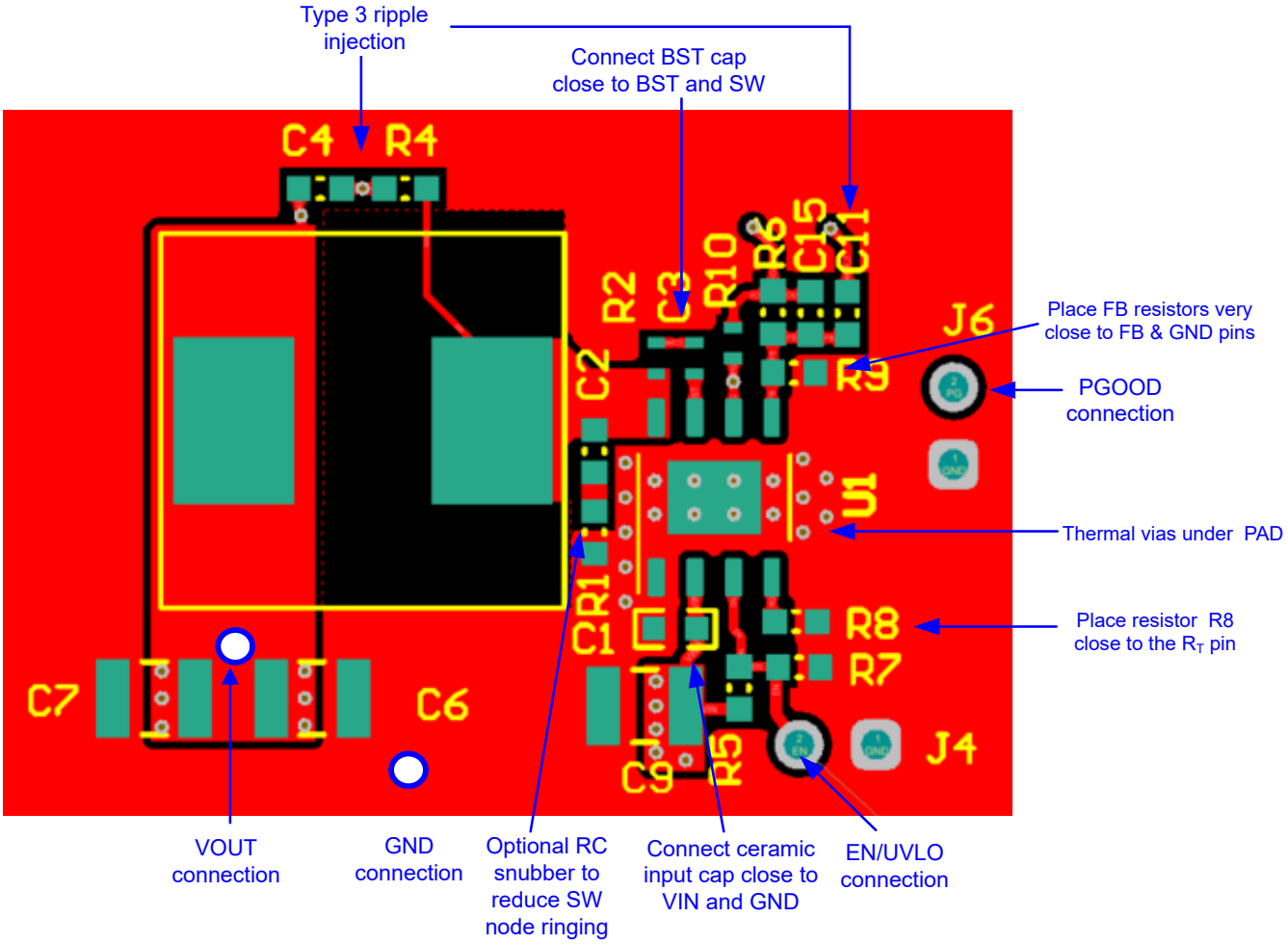


図 8-41. LM516x PCB Layout Example for DDA package

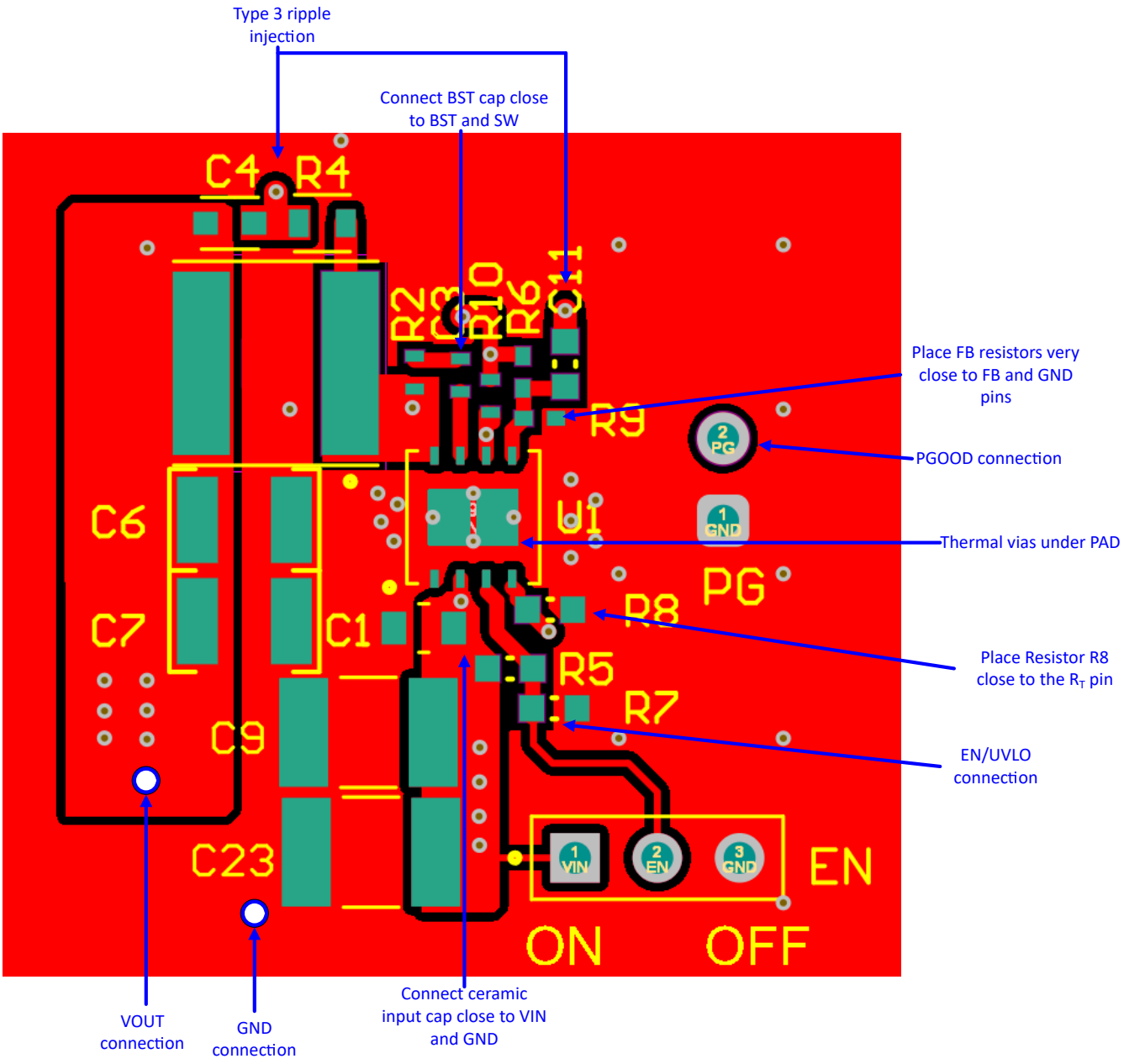


図 8-42. LM516x PCB Layout Example for NGU package

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Stability Analysis of COT Type-III Ripple Circuit application report*
- Texas Instruments, *Designing an Isolated Fly-buck Converter application report*
- Texas Instruments, *Design a Fly-buck Solution with Opto-coupler application report*
- Texas Instruments, *Designing an Isolated Fly-buck Converter Using the LMR36520 application note*
- Texas Instruments, *Selecting an Ideal Ripple Generation Network for Your COT Buck Converter application report*
- Texas Instruments, *Valuing Wide V_{IN}, Low-EMI Synchronous Buck Circuits for Cost-Effective, Demanding Applications white paper*
- Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies white paper*
- Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies white paper*
- Texas Instruments, *24-V AC Power Stage with Wide V_{IN} Converter and Battery Gauge for Smart Thermostat design guide*
- Texas Instruments, *Accurate Gauging and 50-µA Standby Current, 13S, 48-V Li-ion Battery Pack Reference design guide*
- Texas Instruments, *AN-2162: Simple Success with Conducted EMI from DC/DC Converters application report*
- Texas Instruments, *Powering Drones with a Wide V_{IN} DC/DC Converter application report*
- Texas Instruments, *Using New Thermal Metrics application report*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2022) to Revision B (December 2024)	Page
• 「製品情報」表を更新し、新しいパッケージを追加	1
• Added new package and supporting information	4
• Added new package pinout drawing	5
• Deleted "DC" from "SW" in the *Absolute Maximum Ratings* table and added a footnote that links to the *Layout Guidelines* section	6
• Deleted V_{IN} = 4.5V to 120V in the *Electrical Characteristics* table header	6
• Added the new package information	10
• Added the information for NGU package	34
• Added EMI curves for NGU package	37

Changes from Revision * (December 2021) to Revision A (September 2022)	Page
• 文書全体にわたって、すべてのデバイスへの参照を追加	1
• LM5169 からプレビューの注を削除	1
• Added specifications for LM5169 to the *Electrical Characteristics* table	6
• Updated the *Detailed Design Procedure*	19
• Added *Typical Buck Application*	26
• Added *Thermal Considerations* to the *Layout* section	34
• Added derating curves	34
• Added EMI curves	37

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5168FDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	5168F	Samples
LM5168PDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5168P	Samples
LM5169FDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5169F	Samples
LM5169FNGUR	ACTIVE	WSON	NGU	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	5169F NGU	Samples
LM5169PDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5169P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM5168, LM5169 :

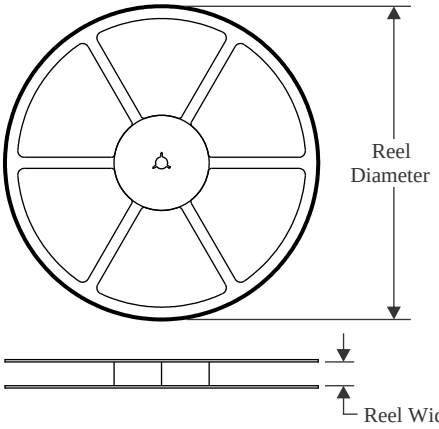
- Automotive : LM5168-Q1, LM5169-Q1

NOTE: Qualified Version Definitions:

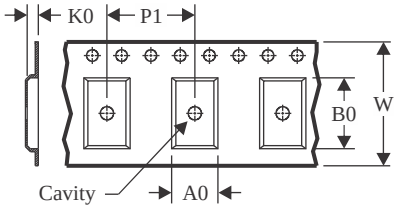
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

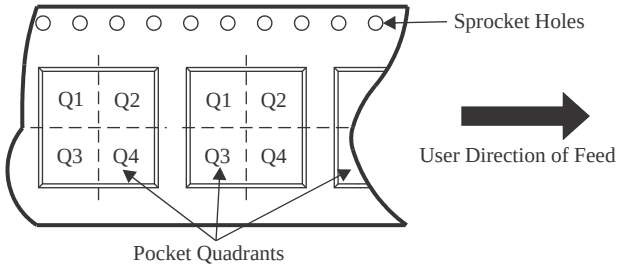


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

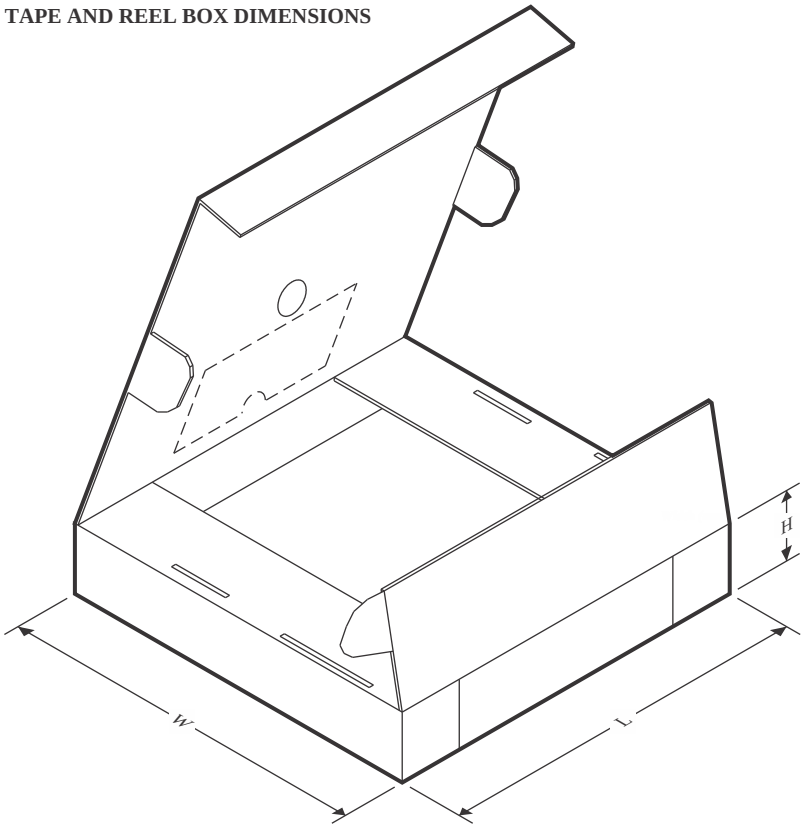
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

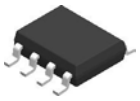
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5168FDDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM5168FDDAR	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM5168PDDAR	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM5169FDDAR	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM5169FNGUR	WSON	NGU	8	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LM5169PDDAR	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5168FDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LM5168FDDAR	SO PowerPAD	DDA	8	2500	340.5	338.1	20.6
LM5168PDDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
LM5169FDDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
LM5169FNGUR	WSON	NGU	8	2500	367.0	367.0	35.0
LM5169PDDAR	SO PowerPAD	DDA	8	2500	340.5	338.1	20.6

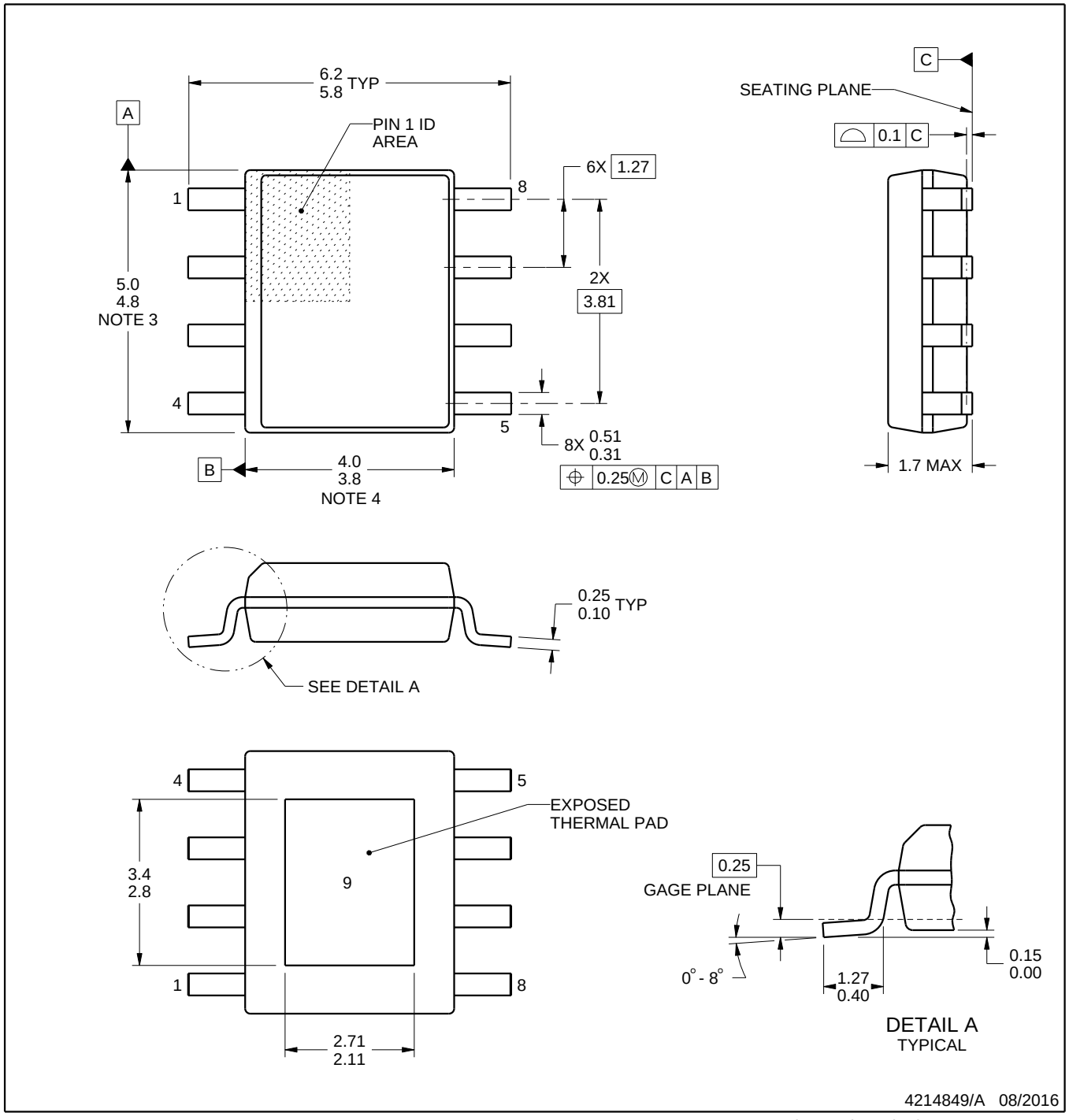


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

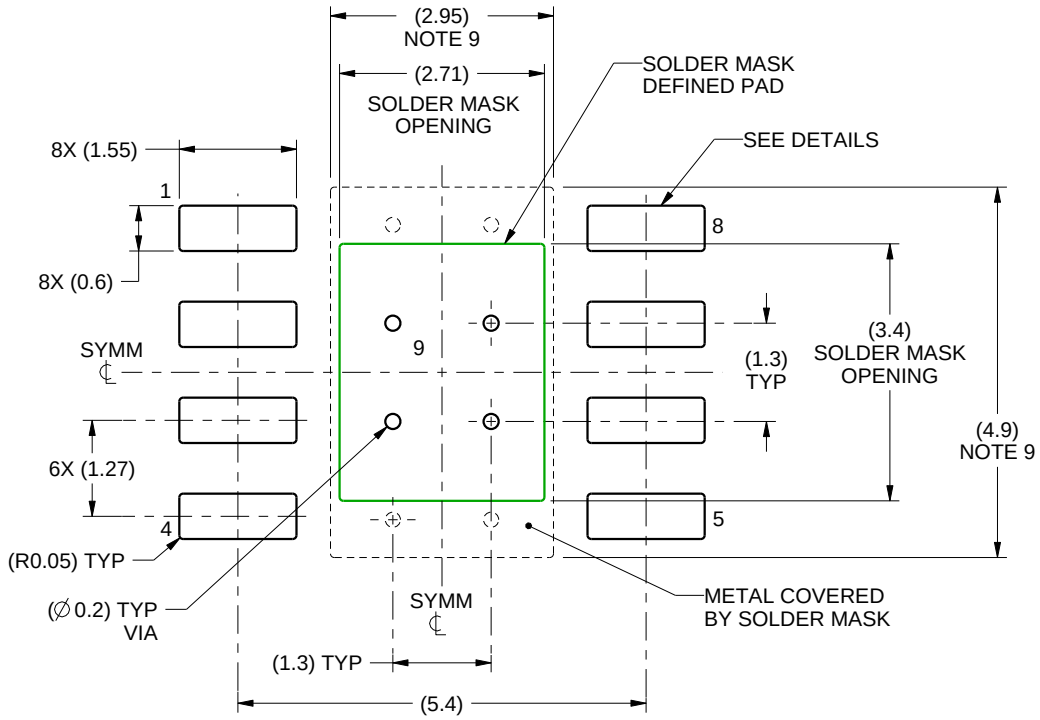
PLASTIC SMALL OUTLINE



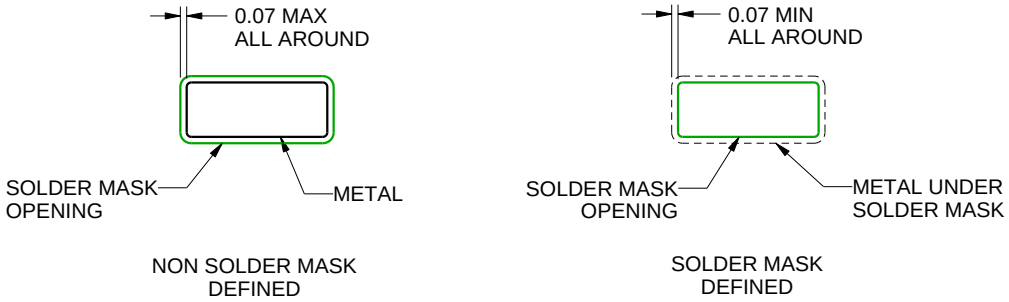
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

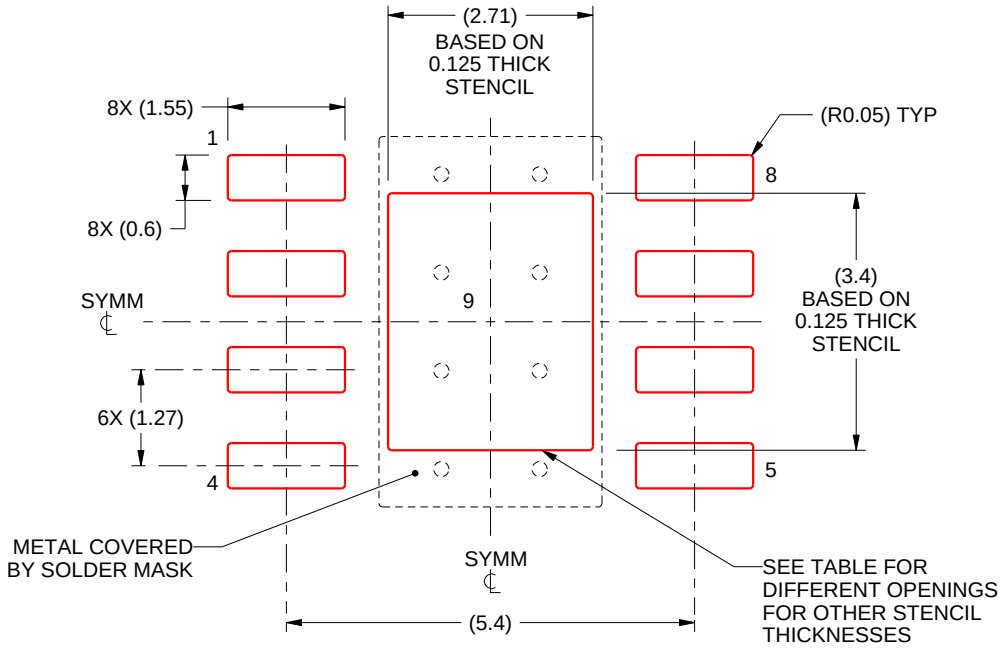
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

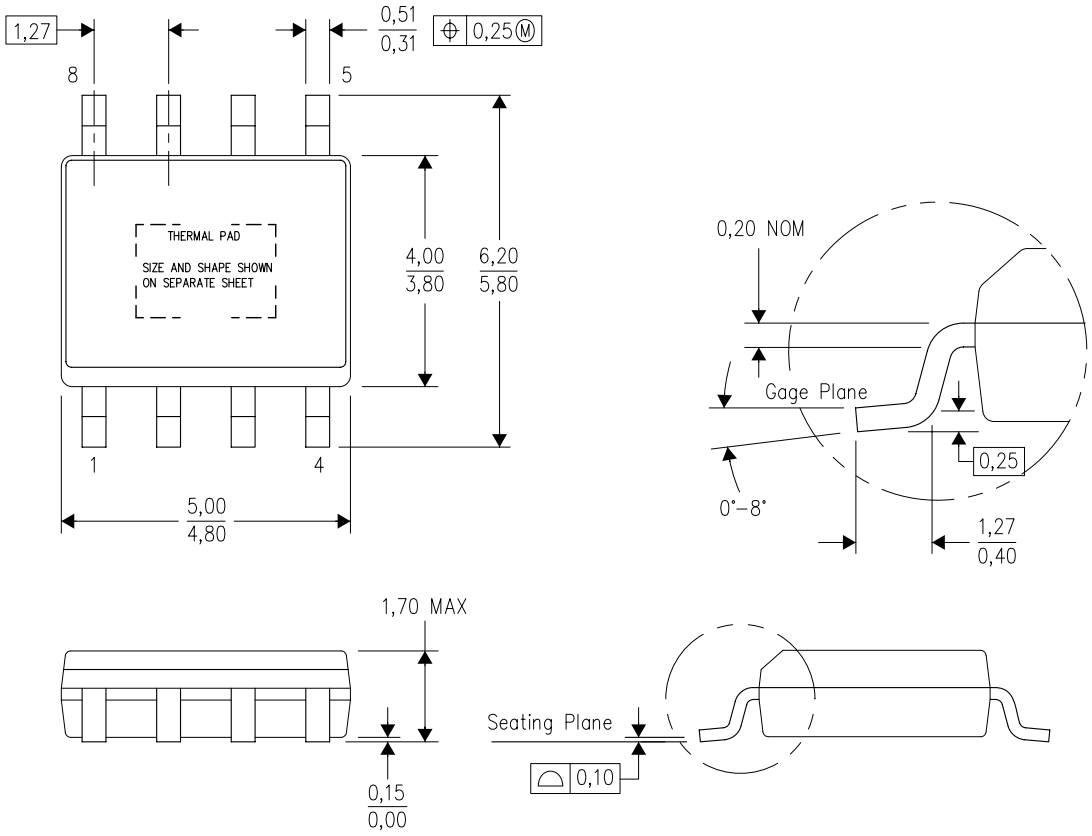
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

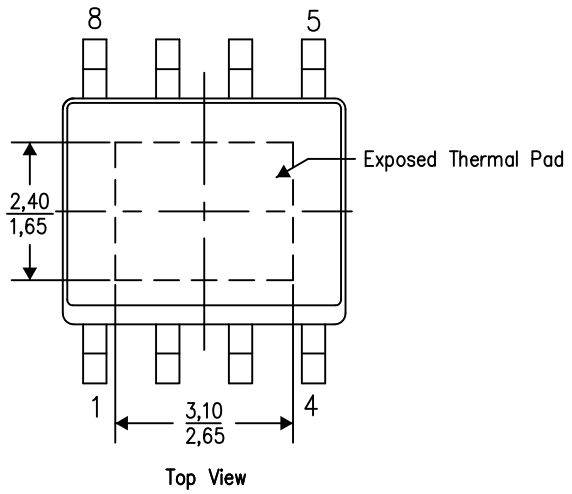
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



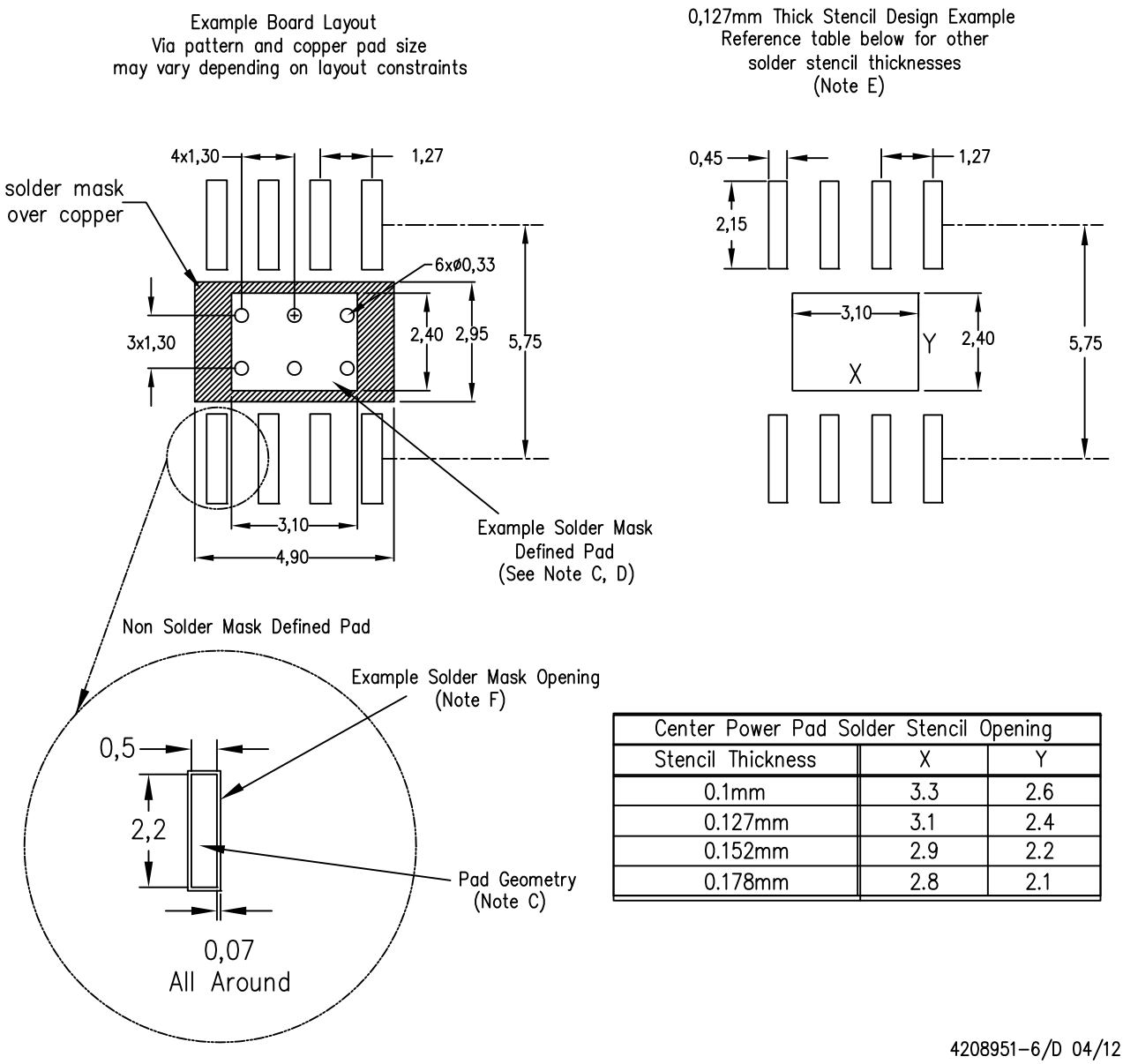
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

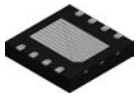


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

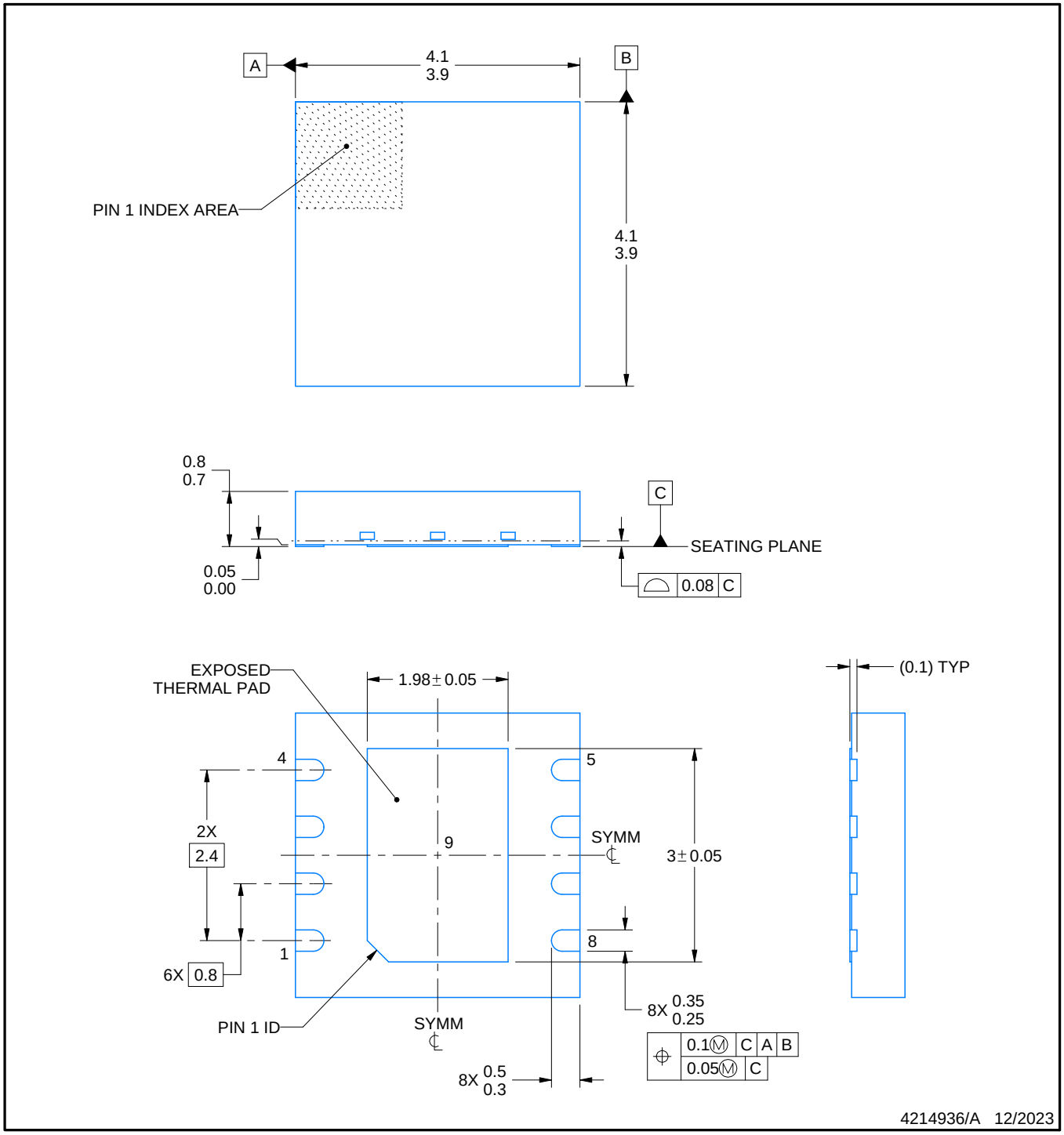
NGU0008B



PACKAGE OUTLINE

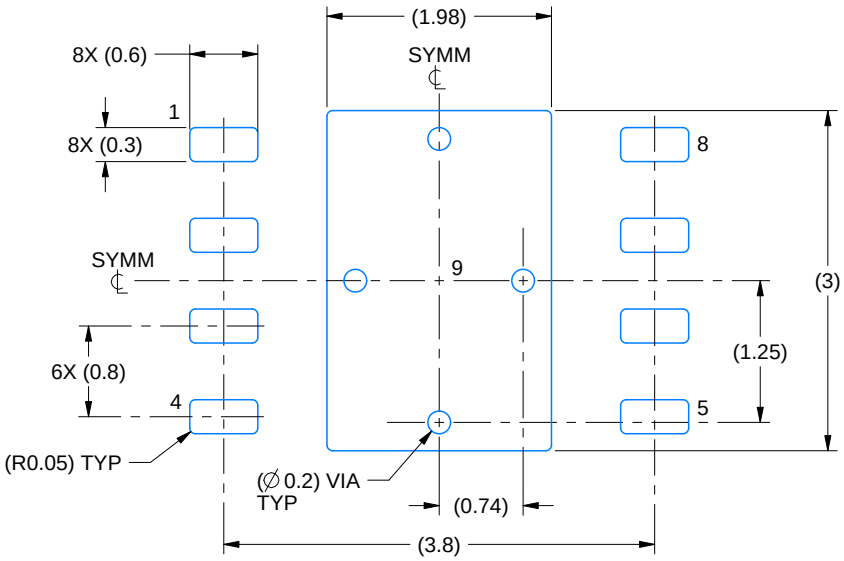
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

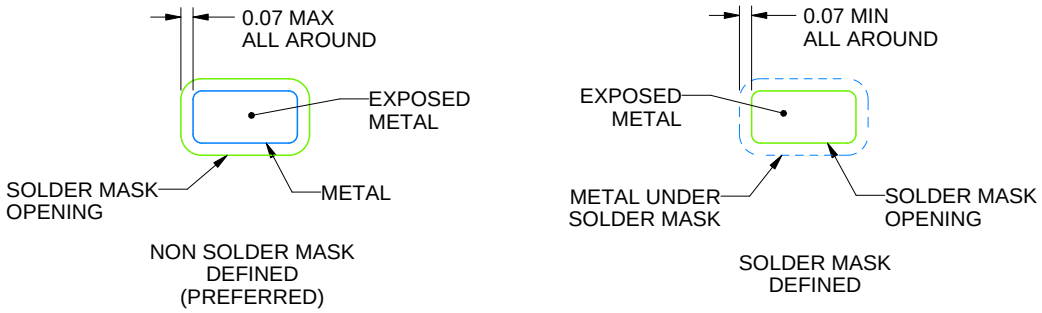


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

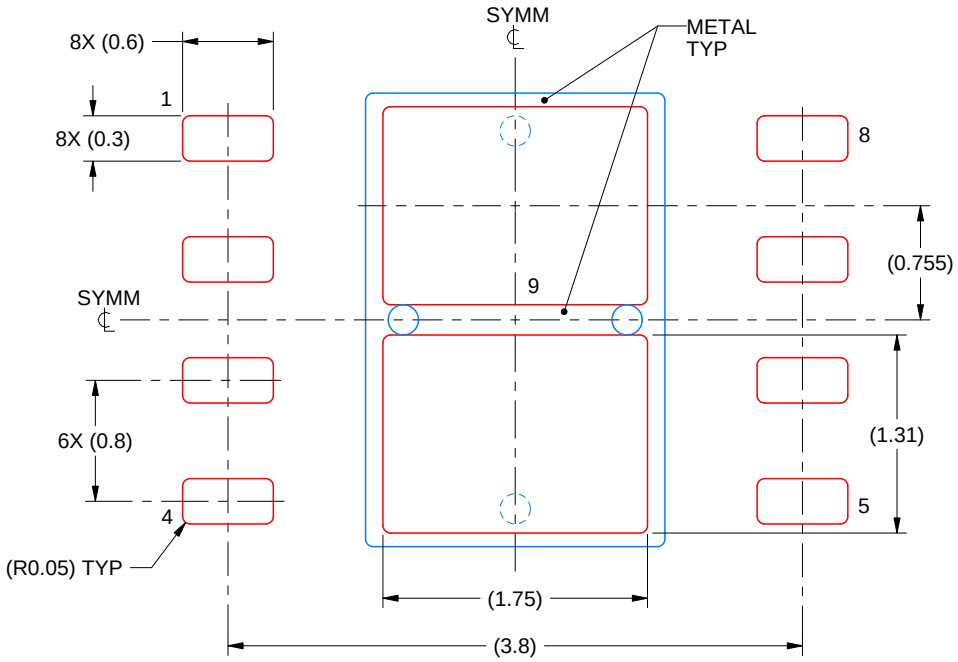


SOLDER MASK DETAILS

4214936/A 12/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214936/A 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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