

LM317L 100mA 可変フローティング電圧レギュレータ

1 特長

- 出力電圧範囲 (V_O):
 - 1.25V~37V の範囲で調整可能 (新しいチップ用)
 - 1.25V~32V の範囲で調整可能 (従来のチップ用)
- 出力電流: 最大 100mA
- 精度:
 - 入力レギュレーションは入力電圧の変化ごとに 0.01% (標準値)
 - 出力レギュレーション: 0.5% (標準値)
- リップル除去の標準値:
 - 120Hz 時に 80dB
 - 100kHz 時に 65dB
- 高出力電流要件については、[LM317M](#) (500mA) および [LM317](#) (1.5A) を参照

2 アプリケーション

- 電子 POS
- 医療、健康、フィットネス アプリケーション
- プリンタ
- 家庭用電気製品および白物家電
- テレビ

3 概要

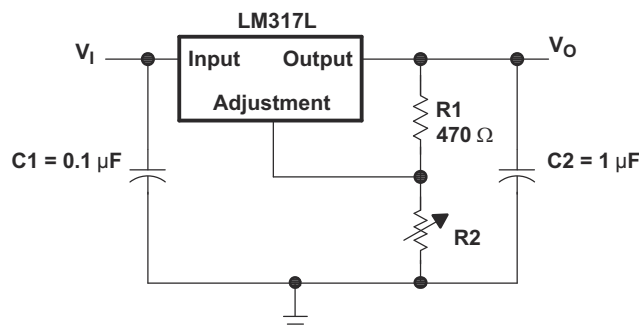
LM317L は、1.25V~37V の出力電圧範囲で最大 100mA を供給できる可変 3 端子正電圧レギュレータです。このデバイスは非常に簡単に使用でき、2 つの外付け抵抗だけで出力電圧を設定できます。

従来のチップの場合、LM317LC シリーズは接合部温度範囲が 0°C~+125°C と規定されており、LM317LI デバイスは動作時接合部温度範囲が -40°C~+125°C と規定されています。新しいチップの場合は、LM317LC および LM317LI シリーズはどちらも接合部温度範囲が -40°C~+125°C と規定されています。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ サイズ ⁽²⁾
LM317L	D (SOIC, 8)	4.9mm × 6mm
	LP (TO-92, 3)	4.8mm × 3.68mm
	PK (SOT-89, 3)	4.5mm × 4.095mm
	PW (TSSOP, 8)	3mm × 6.4mm

- 詳細については、「[メカニカル](#)、[パッケージ](#)、および[注文情報](#)」を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



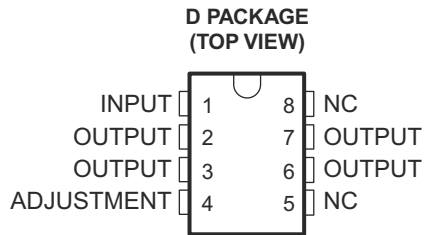
概略回路図



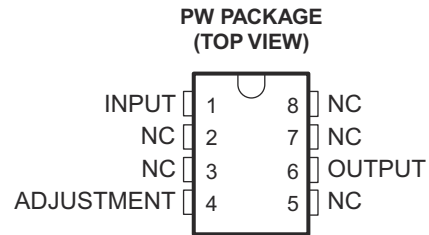
Table of Contents

1 特長	1	7.1 Application Information.....	9
2 アプリケーション	1	7.2 Typical Application.....	9
3 概要	1	7.3 System Examples.....	11
4 Pin Configuration and Functions	3	7.4 Power Supply Recommendations.....	15
5 Specifications	4	7.5 Layout.....	15
5.1 Absolute Maximum Ratings.....	4	7.6 Estimating Junction Temperature.....	15
5.2 ESD Ratings.....	4	8 Device and Documentation Support	17
5.3 Recommended Operating Conditions.....	4	8.1 Device Support.....	17
5.4 Thermal Information.....	4	8.2 ドキュメントの更新通知を受け取る方法.....	17
5.5 Electrical Characteristics.....	5	8.3 サポート・リソース.....	17
5.6 Typical Characteristics.....	6	8.4 Trademarks.....	17
6 Detailed Description	7	8.5 静電気放電に関する注意事項.....	17
6.1 Overview.....	7	8.6 用語集.....	17
6.2 Functional Block Diagram.....	7	9 Revision History	17
6.3 Feature Description.....	8	10 Mechanical, Packaging, and Orderable Information	18
6.4 Device Functional Modes.....	8		
7 Application and Implementation	9		

4 Pin Configuration and Functions



NC – No internal connection
OUTPUT terminals are all internally connected.



NC – No internal connection

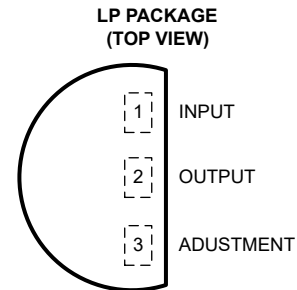
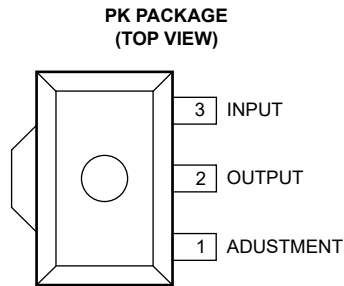


表 4-1. Pin Functions

NAME	D	PW	LP	PK	TYPE ⁽¹⁾	DESCRIPTION
ADJUSTMENT	4	4	3	1	I	Output feedback voltage
INPUT	1	1	1	3	I	Input supply voltage
NC	5, 8	2, 3, 5, 7, 8	—	—	—	No connect. Recommended to ground pins for improved thermal performance but not required.
OUTPUT	2, 3, 6, 7	6	2	2	O	Regulated output voltage

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage	Legacy chip		35	V
		New chip		40	
T_J	Operating virtual-junction temperature			150	°C
T_{stg}	Storage temperature	Legacy chip	-65	150	°C
		New chip	-55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	Legacy chip	±3000	V
			New chip	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾			

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT		
V_O	Output voltage	Legacy chip	1.25	32	V		
		New chip	1.25	37			
$V_I - V_O$	Input-to-output voltage differential	Legacy chip	2.5	32	V		
		New chip	2.5	37			
I_O	Output current		2.5	100	mA		
T_J	Operating virtual-junction temperature	LM317LC	Legacy chip	0	125	°C	
			New chip	-40	125		
		LM317LI	Legacy and new chip		-40		125

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM317L						UNIT	
		D 8 PINS		LP 3 PINS		PK 3 PINS			PW 8 PINS
		Legacy Chip ⁽²⁾	New Chip	Legacy Chip ⁽²⁾	New Chip	Legacy Chip ⁽²⁾	New Chip		Legacy Chip ⁽²⁾
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.1	96.5	139.5	156.7	51.5	44	149.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		48.6		80.6		86.9		
$R_{\theta JB}$	Junction-to-board thermal resistance		34.8				8.5		
Ψ_{JT}	Junction-to-top characterization parameter		5.9		24.7		4.5		
Ψ_{JB}	Junction-to-board characterization parameter		34.2		135.8		8.5		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance						6.9		

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).
 (2) Legacy chip only $R_{\theta JA}$ values reported.

5.5 Electrical Characteristics

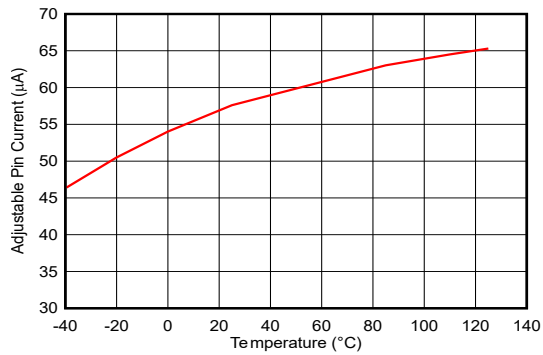
Unless otherwise noted, specifications over recommended operating virtual-junction temperature range, $V_1 - V_O = 5V$ and $I_O = 40mA$, $P \leq$ rated dissipation, measured with a $0.1\mu F$ capacitor across the input and a $1\mu F$ capacitor across the output.

PARAMETER	TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
Line regulation	$V_1 - V_O = 5V$ to $35V$	$T_J = 25^\circ C$	Legacy and new chip	0.01	0.02	%V
		$I_O = 2.5mA$ to $100mA$	Legacy and new chip	0.02	0.05	
Ripple rejection	$V_O = 10V$, $f = 120Hz$		Legacy and new chip	65		dB
	$V_O = 10V$, $10\mu F$ capacitor between ADJUSTMENT and ground		Legacy and new chip	66	80	
Output voltage regulation	$V_1 - V_O = 5V$ to $35V$, $T_J = 25^\circ C$, $I_O = 2.5mA$ to $100mA$	$V_O \leq 5V$	Legacy and new chip	25		mV
		$V_O \geq 5V$	Legacy and new chip	5		mV/V
	$V_1 - V_O = 5V$ to $35V$, $I_O = 2.5mA$ to $100mA$	$V_O \leq 5V$	Legacy and new chip	50		mV
		$V_O \geq 5V$	Legacy and new chip	10		mV/V
Output voltage change with temperature	$T_J = 0^\circ C$ to $125^\circ C$		Legacy and new chip	10		mV/V
Output voltage long-term drift	After 1000 hours at $T_J = 125^\circ C$ and $V_1 - V_O = 35V$		Legacy and new chip	3	10	mV/V
Output noise voltage	$f = 10Hz$ to $10kHz$, $T_J = 25^\circ C$		Legacy and new chip	30		$\mu V/V$
Minimum output current to maintain regulation	$V_1 - V_O = 35V$		Legacy chip	1.5	2.5	mA
			New chip	3.5	5	
Peak output current	$3V \leq V_1 - V_O \leq 13V$		Legacy and new chip	100	200	mA
	$V_1 - V_O = 35V$		Legacy chip	100	200	
			New chip	25	50	
ADJUSTMENT current			Legacy and new chip	50	100	μA
Change in ADJUSTMENT current	$V_1 - V_O = 5V$, $I_O = 40mA$		Legacy and new chip	0.2	5	μA
Reference voltage (output to ADJUSTMENT)	$V_1 - V_O = 5V$, $I_O = 40mA$			1.2	1.25	1.3

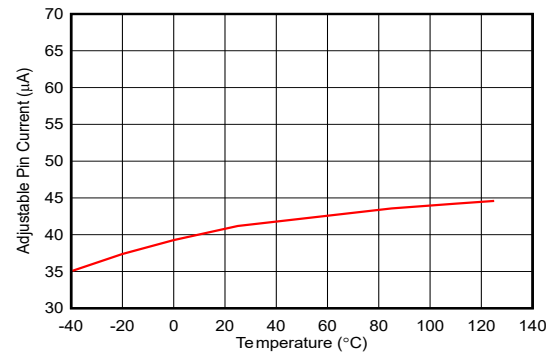
(1) For all tests unless otherwise noted, power dissipation $\leq 1.4W$ in PK, D, and PW packages and $\leq 0.625W$ for LP package. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

5.6 Typical Characteristics

Unless otherwise noted, specifications over recommended operating virtual-junction temperature range, $V_I - V_O = 5V$ and $I_O = 40mA$, $P \leq$ rated dissipation.



5-1. Change in Adjustment Current Over Temperature (Legacy Chip)



5-2. Change in Adjustment Current Over Temperature (New Chip)

6 Detailed Description

6.1 Overview

The LM317L is a 100mA linear regulator with high voltage tolerance up to 37V. The device has a feedback voltage that is relative to the output instead of ground. This ungrounded design allows the LM317L device to have superior line and load regulation. This design also allows the LM317L device to be used as a current source or current sink using a single resistor. Any output voltage from 1.25V to 32V can be obtained by using two resistors. The bias current of the device, up to 2.5mA, flows to the output; this current must be used by the load or the feedback resistors. The power dissipation is the product of pass transistor voltage and current, which is calculated as shown in 式 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

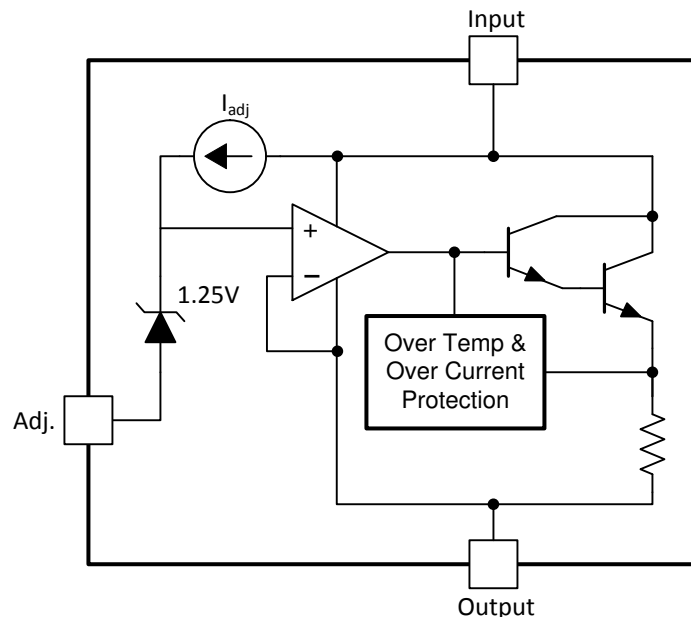
The application heat sink must be able to absorb the power calculated in 式 1.

In addition to higher performance than fixed regulators, this regulator offers full overload protection, available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional even when ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard three-terminal regulators.

In addition to replacing fixed regulators, the LM317L regulator is useful in a wide variety of other applications. Because the regulator is floating and observes only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. The primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.25V, where most loads draw little current.

The LM317LC is characterized for operation over the virtual junction temperature range of 0°C to 125°C. The LM317LI is characterized for operation over the virtual junction temperature range of -40°C to 125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 NPN Darlington Output Drive

The NPN Darlington output topology provides naturally low output impedance and an output capacitor is optional. To support maximum current and lowest temperature, a 2.5V headroom is recommended ($V_I - V_O$).

6.3.2 Overload Block

Overcurrent and overtemperature shutdown protects the device against overload or damage from operating in excessive heat.

6.3.3 Programmable Feedback

An op amp with a 1.25V offset input at the ADJUST pin provides easy output voltage or current (not both) programming. For current regulation applications, use a single resistor whose resistance value is $1.25V / I_{OUT}$ and power rating is greater than $(1.25V)^2 / R$. For voltage regulation applications, two resistors set the output voltage. See the [Typical Application](#) section for a schematic and the resistor formula.

6.4 Device Functional Modes

6.4.1 Normal operation

The device OUTPUT pin sources current necessary to make the OUTPUT pin 1.25V greater than the ADJUST terminal to provide output regulation.

6.4.2 Operation With Low Input Voltage

The device requires up to a 2.5V headroom ($V_I - V_O$) to operate in regulation. With less headroom, the device can drop out and the OUTPUT voltage is the INPUT voltage minus the dropout voltage.

6.4.3 Operation at Light Loads

The device passes the bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output can be too high.

6.4.4 Operation In Self Protection

When an overload occurs, the device shuts down the Darlington NPN output stage or reduces the output current to prevent device damage. The device automatically restarts when the over current is removed. The output can be reduced or cycle thermal shutdown on and off until the overload is removed.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The two output resistors are the only components required to adjust V_{OUT} .

7.2 Typical Application

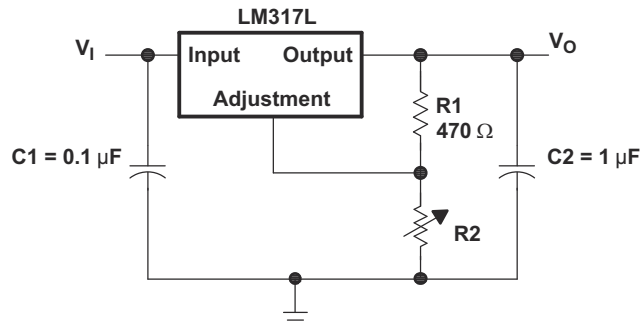


図 7-1. Typical Application Schematic

7.2.1 Design Requirements

1. Use an input bypass capacitor if the regulator is far from the filter capacitors.
2. For this design example, use the parameters listed in 表 7-1.
3. Using an output capacitor improves transient response, but is optional.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	(Output voltage + 2.5V) to 32V
Output voltage	$V_{REF} \times (1 + R_2 / R_1) + I_{ADJ} \times R_2$

7.2.2 Detailed Design Procedure

7.2.2.1 Input Capacitor

An input capacitor is not required, but is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1µF ceramic or 1µF tantalum provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.

7.2.2.2 Output Capacitor

An output capacitor improves transient response, but is not needed for stability.

7.2.2.3 Feedback Resistors

The feedback resistor sets the output voltage using 式 2.

$$V_{REF} \times (1 + R_2 / R_1) + I_{ADJ} \times R_2 \quad (2)$$

7.2.2.4 Adjustment Terminal Capacitor

The optional adjustment pin capacitor improves ripple rejection by preventing the amplification of the ripple. When this capacitor is used and $V_{OUT} > 6V$, a protection diode from adjust to output is recommended.

7.2.2.5 Design Options and Parameters

Common linear regulator designs are concerned with the following parameters:

- Input voltage range
- Input capacitor range
- Output voltage
- Output current rating
- Output capacitor range
- Input short protection
- Stability
- Ripple rejection

7.2.2.6 Output Voltage

V_O is calculated as shown in 式 3.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1} \right) + (I_{ADJ} \times R_2) \quad (3)$$

Because I_{ADJ} typically is $50\mu A$, this parameter is negligible in most applications.

7.2.2.7 Ripple Rejection

C_{ADJ} is used to improve ripple rejection. This capacitor prevents amplification of the ripple when the output voltage is adjusted higher. If C_{ADJ} is used, include protection diodes to prevent ADJ from reverse-biasing when V_{OUT} collapses quickly.

7.2.2.8 Input Short Protection

If the input is shorted to ground during a fault condition, protection diodes provide measures to prevent the possibility of external capacitors discharging through low-impedance paths in the device. By providing low-impedance discharge paths for C_3 and C_2 , respectively, a protection diode across the input to the output and a protection diode across ADJ to the output prevent the capacitors from discharging into the output of the regulator.

7.2.3 Application Curve

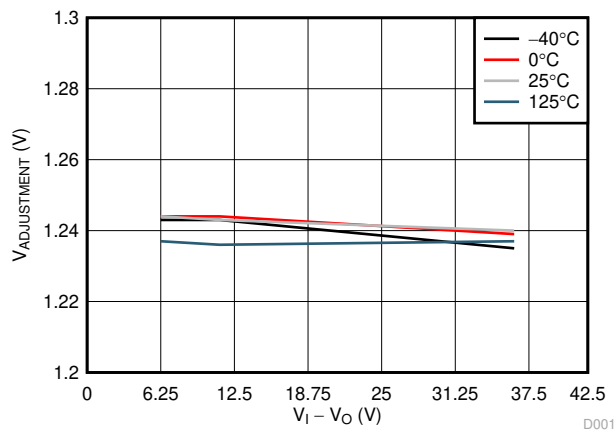


图 7-2. Adjustment Voltage Relative to Output Over Temperature (Legacy Chip)

7.3 System Examples

7.3.1 Regulator Circuit With Improved Ripple Rejection

C2 helps stabilize the voltage at the adjustment pin, which helps reject noise. Diode D1 exists to discharge C2 in case the output is shorted to ground.

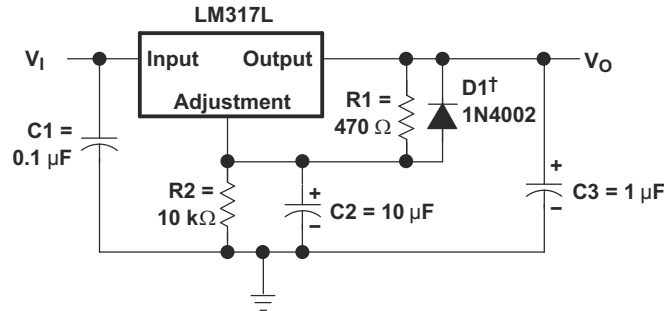


図 7-3. Regulator Circuit With Improved Ripple Rejection

7.3.2 0V to 30V Regulator Circuit

In the 0V to 30V regulator circuit application, the output voltage is determined by 式 4.

$$V_{OUT} = V_{REF} \left(1 + \frac{R_2 + R_3}{R_1} \right) - 10 \text{ V} \quad (4)$$

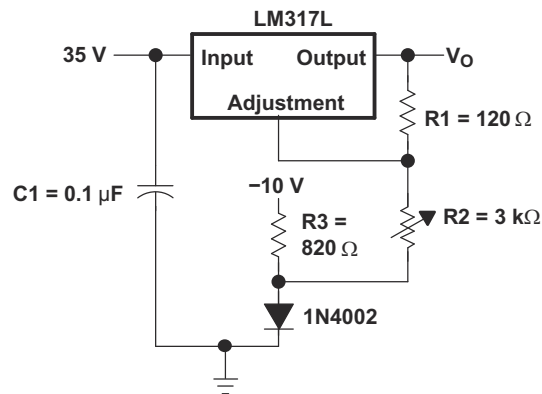


図 7-4. 0V to 30V Regulator Circuit

7.3.3 Precision Current-Limiter Circuit

This application limits the output current to the I_{LIMIT} shown in 図 7-5.

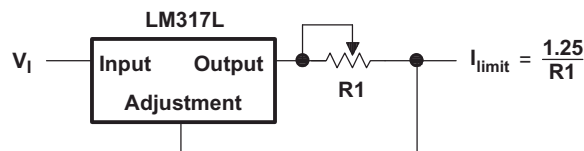


図 7-5. Precision Current-Limiter Circuit

7.3.4 Tracking Preregulator Circuit

The tracking preregulator circuit application keeps a constant voltage across the second LM317L in the circuit.

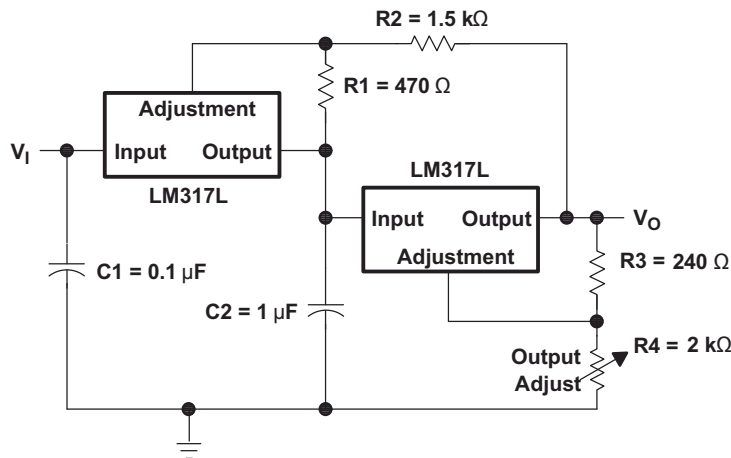


图 7-6. Tracking Preregulator Circuit

7.3.5 Slow-Turn On 15V Regulator Circuit

The capacitor C1, in combination with the PNP transistor, helps the circuit to slowly start supplying voltage. In the beginning, the capacitor is not charged. Therefore, output voltage starts at 1.9V, as determined by 式 5. As the capacitor voltage rises, V_{OUT} rises at the same rate. When the output voltage reaches the value determined by R1 and R2, the PNP is turned off.

$$V_{C1} + V_{BE} + 1.25V = 0V + 0.65V + 1.25V = 1.9V \tag{5}$$

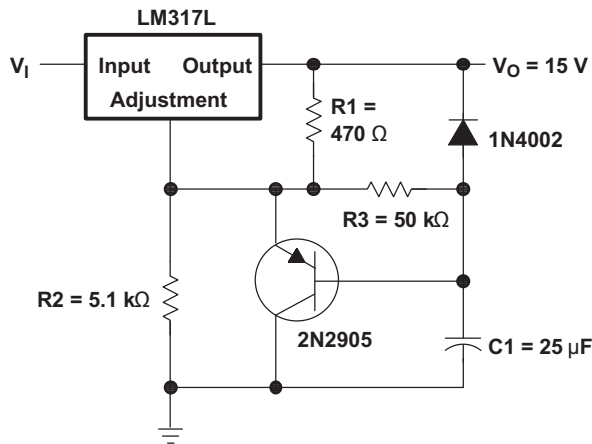


图 7-7. Slow-Turn On of the 15V Regulator Circuit

7.3.6 50mA Constant-Current, Battery-Charger Circuit

The current-limit operation mode can be used to trickle charge a battery at a fixed current as determined by 式 6. V_I must be greater than $V_{BAT} + 3.75V$.

$$I_{CHG} = 1.25V \div 24\Omega \quad (6)$$

$$(1.25V [V_{REF}] + 2.5V [\text{headroom}]) \quad (7)$$

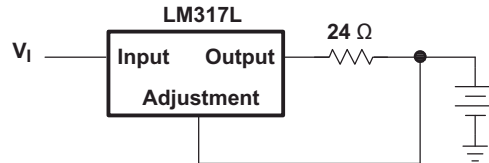


図 7-8. 50mA Constant-Current, Battery-Charger Circuit

7.3.7 Current-Limited 6V Charger

As the charge current increases, the voltage at the bottom resistor increases until the NPN starts sinking current from the adjustment pin. The voltage at the adjustment pin drops, and consequently the output voltage decreases until the NPN stops conducting.

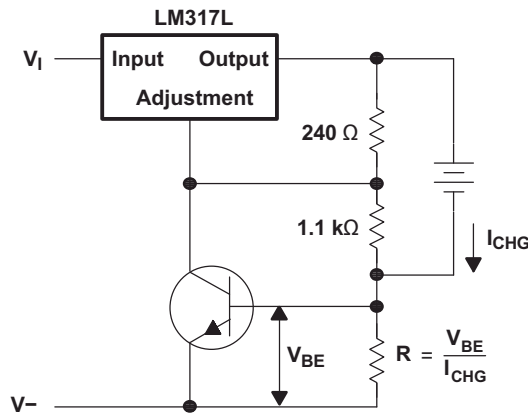
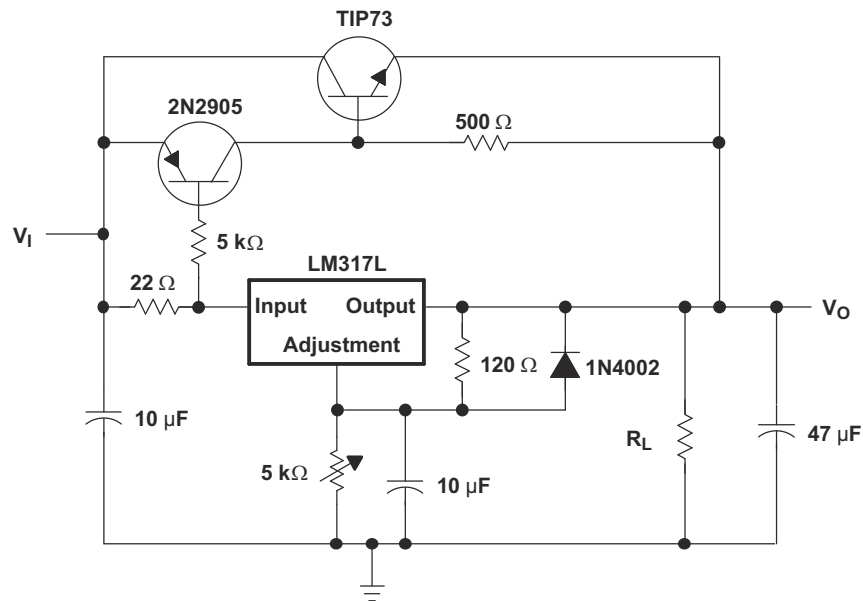


図 7-9. Current-Limited 6V Charger

7.3.8 High-Current Adjustable Regulator

This application allows higher currents at V_{OUT} than the LM317L can provide, while still keeping the output voltage at levels determined by the adjustment-pin resistor divider of the LM317L.



7-10. High-Current Adjustable Regulator

7.4 Power Supply Recommendations

The LM317L is designed to operate from an input voltage supply range between 2.5V to 32V greater than the output voltage. If the device is more than six inches from the input filter capacitors, an input bypass capacitor, 0.1µF or greater, of any type is needed for stability.

7.5 Layout

7.5.1 Layout Guidelines

- Bypass the input pin to ground with a bypass capacitor.
- The optimum placement is closest to the V_{IN} of the device and the GND of the system. Care must be taken to minimize the loop area formed by the bypass capacitor connection, the INPUT pin, and the GND pin of the system.
- For operation at a full-rated load, use wide trace lengths to eliminate IR drop and heat dissipation.

7.5.2 Layout Example

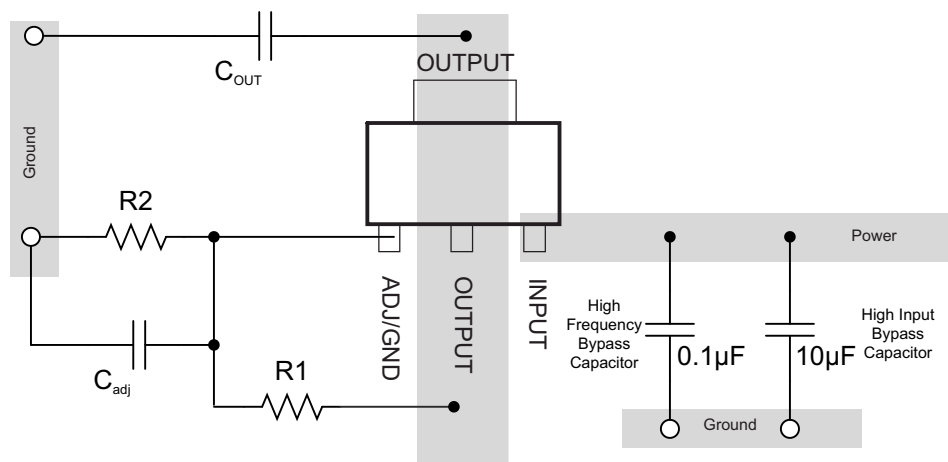


図 7-11. Layout Diagram

7.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The [セクション 5.4](#) table lists the primary thermal metrics, which are the junction-to-top characterization parameter (Ψ_{JT}) and junction-to-board characterization parameter (Ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (Ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (Ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D \quad (8)$$

$$T_J = T_B + \Psi_{JB} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Device Nomenclature

PRODUCT ⁽¹⁾	V _{OUT}
LM317Lxyyyz	<p>x is the operating temperature range designator. yyy is the package designator. z is the package quantity designator. Devices ship with either the legacy chip (CSO: SHE) or the new chip (CSO: TID). The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the data sheet.</p>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの [使用条件](#) を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
 すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (October 2014) to Revision F (December 2024)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
ドキュメント全体を通して、従来のチップと新しいチップの情報を識別するための用語を追加.....	1
Updated <i>Pin Functions</i> table to include correct pin information.....	3
Added $3V \leq V_I - V_O \leq 15V$ rows to <i>Peak output current parameter</i> in <i>Electrical Characteristics</i> table.....	5
Deleted second footnote from <i>Electrical Characteristics</i> table.....	5

- Added *Device Support* section..... 17

Changes from Revision D (October 2011) to Revision E (October 2014)

Page

- 「製品情報」表、「端子機能」表、「取り扱い定格」表、「熱に関する情報」表、「代表的特性」セクション、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- 「注文情報」表を削除。 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM317LCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	L317LC	Samples
LM317LCLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	L317LC	Samples
LM317LCLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	L317LC	Samples
LM317LCPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	LA	Samples
LM317LCPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	LA	Samples
LM317LCPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCPWE4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LCPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC	Samples
LM317LID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples
LM317LIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples
LM317LIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples
LM317LILP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	L317LI	Samples
LM317LILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	L317LI	Samples
LM317LIPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LB	Samples
LM317LIPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LB	Samples
LM317LIPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM317LIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM317LCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LCDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
LM317LCPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM317LIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
LM317LIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM317LCDR	SOIC	D	8	2500	340.5	338.1	20.6
LM317LCDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM317LCPK	SOT-89	PK	3	1000	340.0	340.0	38.0
LM317LCPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM317LIDR	SOIC	D	8	2500	353.0	353.0	32.0
LM317LIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
LM317LIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
LM317LIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

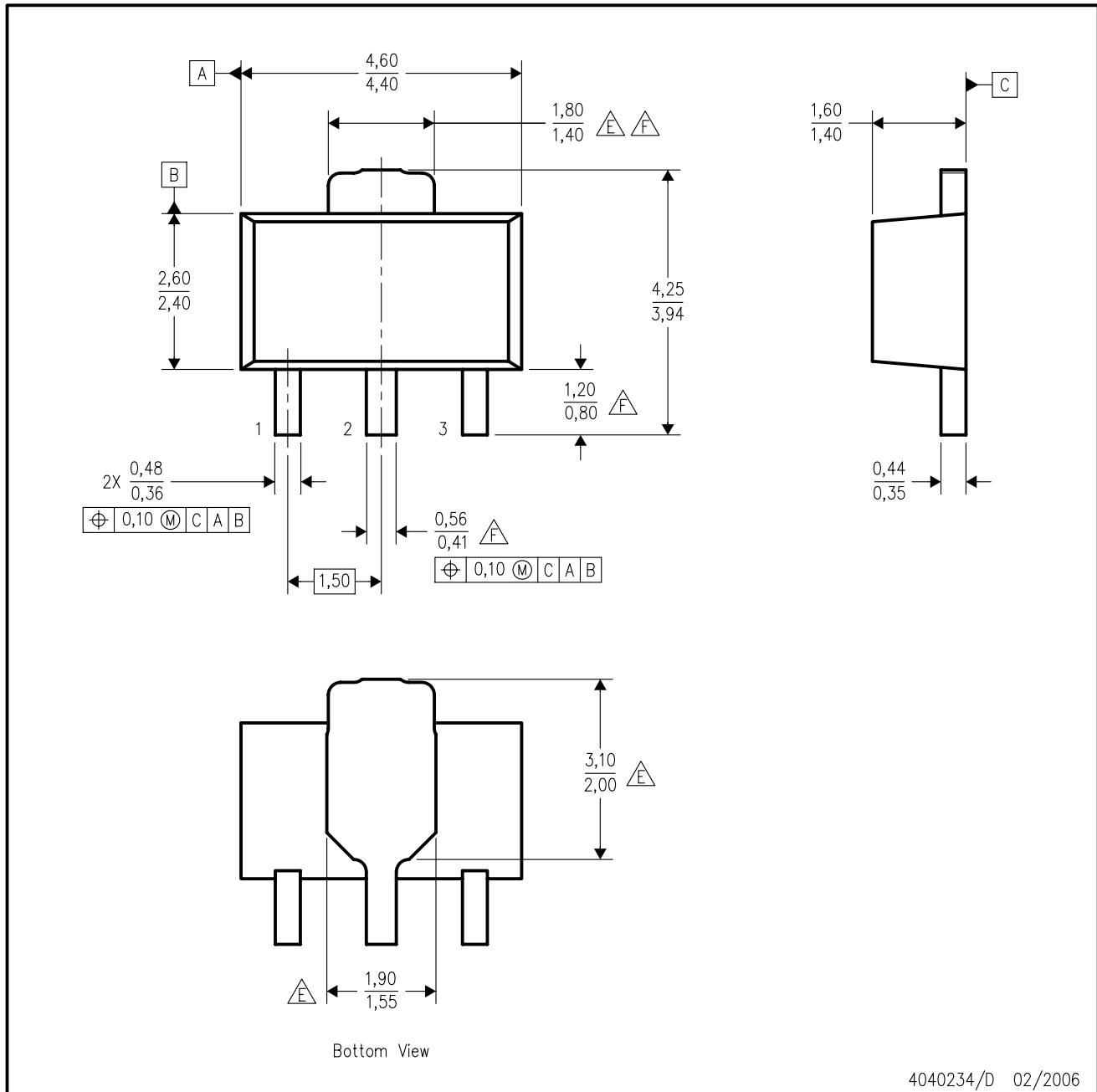
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM317LCD	D	SOIC	8	75	507	8	3940	4.32
LM317LCPW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM317LCPWE4	PW	TSSOP	8	150	530	10.2	3600	3.5
LM317LID	D	SOIC	8	75	507	8	3940	4.32
LM317LIPW	PW	TSSOP	8	150	530	10.2	3600	3.5

PK (R-PSS0-F3)

PLASTIC SINGLE-IN-LINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - The center lead is in electrical contact with the tab.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
- △E Thermal pad contour optional within these dimensions.
- △F Falls within JEDEC TO-243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R-PDSO-G3)



4208221/A 09/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3

TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040001-2/F

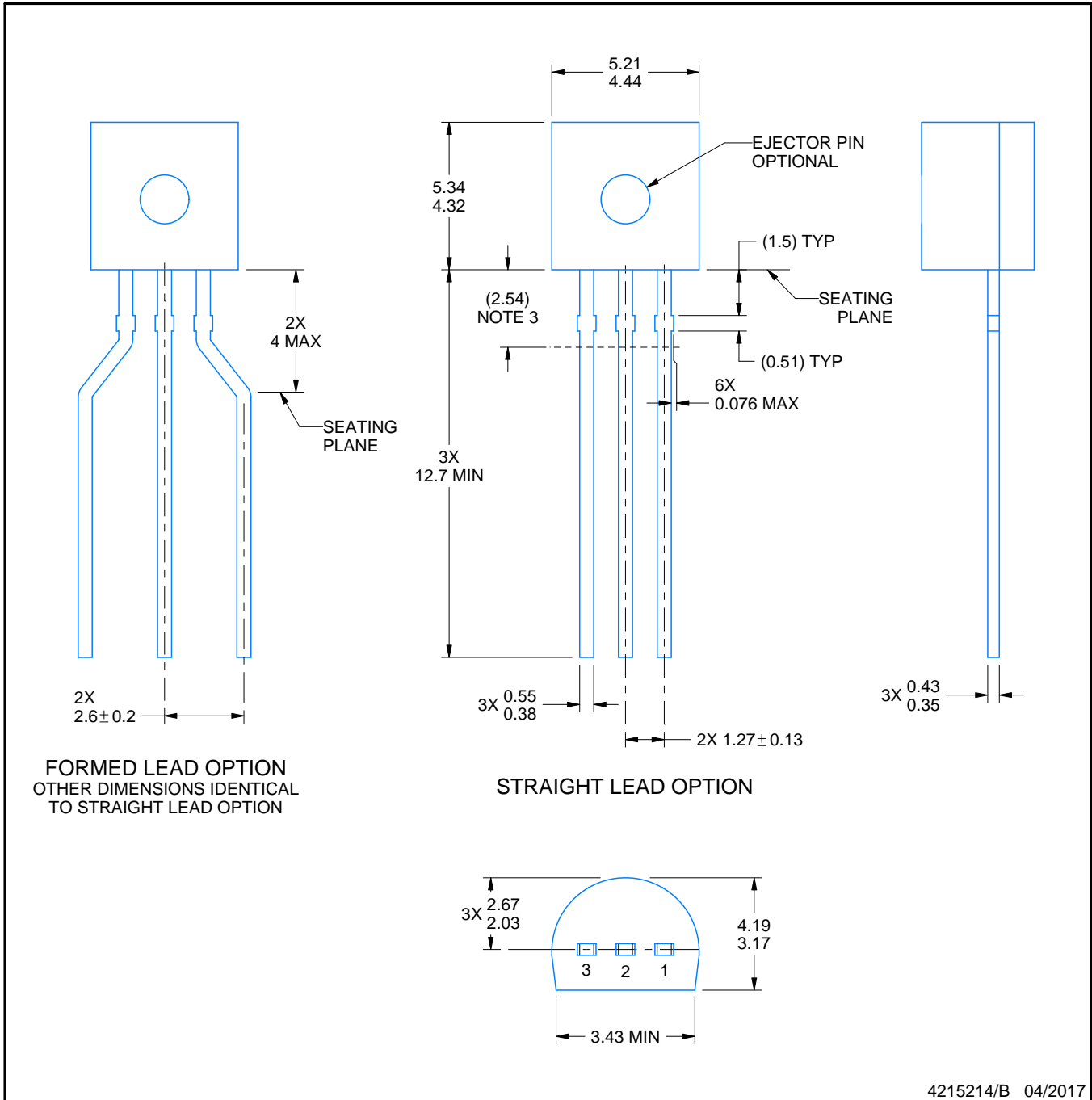
LP0003A



PACKAGE OUTLINE

TO-92 - 5.34 mm max height

TO-92



4215214/B 04/2017

NOTES:

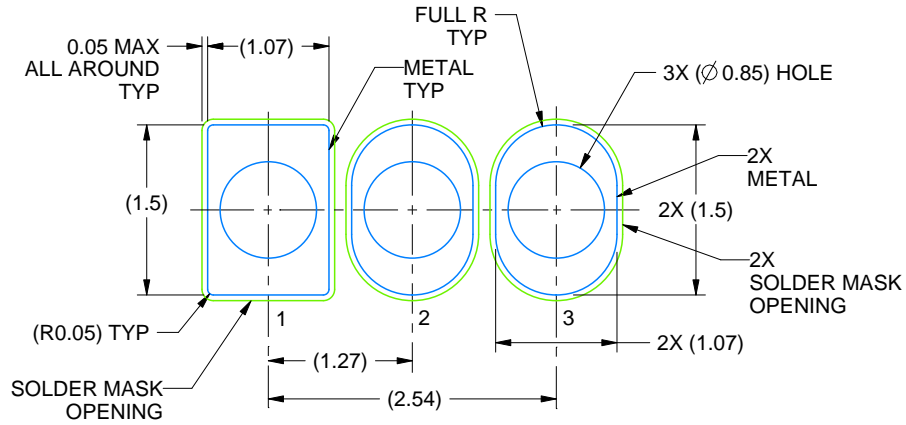
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
 - a. Straight lead option available in bulk pack only.
 - b. Formed lead option available in tape and reel or ammo pack.
 - c. Specific products can be offered in limited combinations of shipping medium and lead options.
 - d. Consult product folder for more information on available options.

EXAMPLE BOARD LAYOUT

LP0003A

TO-92 - 5.34 mm max height

TO-92



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

TAPE SPECIFICATIONS

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、ます。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated