LM2776 Switched Capacitor Inverter

1 Features

- Input Voltage: 2.7 V to 5.5 V
- 200-mA Output Current
- Inverts Input Supply Voltage
- Low-Current PFM Mode Operation
- 2-MHz Switching Frequency
- Greater than 90% Efficiency
- Current Limit and Thermal Protection
- No Inductors

2 Applications

- Operational Amplifier Power Supplies
- Interface Power Supplies
- Data Converter Supplies
- Audio Amplifier Power Supplies
- Portable Electronic Devices

3 Description

The LM2776 CMOS charge-pump voltage converter inverts a positive voltage in the range from 2.7 V to 5.5 V to the corresponding negative voltage. The LM2776 uses three low-cost capacitors to provide 200 mA of output current without the cost, size, and electromagnetic interference (EMI) related to inductor-based converters.

With an operating current of only 100 µA and operating efficiency greater than 90% at most loads, the LM2776 provides ideal performance for battery-powered systems requiring a high power negative power supply.

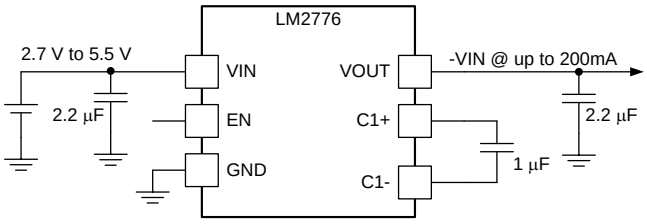
The LM2776 has been placed in TI's 6-pin SOT-23 to maintain a small form factor.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2776	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Output Impedance vs Input Voltage
I_{OUT} = 100 mA

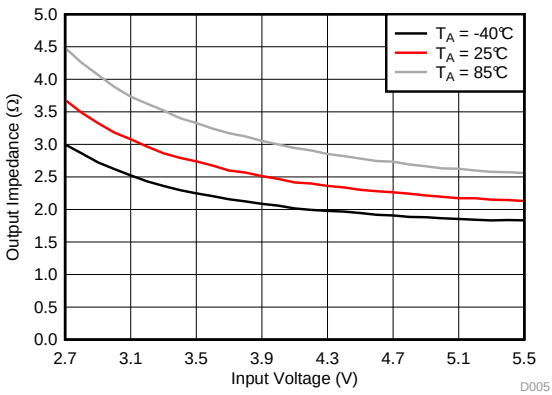


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2016) to Revision B **Page**

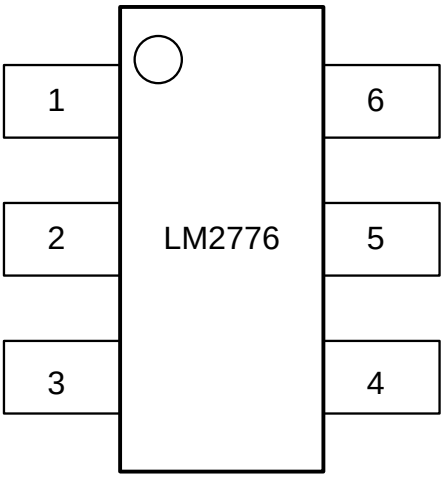
- Added link for TIDA-01063 reference design ... 1

Changes from Original (May 2015) to Revision A **Page**

- Changed Equation 1 from "$R_{OUT} = R_{SW}$..." to "$R_{OUT} = (2 \times R_{SW})$..." ... 12

5 Pin Configuration and Functions

DBV Package
6-Pin SOT
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	VOUT	Output/Power	Negative voltage output.
2	GND	Ground	Power supply ground input.
3	VIN	Input/Power	Power supply positive voltage input.
4	EN	Input	Enable control pin, tie this pin high (EN = 1) for normal operation, and to GND (EN = 0) for shutdown.
5	C1+	Power	Connect this pin to the positive terminal of the charge-pump capacitor.
6	C1-	Power	Connect this pin to the negative terminal of the charge-pump capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltage (VIN to GND, or GND to VOUT)		6	V
EN	(GND − 0.3)	(V_{IN} + 0.3)	V
VOUT continuous output current		250	mA
Operating junction temperature, T_{JMax}(3)		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A) / R_{\theta JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the specified package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Junction temperature	–40		125	°C
Ambient temperature	–40		85	°C
Input voltage	2.7		5.5	V
Output current	0		200	mA

6.4 Thermal Information

THERMAL METRIC(1)		LM2776 DBV (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	158.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical limits tested at T_A = 25°C. Minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). V_{IN} = 3.6 V, C_{IN} = C_{OUT} = 2.2 µF, C_1 = 1 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Supply current	EN = 1. No load		100	200	µA
I_{SD}	Shutdown supply current	EN = 0		0.1	1	µA
V_{EN}	Enable pin input threshold voltage	Normal operation	1.2			V
		Shutdown mode			0.4	
R_{OUT}	Output resistance			2.5		Ω
I_{CL}	Output current limit			400		mA
UVLO	Undervoltage lockout	V_{IN} Falling		2.4		V
		V_{IN} Rising		2.6		

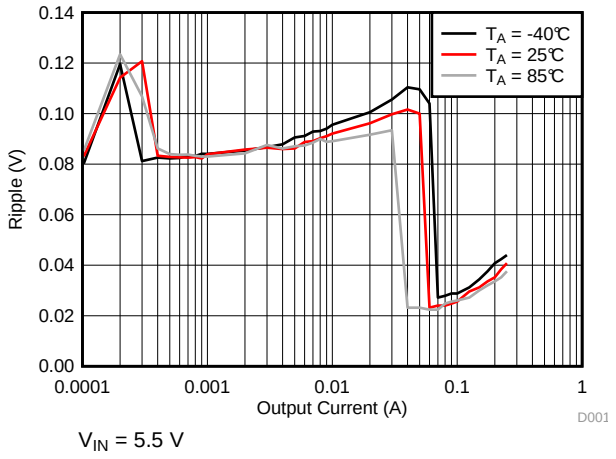
6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency		1.7	2	2.3	MHz

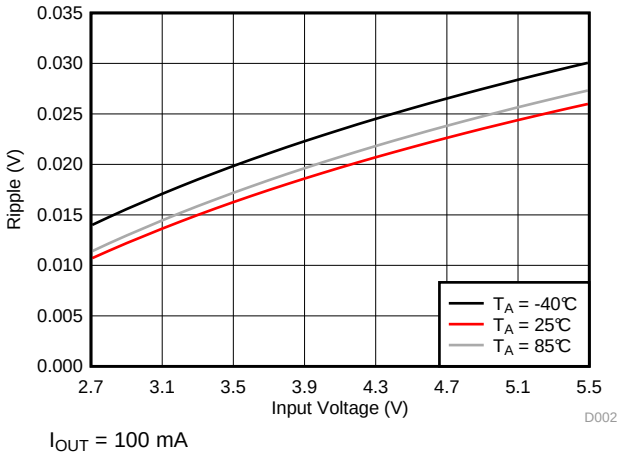
6.7 Typical Characteristics

(*Typical Application* circuit, V_{IN} = 3.6 V unless otherwise specified.)



V_{IN} = 5.5 V

Figure 1. Output Ripple vs Output Current



I_{OUT} = 100 mA

Figure 2. Output Ripple vs Input Voltage

Typical Characteristics (continued)

(*Typical Application* circuit, V_{IN} = 3.6 V unless otherwise specified.)

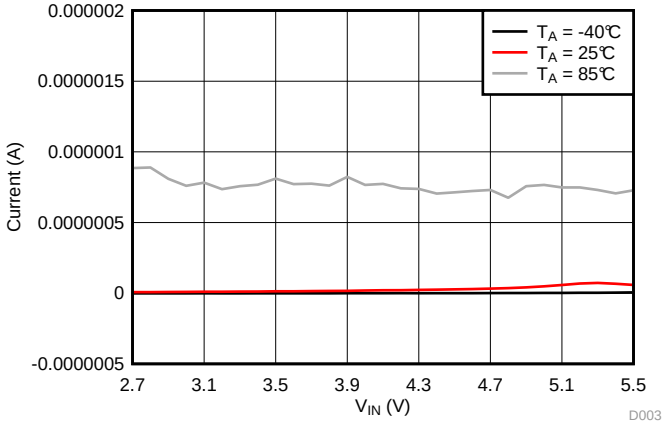
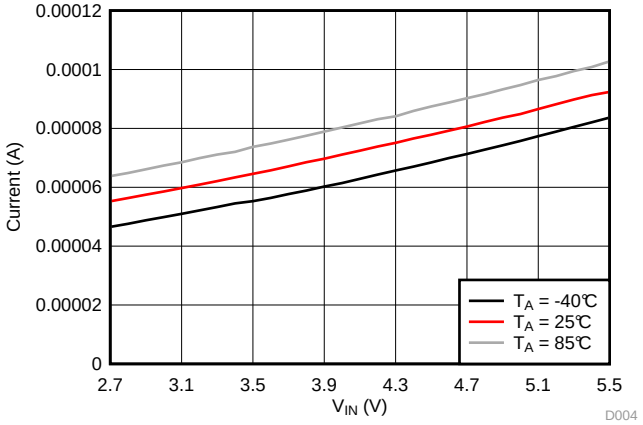
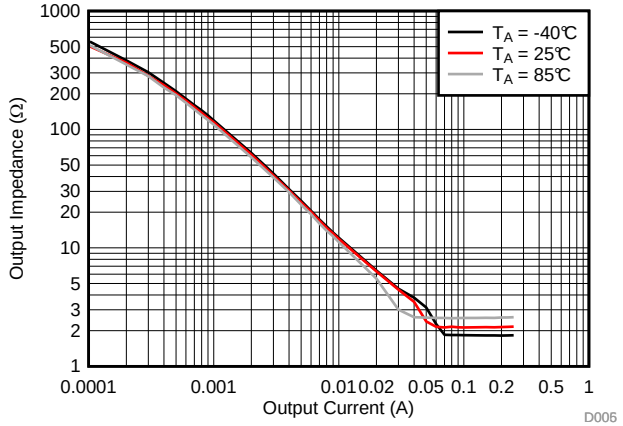


Figure 3. Shutdown Current vs Input Voltage



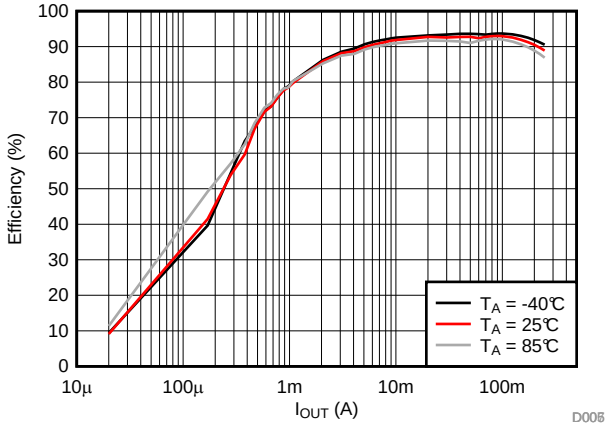
No load

Figure 4. Quiescent Current vs Input Voltage



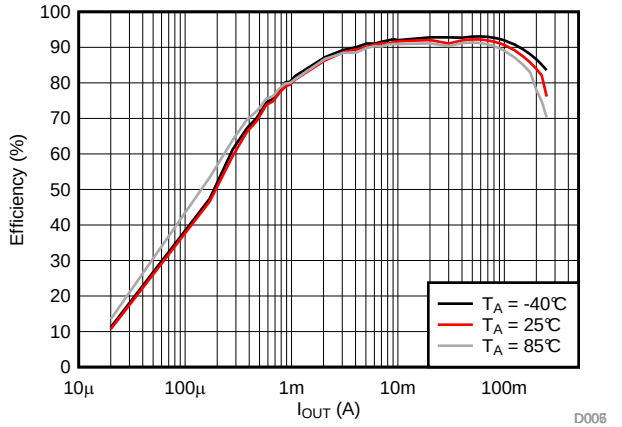
V_{IN} = 5.5 V

Figure 5. Output Impedance vs Output Current



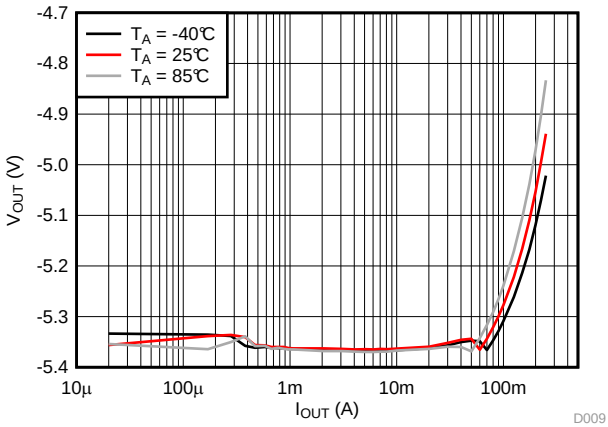
V_{IN} = 5.5 V

Figure 6. Efficiency vs Output Current



V_{IN} = 3.6 V

Figure 7. Efficiency vs Output Current

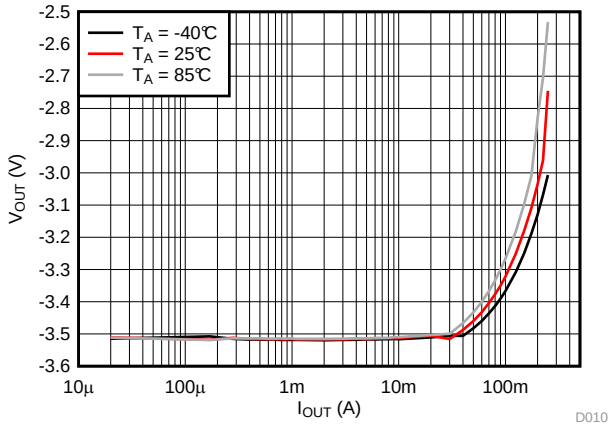


V_{IN} = 5.5 V

Figure 8. Output Voltage vs Output Current

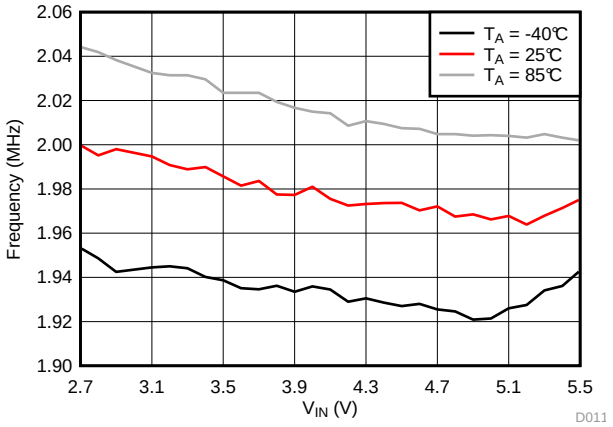
Typical Characteristics (continued)

(*Typical Application* circuit, V_{IN} = 3.6 V unless otherwise specified.)



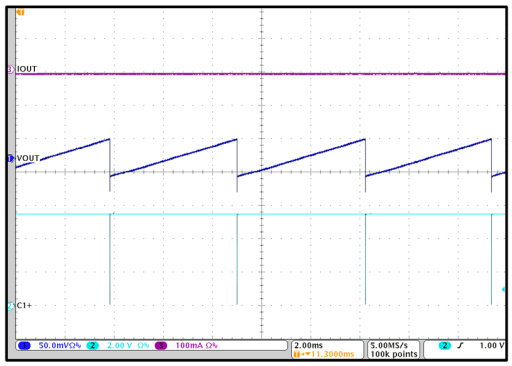
V_{IN} = 3.6 V

Figure 9. Output Voltage vs Output Current



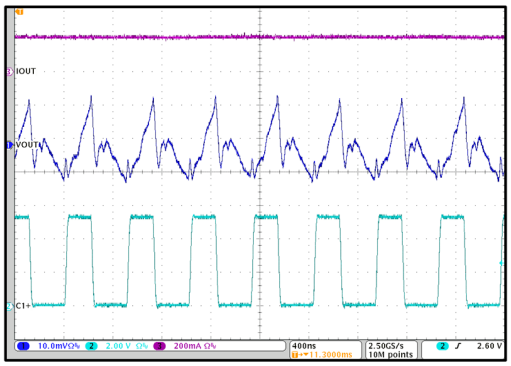
I_{OUT} = 150 mA

Figure 10. Frequency vs Input Voltage



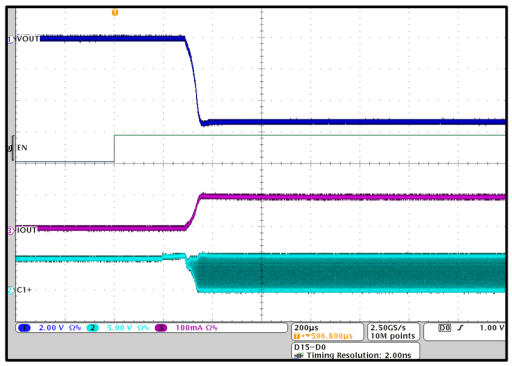
I_{OUT} = 0 mA V_{IN} = 5.5 V

Figure 11. Unloaded Output Voltage Ripple



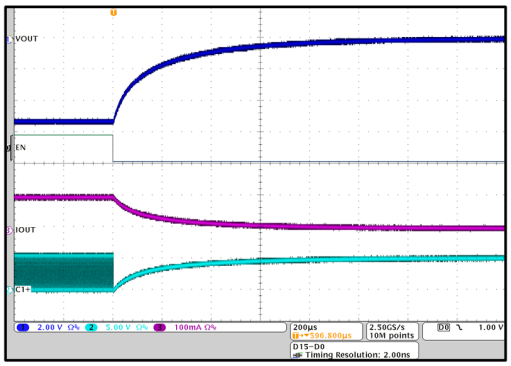
I_{OUT} = 200 mA V_{IN} = 5.5 V

Figure 12. Loaded Output Voltage Ripple



EN = 1 V_{IN} = 5.5 V I_{OUT} = 100 mA

Figure 13. EN High

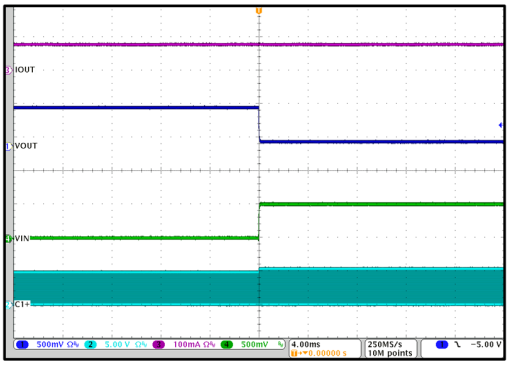


EN = 0 V_{IN} = 5.5 V I_{OUT} = 100 mA

Figure 14. EN Low

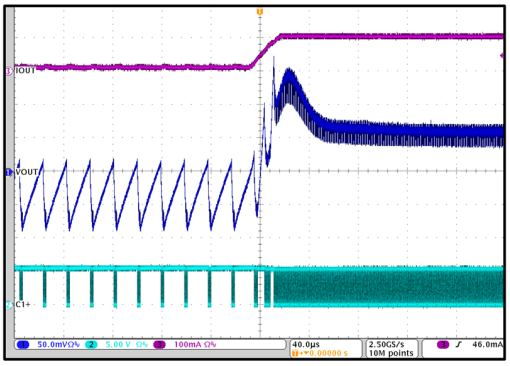
Typical Characteristics (continued)

(*Typical Application* circuit, V_{IN} = 3.6 V unless otherwise specified.)



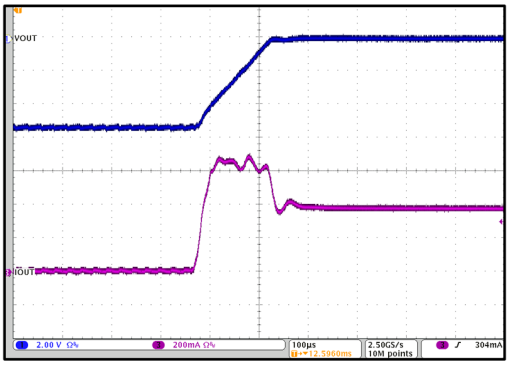
I_{OUT} = 75 mA

Figure 15. Line Step 5.5 V to 5 V



V_{IN} = 5.5 V

Figure 16. Load Step 10 mA to 100 mA



V_{IN} = 5.5 V

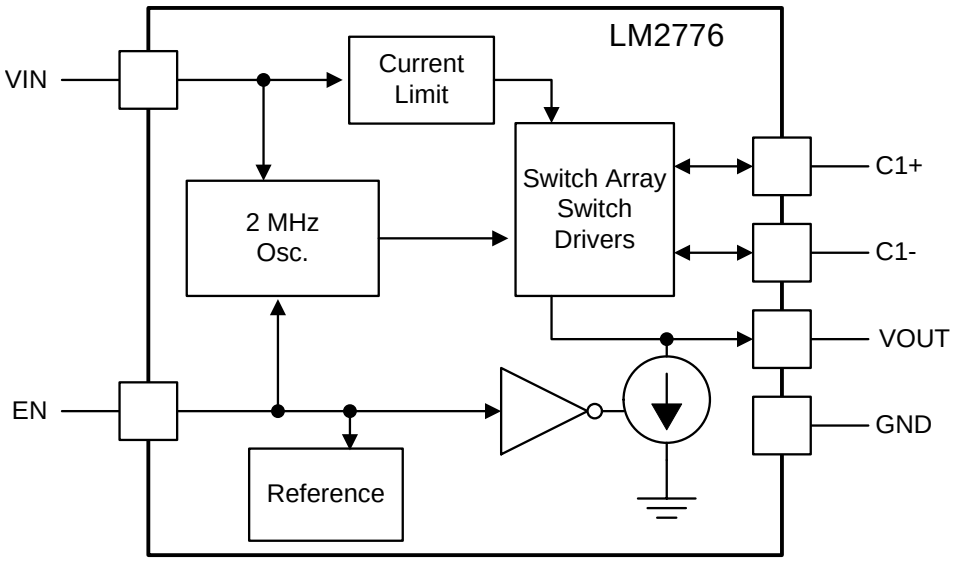
Figure 17. Output Short

7 Detailed Description

7.1 Overview

The LM2776 CMOS charge-pump voltage converter inverts a positive voltage in the range of 2.7 V to 5.5 V to the corresponding negative voltage of −2.7 V to −5.5 V. The LM2776 uses three low-cost capacitors to provide up to 200 mA of output current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Current Limit

The LM2776 contains current limit circuitry that protects the device in the event of excessive input current and/or output shorts to ground. The input current is limited to 400 mA (typical at V_{IN} = 5.5 V) when the output is shorted directly to ground. When the LM2776 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling is expected.

7.3.2 PFM Operation

To minimize quiescent current during light load operation, the LM2776 allows PFM or pulse-skipping operation. By allowing the charge pump to switch less when the output current is less than 40 mA, the quiescent current drawn from the power source is minimized. The frequency of pulsed operation is not limited and can drop into the sub-1-kHz range when unloaded. As the load increases, the frequency of pulsing increases until it transitions to constant frequency. The fundamental switching frequency of the LM2776 is 2 MHz.

7.3.3 Output Discharge

In shutdown, the LM2776 actively pulls down on the output of the device until the output voltage reaches GND. In this mode, the current drawn from the output is approximately 1.85 mA.

7.3.4 Thermal Shutdown

The LM2776 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 150°C (typical), the part switches into shutdown mode. The LM2776 releases thermal shutdown when the junction temperature of the part is reduced to 130°C (typical).

Feature Description (continued)

Thermal shutdown is most often triggered by self-heating, which occurs when there is excessive power dissipation in the device and/or insufficient thermal dissipation. LM2776 power dissipation increases with increased output current and input voltage. When self-heating brings on thermal shutdown, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown (where internal power dissipation is practically zero), cools, turns on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped be reducing the internal power dissipation (reduce input voltage and/or output current) or the ambient temperature. If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the LM2776.

7.3.5 Undervoltage Lockout

The LM2776 has an internal comparator that monitors the voltage at V_{IN} and forces the device into shutdown if the input voltage drops to 2.4 V. If the input voltage rises above 2.6 V, the LM2776 resumes normal operation.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

An enable pin (EN) pin is available to disable the device and place the LM2776 into shutdown mode reducing the quiescent current to 1 µA. In shutdown, the output of the LM2776 is pulled to ground by an internal pullup current source (approx 1.85 mA).

7.4.2 Enable Mode

Applying a voltage greater than 1.2 V to the EN pin places the device into enable mode. When unloaded, the input current during operation is 120 µA. As the load current increases, so does the quiescent current. When enabled, the output voltage is equal to the inverse of the input voltage minus the voltage drop across the charge pump.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2776 CMOS charge-pump voltage converter inverts a positive voltage in the range of 2.7 V to 5.5 V to the corresponding negative voltage of −2.7 V to −5.5 V. The device uses three low-cost capacitors to provide up to 200 mA of output current. The LM2776 operates at 2-MHz oscillator frequency to reduce output resistance and voltage ripple under heavy loads. With an operating current of only 100 µA (operating efficiency greater than 91% with most loads) and 1-µA typical shutdown current, the LM2776 provides ideal performance for battery-powered systems.

8.2 Typical Application - Voltage Inverter

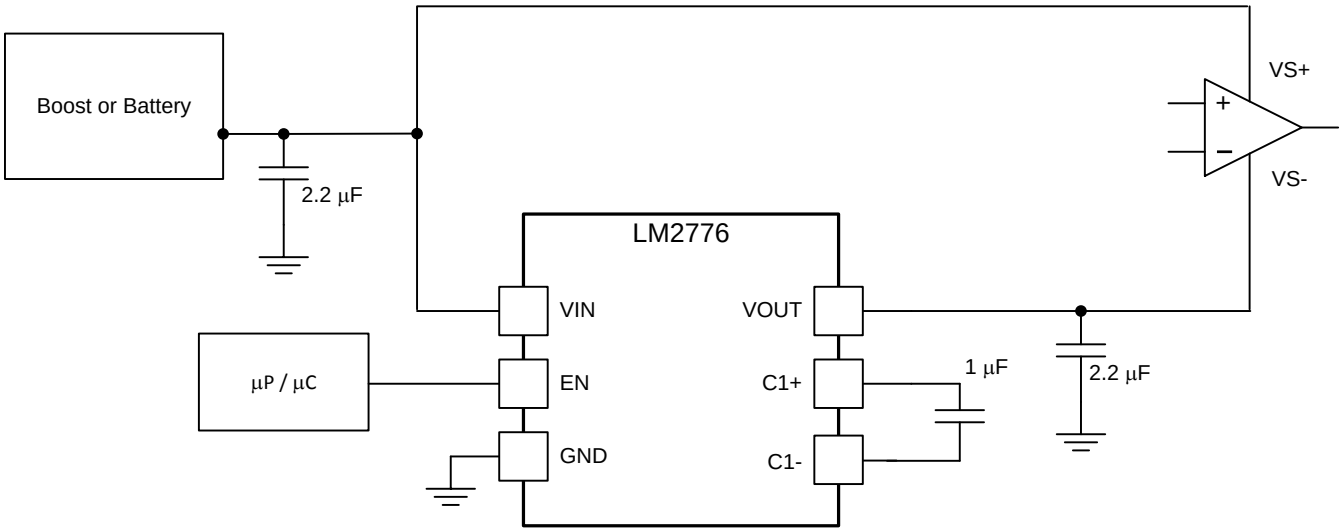


Figure 18. Voltage Inverter

8.2.1 Design Requirements

Example requirements for typical voltage inverter applications:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 5.5 V
Output current	0 mA to 200 mA
Boost switching frequency	2 MHz

8.2.2 Detailed Design Requirements

The main application of LM2776 is to generate a negative supply voltage. The voltage inverter circuit uses only three external capacitors with an range of the input supply voltage from 2.7 V to 5.5 V.

The LM2776 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 19 shows the voltage conversion scheme. When S_1 and S_3 are closed, C_1 charges to the supply voltage V_{IN}. During this time interval, switches S_2 and S_4 are open. In the second time interval, S_1 and S_3 are open; at the same time, S_2 and S_4 are closed, C_1 is charging C_2. After a number of cycles, the voltage across C_2 is pumped to VIN. Because the anode of C_2 is connected to ground, the output at the cathode of C_2 equals −(VIN) when there is no load current. The output voltage drop when a load is added is determined by the parasitic resistance ($R_{ds(on)}$ of the MOSFET switches and the equivalent series resistance (ESR) of the capacitors) and the charge transfer loss between capacitors.

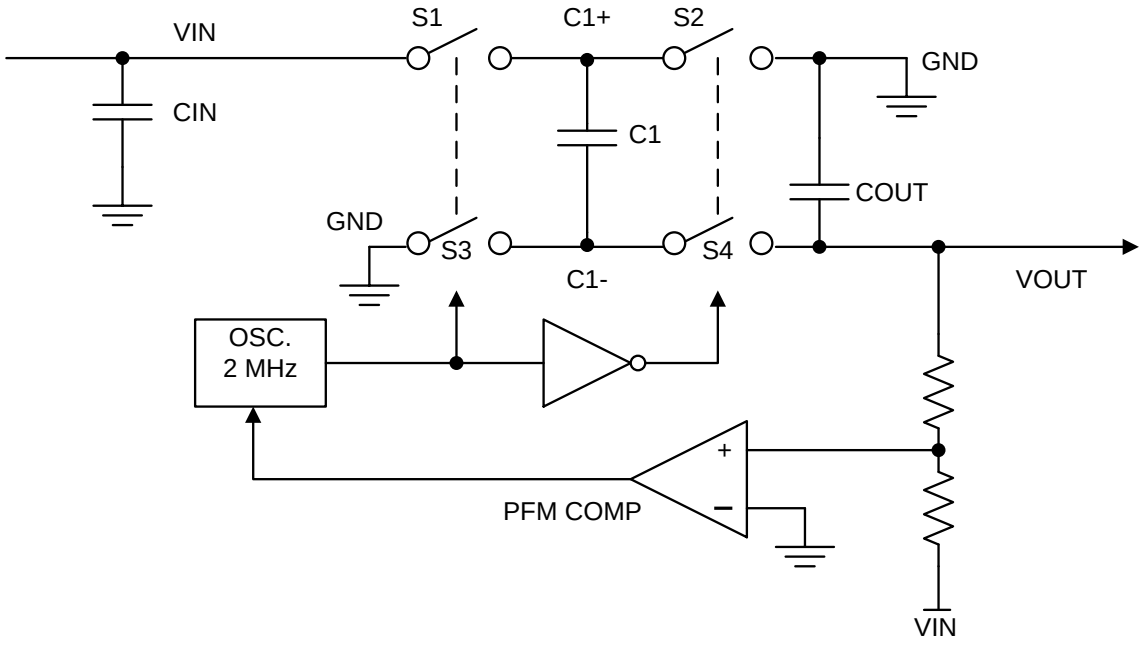


Figure 19. Voltage Inverting Principle

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals − (V_{IN}). The output resistance R_{OUT} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance and ESR of C_1 and C_2. Because the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation of R_{OUT} is:

$$R_{OUT} = (2 \times R_{SW}) + [1 / (f_{SW} \times C)] + (4 \times ESR_{C1}) + ESR_{COUT} \quad (1)$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in Figure 19.

High-capacitance, low-ESR ceramic capacitors reduce the output resistance.

8.2.2.1 Efficiency

Charge-pump efficiency is defined as

$$\text{Efficiency} = [(V_{OUT} \times I_{OUT}) / \{V_{IN} \times (I_{IN} + I_Q)\}] \quad (2)$$

where

- I_Q (V_{IN}) is the quiescent power loss of the device.

8.2.2.2 Power Dissipation

LM2776 power dissipation (P_D) is calculated simply by subtracting output power from input power:

$$P_D = P_{IN} – P_{OUT} = [V_{IN} × (–I_{OUT} + I_Q)] – [V_{OUT} × I_{OUT}] \quad (3)$$

Power dissipation increases with increased input voltage and output current. Internal power dissipation self-heats the device. Dissipating this amount power/heat so the LM2776 does not overheat is a demanding thermal requirement for a small surface-mount package. When soldered to a PCB with layout conducive to power dissipation, the thermal properties of the SOT package enable this power to be dissipated from the LM2776 with little or no derating, even when the circuit is placed in elevated ambient temperatures when the output current is 200 mA or less.

8.2.2.3 Capacitor Selection

The LM2776 requires 3 external capacitors for proper operation. TI recommends surface-mount multi-layer ceramic capacitors. These capacitors are small, inexpensive, and have very low ESR (≤ 15 mΩ typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM2776 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferred for use with the LM2776. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over –55ºC to 125°C; X5R: ±15% over –55°C to 85°C).

Capacitors with a Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2776. These types of capacitors typically have wide capacitance tolerance (80%, …20%) and vary significantly over temperature (Y5V: 22%, –82% over –30°C to 85°C range; Z5U: 22%, –56% over 10°C to 85°C range). Under some conditions, a 1-µF-rated Y5V or Z5U capacitor could have a capacitance as low as 0.1 µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2776.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower capacitance than expected on the input and/or output, resulting in higher ripple voltages and currents. Using capacitors at DC bias voltages significantly below the capacitor voltage rating usually minimizes DC bias effects. Consult capacitor manufacturers for information on capacitor DC bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. It is strongly recommended that the LM2776 circuit be thoroughly evaluated early in the design-in process with the mass-production capacitors of choice. This helps ensure that any such variability in capacitance does not negatively impact circuit performance.

The voltage rating of the output capacitor must be 10 V or more. For example, a 10-V 0603 1-µF is acceptable for use with the LM2776, as long as the capacitance does not fall below a minimum of 0.5 µF in the intended application. All other capacitors must have a voltage rating at or above the maximum input voltage of the application. Select the capacitors such that the capacitance on the input does not fall below 0.7 µF, and the capacitance of the flying capacitor does not fall below 0.2 µF.

8.2.2.4 Output Capacitor and Output Voltage Ripple

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the output capacitor C_{OUT}:

$$V_{RIPPLE} = [(2 × I_{LOAD}) / (f_{SW} × C_{OUT})] + (2 × I_{LOAD} × ESR_{COUT}) \quad (4)$$

In typical applications, a 1-µF low-ESR ceramic output capacitor is recommended. Different output capacitance values can be used to reduce ripple shrink the solution size, and/or cut the cost of the solution. But changing the output capacitor may also require changing the flying capacitor and/or input capacitor to maintain good overall circuit performance.

NOTE

In high-current applications, TI recommends a 10-µF, 10-V low-ESR ceramic output capacitor. If a small output capacitor is used, the output ripple can become large during the transition between PFM mode and constant switching. To prevent toggling, a 2-µF capacitance is recommended. For example, a 10- µF, 10-V output capacitor in a 0402 case size typically only has 2-µF capacitance when biased to 5 V.

High ESR in the output capacitor increases output voltage ripple. If a ceramic capacitor is used at the output, this is usually not a concern because the ESR of a ceramic capacitor is typically very low and has only a minimal impact on ripple magnitudes. If a different capacitor type with higher ESR is used (tantalum, for example), the ESR could result in high ripple. To eliminate this effect, the net output ESR can be significantly reduced by placing a low-ESR ceramic capacitor in parallel with the primary output capacitor. The low ESR of the ceramic capacitor is in parallel with the higher ESR, resulting in a low net ESR based on the principles of parallel resistance reduction.

8.2.2.5 Input Capacitor

The input capacitor (C_{IN}) is a reservoir of charge that aids a quick transfer of charge from the supply to the flying capacitors during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitors are connected to the input. It also filters noise on the input pin, keeping this noise out of sensitive internal analog circuitry that is biased off the input line.

Much like the relationship between the output capacitance and output voltage ripple, input capacitance has a dominant and first-order effect on input ripple magnitude. Increasing (decreasing) the input capacitance results in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also affects input ripple levels to some degree.

In typical applications, a 1-µF low-ESR ceramic capacitor is recommended on the input. When operating near the maximum load of 200 mA, a minimum recommended input capacitance after taking into the DC-bias derating is 2 µF or larger. Different input capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution.

8.2.2.6 Flying Capacitor

The flying capacitor (C1) transfers charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM2776 may not be able to regulate the output voltage when load currents are high. On the other hand, if the flying capacitance is too large, the flying capacitor might overwhelm the input and output capacitors, resulting in increased input and output ripple.

In typical high-current applications, TI recommends 0.47-µF or 1-µF 10 V low-ESR ceramic capacitors for the flying capacitors. Polarized capacitors (tantalum, aluminum electrolytic, etc.) must not be used for the flying capacitor, as they could become reverse-biased during LM2776 operation.

8.2.3 Application Curve

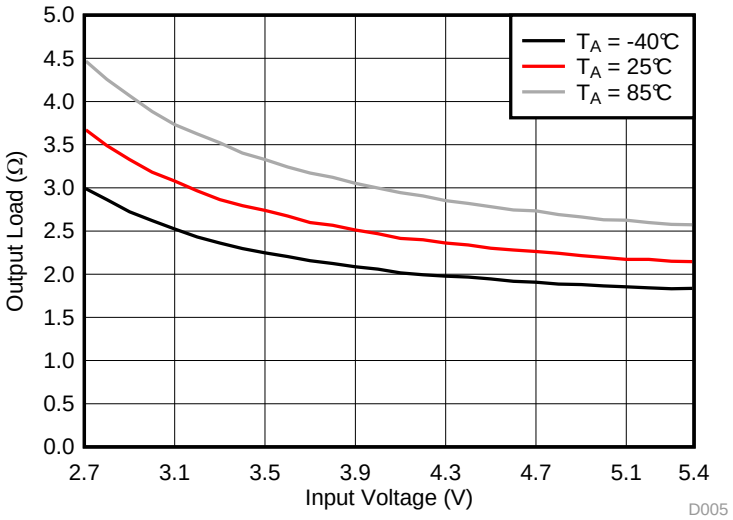


Figure 20. Output Impedance vs Input Voltage

9 Power Supply Recommendations

The LM2776 is designed to operate from an input voltage supply range from 2.7 V to 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM2776 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high switching frequency and large switching currents of the LM2776 make the choice of layout important. Use the following steps as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range:

- Place C_{IN} on the top layer (same layer as the LM2776) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the VIN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the VIN line.
- Place C_{OUT} on the top layer (same layer as the LM2776) and as close to the VOUT and GND pins as possible. The returns for both C_{IN} and C_{OUT} must come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces reduce the series inductance on the VOUT and GND pins that can corrupt the V_{OUT} and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on the top layer (same layer as the LM2776) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the C1+ and C1– pins.

10.2 Layout Example

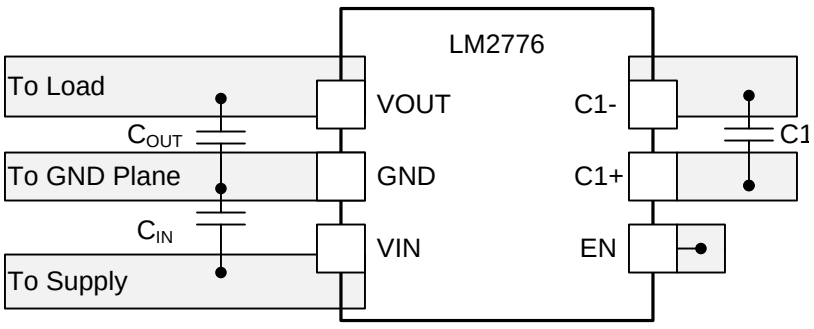


Figure 21. LM2776 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2776DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	2776	Samples
LM2776DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	2776	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

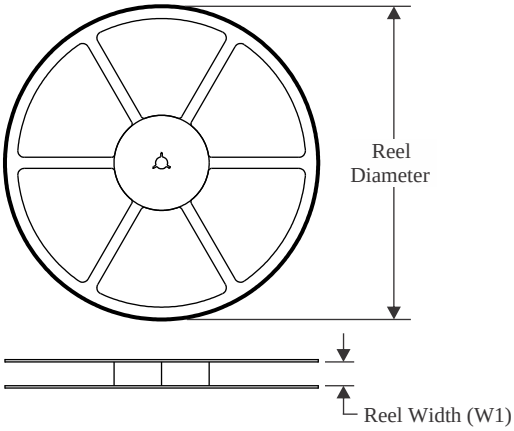
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

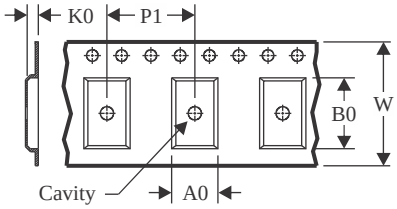
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

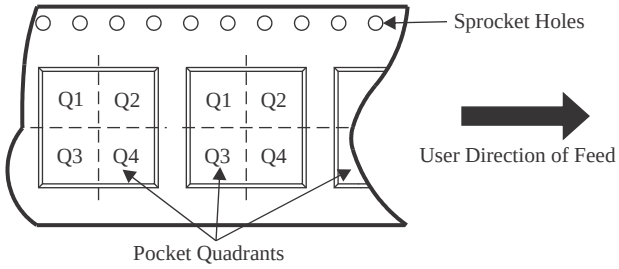


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

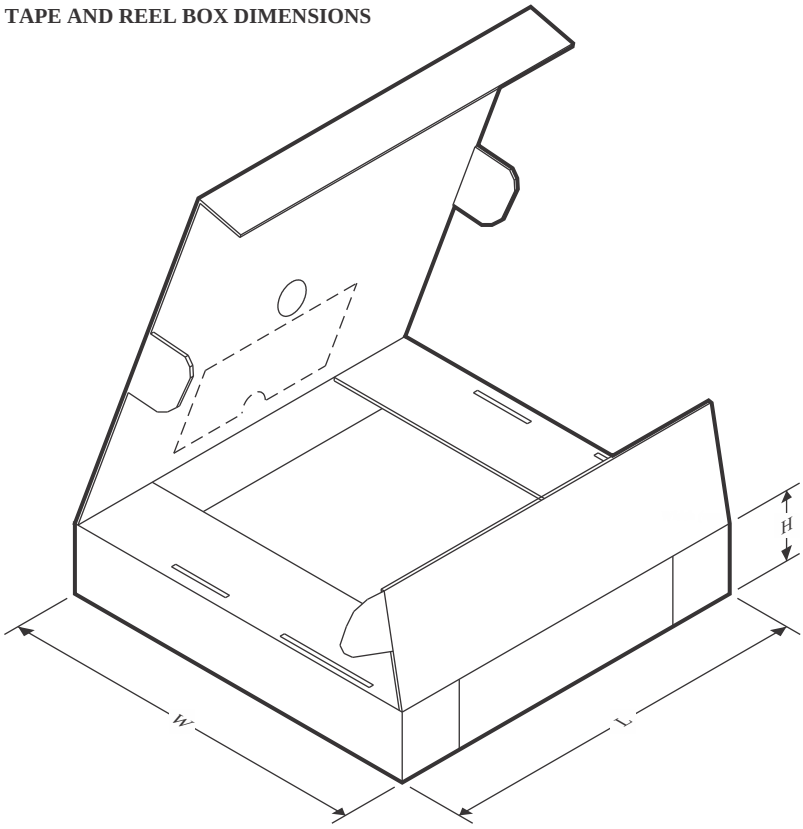
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2776DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LM2776DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2776DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2776DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

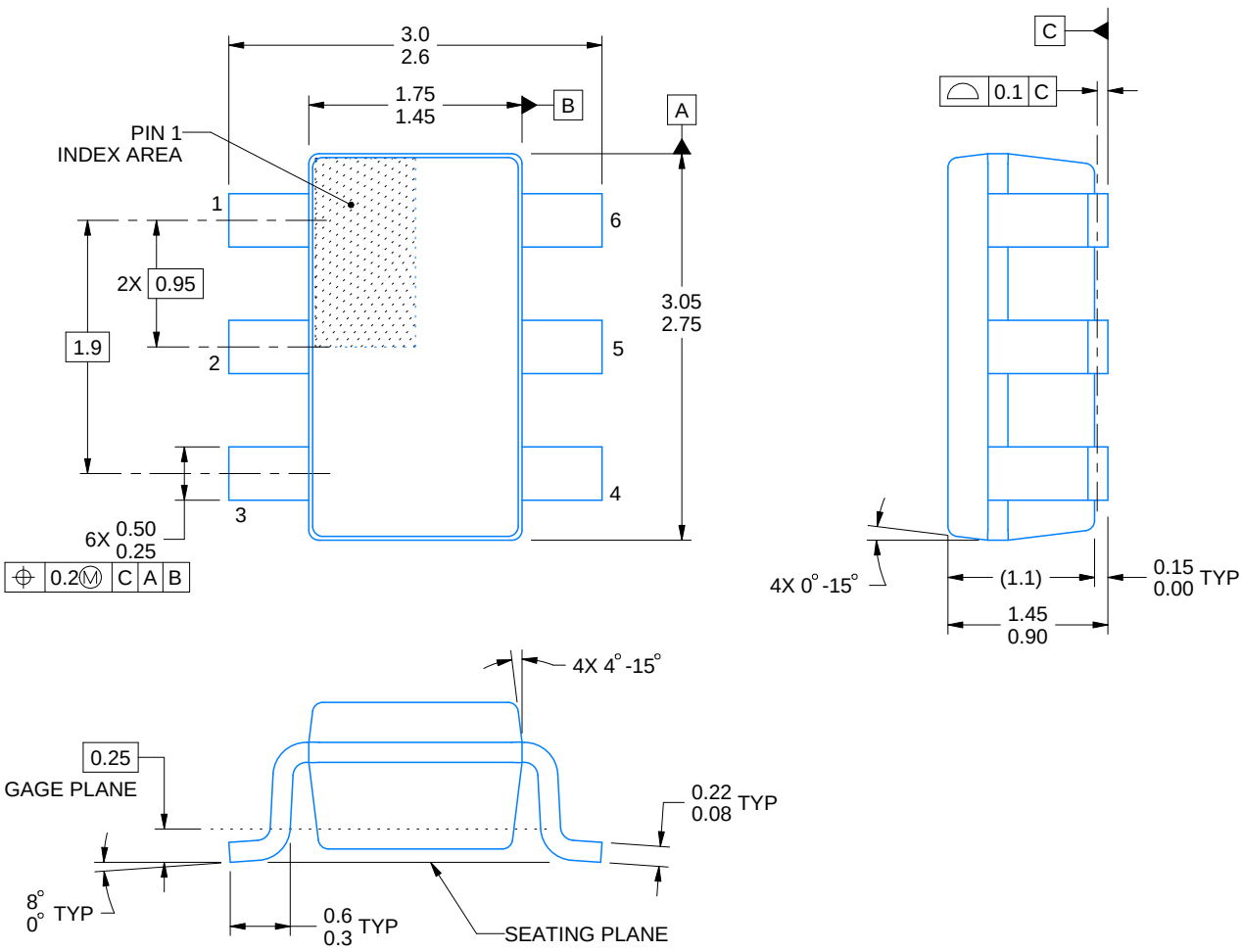
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2776DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
LM2776DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM2776DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
LM2776DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

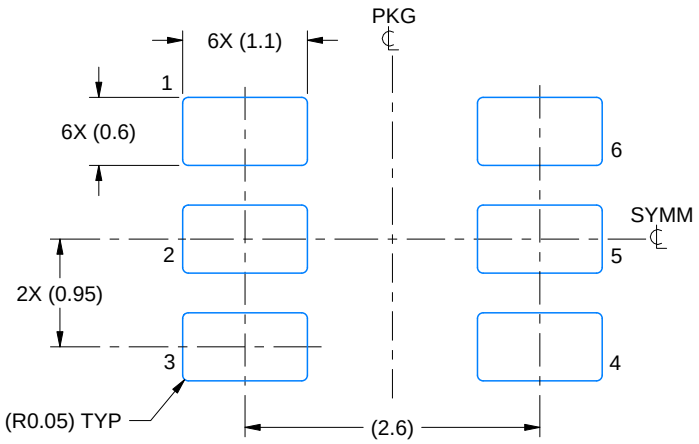
SMALL OUTLINE TRANSISTOR



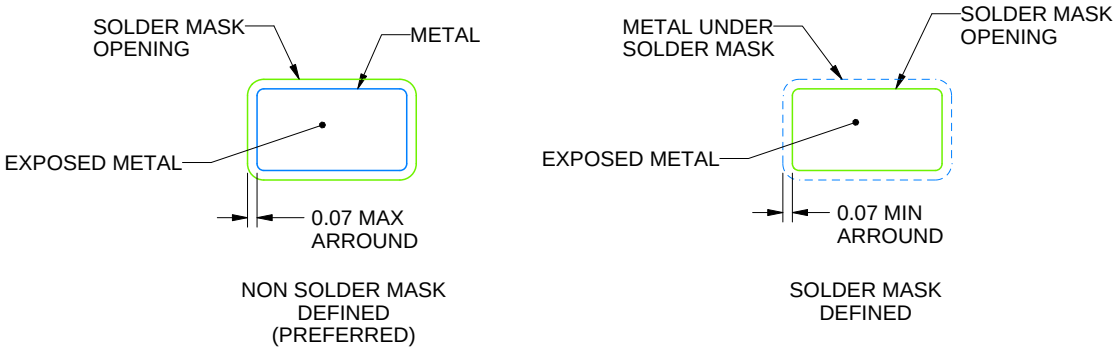
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

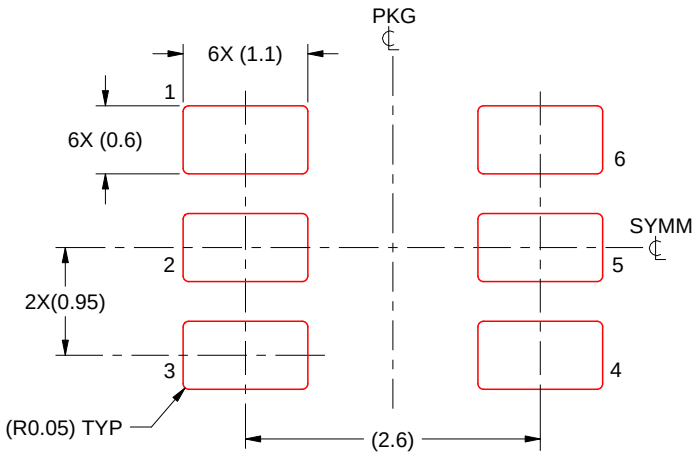


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265