LM25011/LM25011-Q1/LM25011A/LM25011A-Q1 42V 2Aコンスタント・オンタイム・スイッチング・レギュレータ、可変電流制限機能付き

1 特長

- LM25011-Q1はAEC-Q100グレード1準拠の車載グレード製品(−40℃～＋125℃の接合部温度で動作)
- LM25011Aでは高いスイッチング周波数で低ドロップアウト動作が可能
- 動作入力電圧範囲: 6V～42V
- 絶対最大定格入力電圧: 45V
- 2AのNチャネル降圧スイッチを内蔵
- 可変電流制限機能によりインダクタの小型化が可能
- 設定可能な出力電圧は2.51V以上
- V_{OUT}でのリップル電圧は最小限
- パワー・グッド出力
- スイッチング周波数が2MHzまで可変
- COT方式の特長:
  - 負荷電流や入力電圧の変動に関係なく、スイッチング周波数をほぼ一定に維持
  - 超高速の過渡応答
  - ループ補償が不要
  - セラミック出力コンデンサで安定動作
  - 出力コンデンサと電流センス抵抗の小型化が可能
- 可変ソフトスタート・タイミング
- サーマル・シャットダウン
- 2%の高精度帰還基準電圧
- パッケージ: 10ピン、HVSSOP
- WEBENCH Power Designerにより、LM25011ファミリを使用するカスタム設計を作成

2 アプリケーション

- 車載用安全装置
- インフォテインメント
- 電気通信
- フロント・カメラ

3 概要

LM25011コンスタント・オンタイム降圧型スイッチング・レギュレータは、最大2Aの負荷電流を供給可能な、低コストかつ高効率の降圧型バイアス・レギュレータを実装するために必要なすべての機能を備えています。この高電圧レギュレータには、Nチャネル降圧スイッチ、スタートアップ・レギュレータ、電流制限検出機能、内部リップル制御機能が内蔵されています。コンスタント・オンタイム制御は原理上、ループ補償を必要としないため、高速な負荷過渡応答と単純な回路実装を実現できます。入力電圧変動や負荷変動に対して動作周波数は一定に保たれます。調整可能なバレー電流制限検出機能により、電流制限値に達すると電流制限フォールドバックを行わずに、定電圧から定電流モードへとスムーズに移行します。出力電圧が予想制御値の5%以内に上昇するとPGD出力により通知されます。ほかにも低出力リップル、VIN低電圧誤動作防止、可変ソフトスタート・タイミング、サーマル・シャットダウン、ゲート・ドライブ・プリチャージ、ゲート・ドライブ低電圧誤動作防止、最大デューティ・サイクル制限といった特長を備えています。

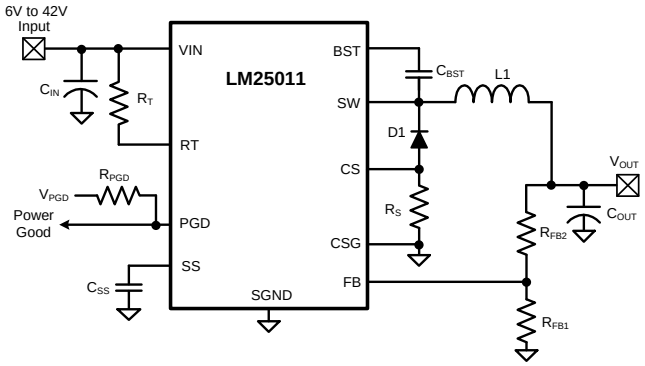
LM25011AはLM25011に比べて最小オフ時間が短いため、低い入力電圧で高周波動作が可能です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM25011 / -Q1	HVSSOP (10)	3.00mm×3.00mm
LM25011A / -Q1		

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーション



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision G (February 2013) から **Revision H** に変更 **Page**

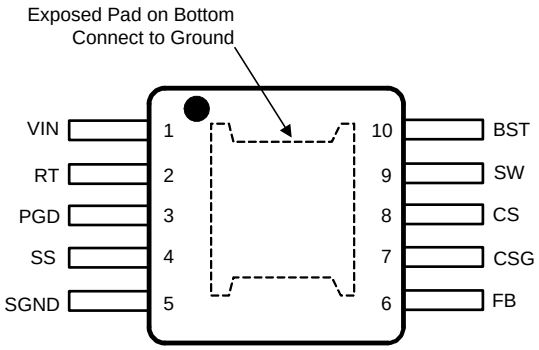
- 「*ピン構成および機能*」セクション、「*取り扱いに関する定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1

Revision F (February 2013) から **Revision G** に変更 **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 23

5 Pin Configuration and Functions

10-Pin
HVSSOP Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NUMBER	NAME			
1	VIN	I	Input supply voltage	Operating input range is 6 V to 42 V. Transient capability is 45 V. A low ESR capacitor must be placed as close as possible to the VIN and SGND pins.
2	RT	I	On-time Control	An external resistor from VIN to this pin sets the buck switch on-time and the switching frequency.
3	PGD	–	Power Good	Logic output indicates when the voltage at the FB pin has increased to above 95% of the internal reference voltage. Hysteresis is provided. An external pull-up resistor to a voltage less than 7 V is required.
4	SS	I	Soft-Start	An internal current source charges an external capacitor to provide the soft-start function.
5	SGND		Signal Ground	Ground for all internal circuitry other than the current limit sense circuit.
6	FB	I	Feedback	Internally connected to the regulation comparator. The regulation level is 2.51 V.
7	CSG	–	Current Sense Ground	Ground connection for the current limit sensing circuit. Connect to ground and to the current sense resistor.
8	CS	I	Current sense	Connect to the current sense resistor and the anode of the free-wheeling diode.
9	SW	O	Switching Node	Internally connected to the buck switch source. Connect to the external inductor, cathode of the free-wheeling diode, and bootstrap capacitor.
10	BST	I	Bootstrap capacitor connection of the buck switch gate driver.	Connect a 0.1-µF capacitor from SW to this pin. The capacitor is charged during the buck switch off-time via an internal diode.
-	EP	–	Exposed Pad	Exposed pad on the underside of the package. This pad should be soldered to the PC board ground plane to aid in heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
VIN to SGND (T_J = 25°C)		45	V
BST to SGND		52	V
SW to SGND (Steady State)	–1.5	45	V
BST to SW	–0.3	7	V
CS to CSG	–0.3	0.3	V
CSG to SGND	–0.3	0.3	V
PGD to SGND	–0.3	7	V
SS to SGND	–0.3	3	V
RT to SGND	–0.3	1	V
FB to SGND	–0.3	7	V
For soldering specs, see www.ti.com/packaging.			
Junction Temperature		150	°C

(1) *Absolute Maximum Ratings*(1) are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics* .

6.2 Handling Ratings: LM25011

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Handling Ratings: LM25011-Q1

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)			2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 5, 6, and 10)		750	
			Other pins		750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN Voltage	6.0	42	V
Junction Temperature	–40	125	°C

(1) *Absolute Maximum Ratings*(1) are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics* .

6.5 Thermal Information

THERMAL METRIC(1)		HVSSOP (DGQ)	UNIT
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.2	
ψ_{JT}	Junction-to-top characterization parameter	4.0	
ψ_{JB}	Junction-to-board characterization parameter	33.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, R_T = 50 kΩ.(1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (VIN PIN)						
I_{IN}	Input operating current	Non-switching, FB = 3 V		1200	1600	µA
$UVLO_{VIN}$	V_{IN} undervoltage lock-out threshold	V_{IN} increasing	4.6	5.3	5.9	V
	V_{IN} undervoltage lock-out threshold hysteresis			200		mV
SWITCH CHARACTERISTICS						
$R_{DS(ON)}$	Buck Switch $R_{DS(ON)}$	I_{TEST} = 200 mA		0.3	0.6	Ω
$UVLO_{GD}$	Gate Drive UVLO	BST-SW	2.4	3.4	4.4	V
	$UVLO_{GD}$ Hysteresis			350		mV
	Pre-charge switch voltage	I_{TEST} = 10 mA into SW pin		1.4		V
	Pre-charge switch on-time			120		ns
SOFT-START PIN						
V_{SS}	Pullup voltage			2.51		V
I_{SS}	Internal current source			10		µA
V_{SS-SH}	Shutdown threshold		70	140		mV
CURRENT LIMIT						
V_{ILIM}	Threshold voltage at CS		–146	–130	–115	mV
	CS bias current	FB = 3 V		–120		µA
	CSG bias current	FB = 3 V		–35		µA
ON TIMER, RT PIN						
t_{ON} - 1	On-time	V_{IN} = 12 V, R_T = 50 kΩ	150	200	250	ns
t_{ON} - 2	On-time	V_{IN} = 32 V, R_T = 50 kΩ		75		ns
t_{ON} - 3	On-time (current limit) LM25011	V_{IN} = 12 V, R_T = 50 kΩ		100		ns
t_{ON} - 3	On-time (current limit) LM25011A	V_{IN} = 12 V, R_T = 50 kΩ		200		ns
t_{ON} - 4	On-time	V_{IN} = 12 V, R_T = 301 kΩ		1020		ns
t_{ON} - 5	On-time	V_{IN} = 9 V, R_T = 30.9 kΩ	130	171	215	ns
t_{ON} - 6	On-time	V_{IN} = 12 V, R_T = 30.9 kΩ	105	137	170	ns
t_{ON} - 7	On-time	V_{IN} = 16 V, R_T = 30.9 kΩ	79	109	142	ns
OFF TIMER						
t_{OFF}	Minimum off-time (LM25011)		90	150	208	ns
	Minimum off-time (LM25011A)		52	75	93	
REGULATION COMPARATOR (FB PIN)						
V_{REF}	FB regulation threshold	SS pin = steady state	2.46	2.51	2.56	V
	FB bias current	FB = 3 V		100		nA
POWER GOOD (PGD PIN)						
	Threshold at FB, with respect to V_{REF}	FB increasing	91%	95%		
	Threshold hysteresis			3.3%		
PGD_{VOL}	Low state voltage	I_{PGD} = 1 mA, FB = 0 V		125	180	mV
PGD_{LKG}	Off state leakage	V_{PGD} = 7 V, FB = 3 V		0.1		µA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown	Junction temperature increasing		155		°C
	Thermal shutdown hysteresis			20		°C

(1) Current flow out of a pin is indicated as a negative number.
(2) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in watts) as follows: $T_J = T_A + (P_D \times R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in the *Thermal Information* section.

6.7 Typical Characteristics

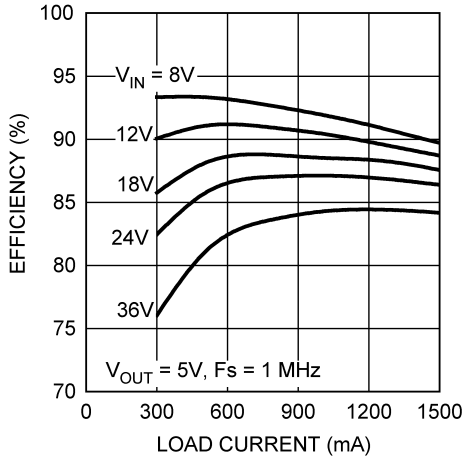


Figure 1. Efficiency (Circuit of Figure 19)

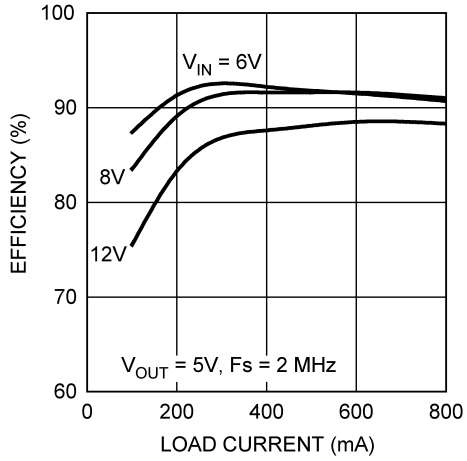


Figure 2. Efficiency at 2 MHz

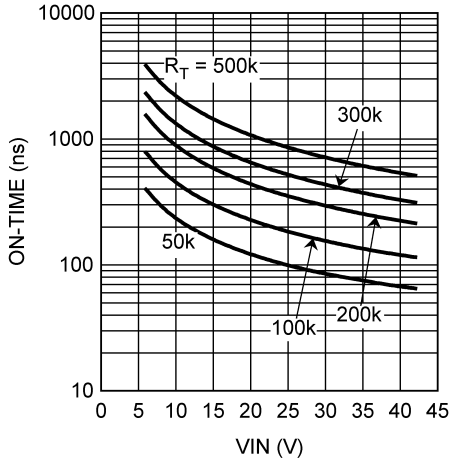


Figure 3. On-Time vs V_{IN} and R_T

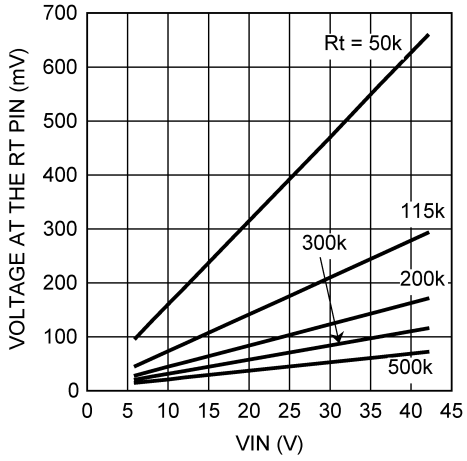


Figure 4. Voltage at the RT Pin

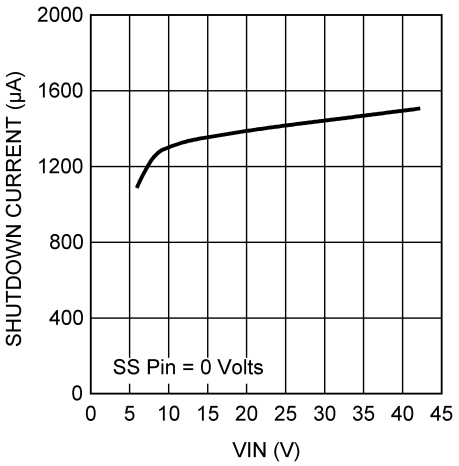


Figure 5. Shutdown Current into VIN

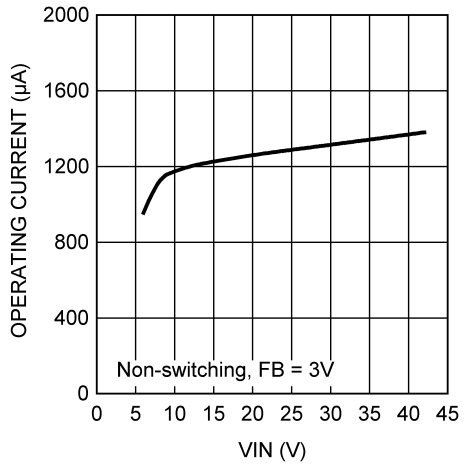


Figure 6. Operating Current into VIN

Typical Characteristics (continued)

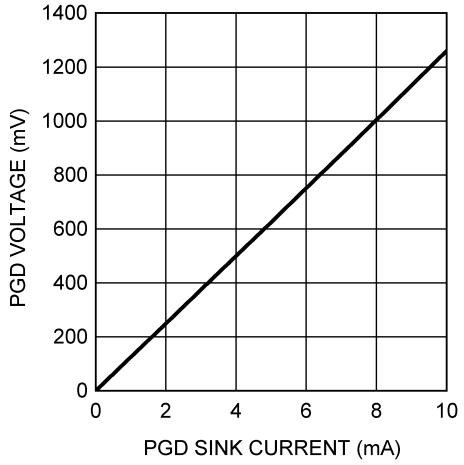


Figure 7. PGD Low Voltage vs Sink Current

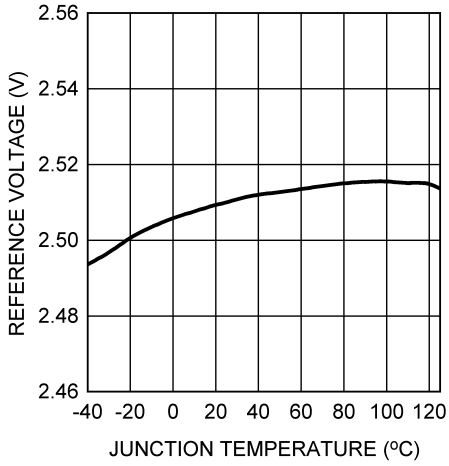


Figure 8. Reference Voltage vs Temperature

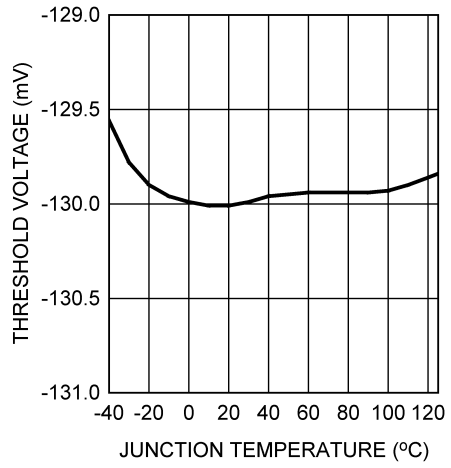


Figure 9. Current Limit Threshold vs Temperature

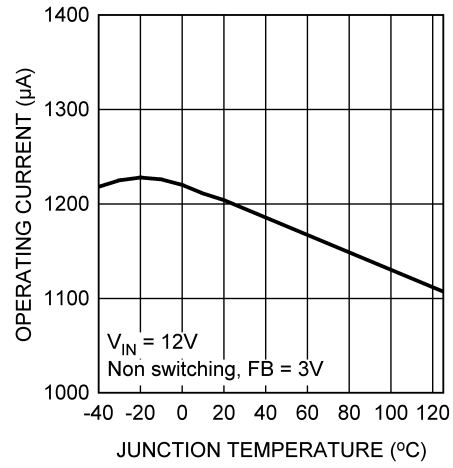


Figure 10. Operating Current vs Temperature

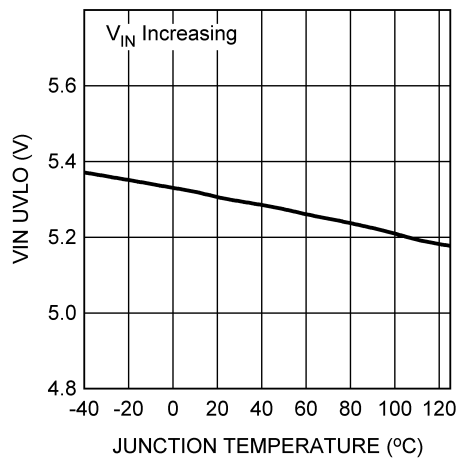


Figure 11. VIN UVLO vs Temperature

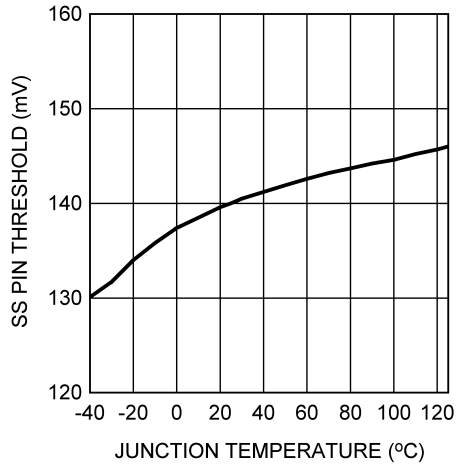


Figure 12. SS Pin Shutdown Threshold vs Temperature

Typical Characteristics (continued)

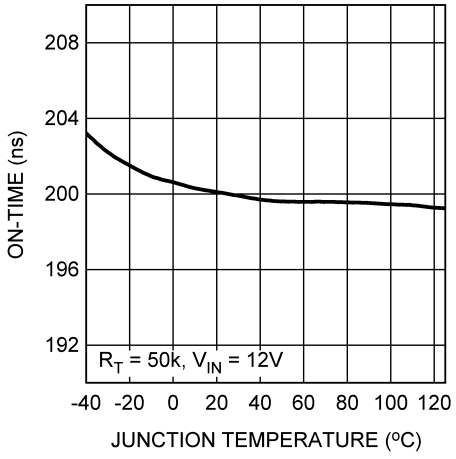


Figure 13. On-Time vs Temperature

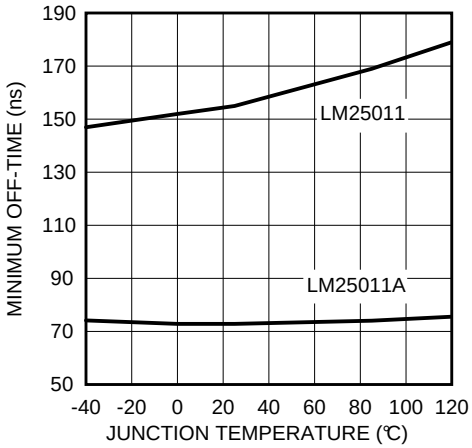


Figure 14. Minimum Off-Time vs Temperature

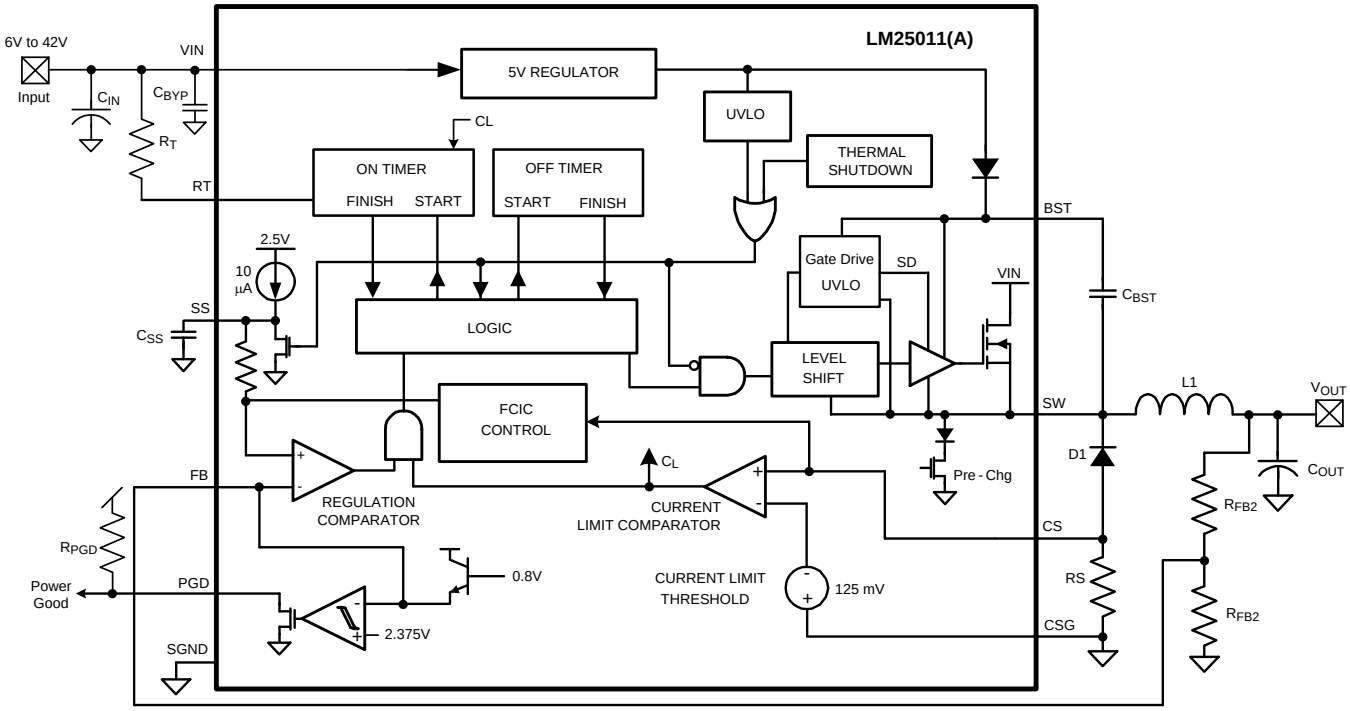
7 Detailed Description

7.1 Overview

The LM25011 constant on-time step-down switching regulator features all the functions needed to implement a low-cost, efficient buck bias power converter capable of supplying up to 2.0 A to the load. This high-voltage regulator contains an N-Channel buck switch, is easy to implement, and is available in a 10-pin VSSOP, PowerPAD power enhanced package. The operation of the regulator is based on a constant on-time control principle with the on-time inversely proportional to the input voltage. This feature results in the operating frequency remaining relatively constant with load and input voltage variations. The constant on-time feedback control principle requires no loop compensation resulting in very fast load transient response. The adjustable valley current limit detection results in a smooth transition from constant voltage to constant current when current limit is reached. To aid in controlling excessive switch current due to a possible saturating inductor, the on-time is reduced by approximately 40% when the current limit is detected. The Power Good output (PGD pin) indicates when the output voltage is within 5% of the expected regulation voltage.

The LM25011 can be implemented to efficiently step-down higher voltages in non-isolated applications. Additional features include: low output ripple, VIN under-voltage lock-out, adjustable soft-start timing, thermal shutdown, gate drive pre-charge, gate drive under-voltage lock-out, and maximum duty-cycle limit.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Circuit Overview

The LM25011 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (2.51 V). If the FB voltage is below the reference, the internal buck switch is switched on for the one-shot timer period which is a function of the input voltage and the programming resistor (R_T). Following the on-time, the switch remains off until the FB voltage falls below the reference, but never less than the minimum off-time forced by the off-time one-shot timer. When the FB pin voltage falls below the reference and the off-time one-shot period expires, the buck switch is then turned on for another on-time one-shot period.

Feature Description (continued)

When in regulation, the LM25011 operates in continuous conduction mode at heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode, the inductor current is always greater than zero and the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half of the ripple current amplitude of the inductor. The approximate operating frequency is calculated as follows:

$$F_S = \frac{V_{OUT}}{(4.1 \times 10^{-11} \times (R_T + 0.5k)) + (V_{IN} \times 15\ ns)} \quad (1)$$

The buck switch duty cycle is approximately equal to:

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times F_S = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

When the load current is less than one-half of the ripple current amplitude of the inductor, the circuit operates in discontinuous conduction mode. The off-time is longer than in continuous conduction mode while the inductor current is zero, causing the switching frequency to reduce as the load current is reduced. Conversion efficiency is maintained at light loads because the switching losses are reduced with the reduction in load and frequency. The approximate discontinuous operating frequency can be calculated as follows:

$$F_S = \frac{V_{OUT}^2 \times L1 \times 1.19 \times 10^{21}}{R_L \times R_T^2} \quad (3)$$

where R_L = the load resistance, and L1 is the inductor in the circuit.

The output voltage is set by the two feedback resistors (R_{FB1}, R_{FB2} in the *Functional Block Diagram*). The regulated output voltage is calculated as follows:

$$V_{OUT} = 2.51\ V \times (R_{FB1} + R_{FB2}) / R_{FB1} \quad (4)$$

Ripple voltage, which is required at the input of the regulation comparator for proper output regulation, is generated internally in the LM25011, and externally when the LM25011A is used. In the LM25011 the ERM (emulated ripple mode) control circuit generates the required internal ripple voltage from the ripple waveform at the CS pin. The LM25011A, which is designed for higher frequency operation, requires additional ripple voltage which must be generated externally and provided to the FB pin. This is described in the *Application and Implementation* section.

7.3.2 On-Time Timer

The on-time for the LM25011/LM25011A is determined by the R_T resistor and the input voltage (V_{IN}), calculated from:

$$t_{ON} = \frac{4.1 \times 10^{-11} \times (R_T + 500\Omega)}{(V_{IN})} + 15\ ns \quad (5)$$

The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. To set a specific continuous conduction mode switching frequency (F_S), the R_T resistor is determined from the following:

$$R_T = \frac{V_{OUT} - (V_{IN} \times F_S \times 15\ ns)}{F_S \times 4.1 \times 10^{-11}} - 500\Omega \quad (6)$$

The on-time must be chosen greater than 90 ns for proper operation. Equation 1, Equation 5, and Equation 6 are valid only during normal operation; that is, the circuit is not in current limit. When the LM25011 operates in current limit, the on-time is reduced by approximately 40% (this feature is not present in LM25011A). This feature reduces the peak inductor current which may be excessively high if the load current and the input voltage are simultaneously high. This feature operates on a cycle-by-cycle basis until the load current is reduced and the

Feature Description (continued)

output voltage resumes its normal regulated value. The maximum continuous current into the RT pin must be less than 2 mA. For high-frequency applications, the maximum switching frequency is limited at the maximum input voltage by the minimum on-time one-shot period (90 ns). At minimum input voltage the maximum switching frequency is limited by the minimum off-time one-shot period which, if reached, prevents achievement of the proper duty cycle.

7.3.3 Current Limit

Current limit detection occurs during the off-time by monitoring the voltage across the external current sense resistor R_S. Referring to the *Functional Block Diagram* , during the off-time the recirculating current flows through the inductor, through the load, through the sense resistor, and through D1 to the inductor. If the voltage across the sense resistor exceeds the threshold (V_{ILIM}), the current limit comparator output switches to delay the start of the next on-time period. The next on-time starts when the recirculating current decreases such that the voltage across R_S reduces to the threshold and the voltage at FB is below 2.51 V. The operating frequency is typically lower due to longer-than-normal off-times. When current limit is detected, the on-time is reduced by approximately 40% (only in LM25011) if the voltage at the FB pin is below its threshold when the voltage across R_S reduces to its threshold (V_{OUT} is low due to current limiting).

Figure 15 illustrates the inductor current waveform during normal operation and in current limit. During the first normal operation, the load current is I_{01}, the average of the inductor current waveform. As the load resistance is reduced, the inductor current increases until the lower peak of the inductor ripple current exceeds the threshold. During the current limited portion of Figure 15, each on-time is reduced by approximately 40%, resulting in lower ripple amplitude for the inductor current. During this time the LM25011 is in a constant-current mode with an average load current equal to the current limit threshold plus half the ripple amplitude (I_{OCL}), and the output voltage is below the normal regulated value. Normal operation resumes when the load current is reduced (to I_{O2}), allowing V_{OUT} and the on-time to return to their normal values. Note that in the second period of normal operation, even though the peak current of the inductor exceeds the current limit threshold during part of each cycle, the circuit is not in current limit because the inductor current falls below the current limit threshold during each off-time. The peak current allowed through the buck switch is 3.5 A and the maximum allowed average current is 2.0 A.

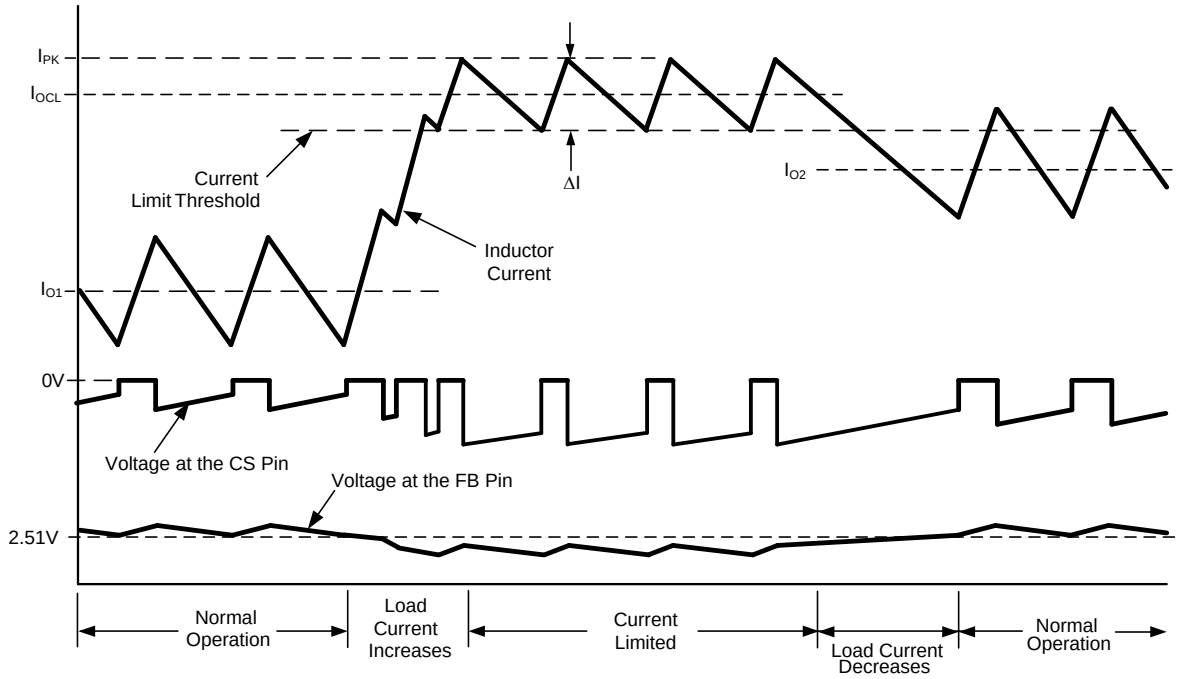


Figure 15. Normal and Current Limit Operation

Feature Description (continued)

7.3.4 Ripple Requirements

The LM25011 requires about 25 mV_{P-P} of ripple voltage at the CS pin. Higher switching frequencies may require more ripple. That ripple voltage is generated by the decreasing recirculating current (the inductor ripple current) through R_S during the off-time. See Figure 16.

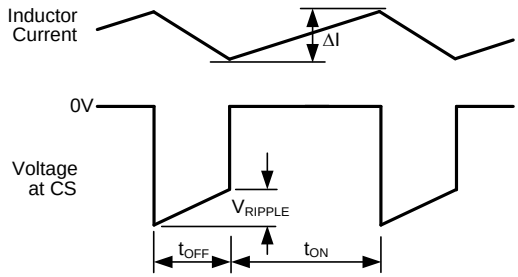


Figure 16. CS Pin Waveform

The ripple voltage is equal to:

$$V_{RIPPLE} = \Delta I \times R_S \quad (7)$$

where ΔI is the inductor current ripple amplitude, and R_S is the current-sense resistor at the CS pin.

More ripple can be achieved by decreasing the inductor value.

The LM25011A, with its shorter minimum off-time, typically will require more ripple than the LM25011. An external circuit to increase the effective ripple voltage may be needed. Different methods of generating this ripple are explained in the *External Components* section.

7.3.5 N-Channel Buck Switch and Driver

The LM25011 integrates an N-Channel buck switch and associated floating high-voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor (C_{BST}) and an internal high-voltage diode. A 0.1-µF capacitor connected between BST and SW provides the supply voltage for the driver during the on-time. During each off-time, the SW pin is at approximately –1 V, and C_{BST} is recharged from the internal 5-V regulator for the next on-time. The minimum off-time ensures a sufficient time each cycle to recharge the bootstrap capacitor.

In applications with relatively high output voltage and low minimum load current, the internal pre-charge device of the LM25011 may not pull the SW pin sufficiently low during the off-time to maintain the voltage on the bootstrap capacitor. If the bootstrap capacitor (C_{BST}) discharges during the long off-times, and the regulator will cycle on and off at a low frequency. Decreasing the values of the feedback resistors R_{FB1} and R_{FB2} to provide a minimum load of typically 1mA at nominal V_{OUT} will increase the minimum switching frequency and maintain sufficient bootstrap capacitor voltage.

7.3.6 Soft-Start

The soft-start feature allows the converter to gradually reach a steady-state operating point, thereby reducing startup stresses and current surges. Upon turn-on, when V_{IN} reaches its undervoltage lock-out threshold an internal 10-µA current source charges the external capacitor at the SS pin to 2.51 V (t1 in Figure 17). The ramping voltage at SS ramps the non-inverting input of the regulation comparator and the output voltage, in a controlled manner. For proper operation, the soft-start capacitor should be no smaller than 1000 pF.

Feature Description (continued)

The LM25011 can be employed as a tracking regulator by applying the controlling voltage to the SS pin. The output voltage of the regulator tracks the applied voltage, gained up by the ratio of the feedback resistors. The applied voltage at the SS pin must be within the range of 0.5 V to 2.6 V. The absolute maximum rating for the SS pin is 3.0 V. If the tracking function causes the voltage at the FB pin to go below the thresholds for the PGD pin, the PGD pin will switch low (see the *Power Good Output (PGD)* section). An internal switch grounds the SS pin if the input voltage at VIN is below its undervoltage lock-out threshold or if the thermal shutdown activates. If the tracking function (described above) is used, the tracking voltage applied to the SS pin must be current limited to a maximum of 1 mA.

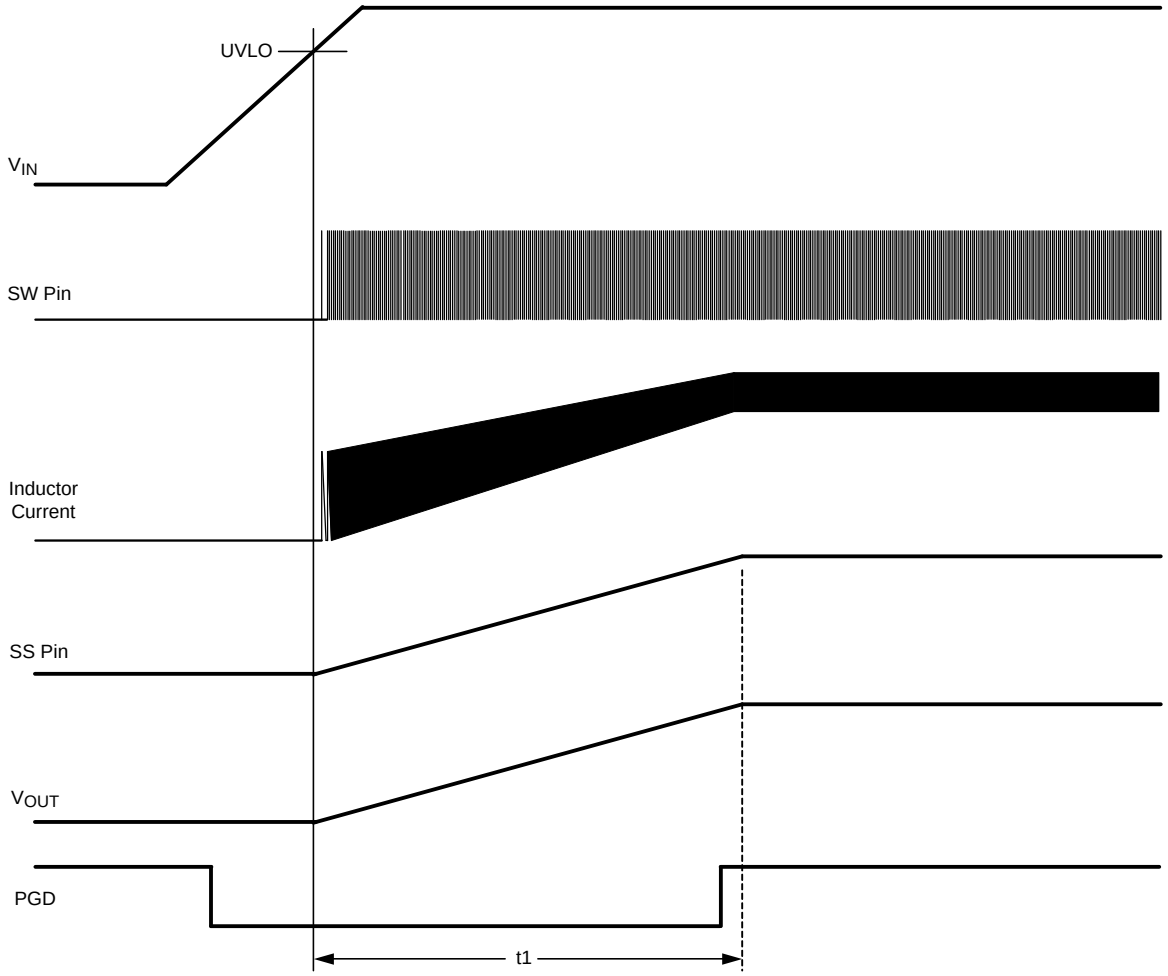


Figure 17. Startup Sequence

7.3.7 Power Good Output (PGD)

The Power Good output (PGD) indicates when the voltage at the FB pin is close to the internal 2.51-V reference voltage. The rising threshold at the FB pin for the PGD output to switch high is 95% of the internal reference. The falling threshold for the PGD output to switch low is approximately 3.3% below the rising threshold.

The PGD pin is internally connected to the drain of an N-channel MOSFET switch. An external pull-up resistor (R_{PGD}), connected to an appropriate voltage not exceeding 7 V, is required at PGD to indicate the LM25011 status to other circuitry. When PGD is low, the pin voltage is determined by the current into the pin. See Figure 7, *PGD Low Voltage vs Sink Current*.

Feature Description (continued)

Upon powering up the LM25011, the PGD pin is high until the voltage at V_{IN} reaches 2 V, at which time PGD switches low. As V_{IN} is increased, PGD stays low until the output voltage takes the voltage at the FB pin above 95% of the internal reference voltage, at which time PGD switches high. As V_{IN} is decreased (during shutdown), PGD remains high until either the voltage at the FB pin falls below approximately 92% of the internal reference or when V_{IN} falls below its lower UVLO threshold, whichever occurs first. PGD then switches low, and remains low until V_{IN} falls below 2 V, at which time PGD switches high. If the LM25011 is used as a tracking regulator (see the *Soft-Start* section), the PGD output is high as long as the voltage at the FB pin is above the thresholds mentioned above.

7.3.8 Thermal Shutdown

The LM25011 should be operated so the junction temperature does not exceed 125°C. If the junction temperature increases above that, an internal thermal shutdown circuit activates (typically) at 155°C, taking the controller to a low-power reset state by disabling the buck switch and taking the SS pin to ground. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature decreases below 135°C (typical hysteresis = 20°C), normal operation resumes.

7.4 Device Functional Modes

7.4.1 Shutdown Function

The SS pin can be used to shutdown the LM25011 by grounding the SS pin as shown in Figure 18. Releasing the pin allows normal operation to resume.

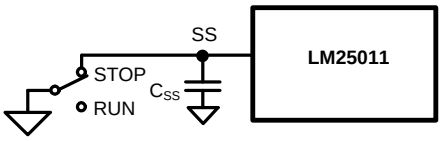


Figure 18. Shutdown Implementation

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM25011/LM25011-Q1 is a non-synchronous buck regulator designed to operate over a wide input voltage range and output current. Spreadsheet-based quick-start calculation tools and the on-line WEBENCH® software can be used to create a buck design with the bill of materials, estimated efficiency, and the complete solution cost.

8.2 Typical Application

8.2.1 LM25011 Example Circuit

The final circuit is shown in Figure 19, and its performance is shown in Figure 20 and Figure 21. The current limit measures approximately 1.62 A at V_{IN} = 8 V, and 1.69 A at V_{IN} = 36 V.

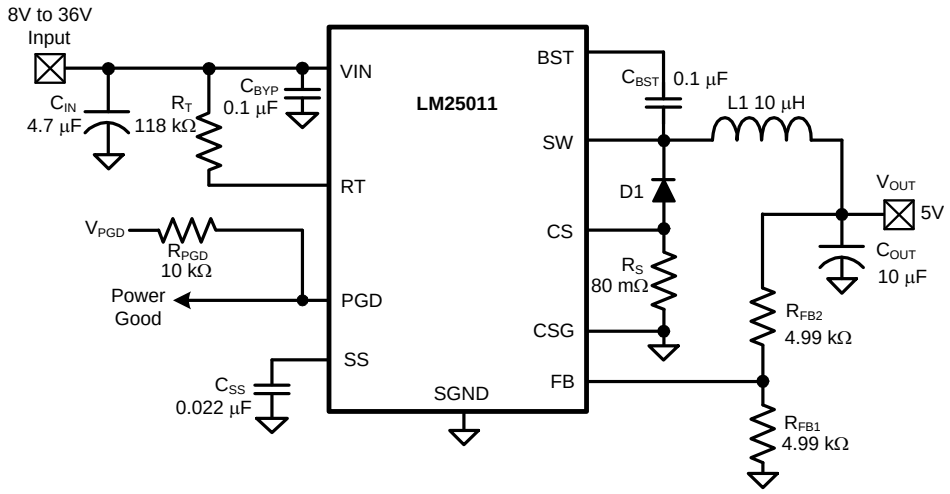


Figure 19. Example Circuit

8.2.1.1 Design Requirements

Table 1 shows the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	8 V to 36 V
Output voltage	5 V
Maximum load current ($I_{OUT(max)}$)	1.5 A
Minimum load current ($I_{OUT(min)}$)	300 mA
Switching frequency (F_{SW})	1 MHz
Soft-start time	5 ms

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM25011 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.1.2.2 External Components

The procedure for calculating the external components is illustrated with a design example using the LM25011. Referring to the *Functional Block Diagram* , the circuit is to be configured for the following specifications:

- V_{OUT} = 5 V
- V_{IN} = 8 V to 36 V
- Minimum load current for continuous conduction mode $I_{OUT(min)}$ = 300 mA
- Maximum load current $I_{OUT(max)}$ = 1.5 A
- Switching frequency (F_{SW}) = 1.0 MHz
- Soft-start time = 5 ms

R_{FB2} and R_{FB1}: These resistors set the output voltage, and their ratio is calculated from:

$$R_{FB2}/R_{FB1} = (V_{OUT} / 2.51\ V) - 1 \quad (8)$$

For this example, R_{FB2}/R_{FB1} = 0.992. R_{FB1} and R_{FB2} should be chosen from standard value resistors in the range of 1.0 kΩ to 10 kΩ which satisfy the above ratio. For this example, 4.99 kΩ is chosen for both resistors, providing a 5.02-V output.

R_T: This resistor sets the on-time and (by default) the switching frequency. First check that the desired frequency does not require an on-time or off-time shorter than the minimum allowed values (90 ns and 150, respectively). The minimum on-time occurs at the maximum input voltage. For this example:

$$t_{ON(min)} = \frac{V_{OUT}}{V_{IN(max)} \times F_S} = \frac{5V}{36V \times 1\ MHz} = 139\ ns \quad (9)$$

The minimum off-time occurs at the minimum input voltage. For this example:

$$t_{OFF(min)} = \frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)} \times F_S} = \frac{8V - 5V}{8V \times 1\ MHz} = 375\ ns \quad (10)$$

Both the on-time and off-time are acceptable because they are significantly greater than the minimum value for each. The R_T resistor is calculated from Equation 6 using the minimum input voltage:

$$R_T = \frac{5 - (8V \times 1MHz \times 15\ ns)}{1MHz \times 4.1 \times 10^{-11}} - 500\Omega = 118.5\ k\Omega \quad (11)$$

A standard value 118-kΩ resistor is selected. The minimum on-time calculates to 152 ns at V_{IN} = 36 V, and the maximum on-time calculates to 672 ns at V_{IN} = 8 V.

L1: The parameters controlled by the inductor are the inductor current ripple amplitude (I_{OR}), and the ripple voltage amplitude across the current sense resistor R_S. The minimum load current is used to determine the maximum allowable ripple to maintain continuous conduction mode (the lower peak does not reach 0 mA). This is not a requirement of the LM25011, but serves as a guideline for selecting L1. For this example, the maximum ripple current should be less than:

$$I_{OR(max)} = 2 \times I_{OUT(min)} = 600\ mA_{P-P} \quad (12)$$

For applications where the minimum load current is zero, a good starting point for allowable ripple is 20% of the maximum load current. In this case substitute 20% of $I_{OUT(max)}$ for $I_{OUT(min)}$ in Equation 12. The ripple amplitude calculated in Equation 12 is then used in Equation 13:

$$L1_{(min)} = \frac{t_{ON(min)} \times (V_{IN(max)} - V_{OUT})}{I_{OR(max)}} = 7.85\ \mu H \quad (13)$$

A standard value 10-µH inductor is chosen. Using this inductor value, the maximum ripple current amplitude, which occurs at maximum V_{IN}, calculates to 472 mA_{P-P}, and the peak current is 1736 mA at maximum load current. Ensure the selected inductor is rated for this peak current. The minimum ripple current, which occurs at minimum V_{IN}, calculates to 200 mA_{P-P}.

R_S: The minimum current limit threshold is calculated at maximum load current using the minimum ripple current calculated above. The current limit threshold is the lower peak of the inductor current waveform when in current limit (see Figure 15).

$$I_{LIM} = 1.5\ A - (0.2\ A / 2) = 1.4\ A \quad (14)$$

Current limit detection occurs when the voltage across the sense resistor (R_S) reaches the current limit threshold. To allow for tolerances, the sense resistor value is calculated using the minimum threshold specification:

$$R_S = 115\ mV / 1.4\ A = 82\ m\Omega \quad (15)$$

The next smaller standard value, 80 mΩ, is selected. The next step is to ensure that sufficient ripple voltage occurs across R_S with this value sense resistor. As mentioned in the *Ripple Requirements* section, a minimum of 15-mV_{P-P} voltage ripple is required across the R_S sense resistor during the off-time to ensure the regulation circuit operates properly. The ripple voltage is the product of the inductor ripple current amplitude and the sense resistor value. In this case, the minimum ripple voltage calculates to:

$$V_{RIPPLE} = \Delta I \times R_S = 200\ mA \times 0.080\ \Omega = 16\ mV \quad (16)$$

If the ripple voltage had calculated to less than 15 mV_{P-P}, the inductor value would have to be reduced to increase the ripple current amplitude. This would have required a recalculation of I_{LIM} and R_S in the above equations. Because the minimum requirement is satisfied in this case, no change is necessary.

The nominal current limit threshold calculates to 1.63 A. The minimum and maximum thresholds calculate to 1.44 A and 1.83 A, respectively, using the minimum and maximum limits for the current limit threshold specification. The load current is equal to the threshold current plus one-half of the ripple current. Under normal load conditions, the maximum power dissipation in R_S occurs at maximum load current, and at maximum input voltage where the on-time duty cycle is minimum. In this design example, the minimum on-time duty cycle is:

$$\text{Duty Cycle} = D = \frac{V_{OUT}}{V_{IN}} = \frac{5V}{36V} = 13.9\% \quad (17)$$

At maximum load current, the power dissipation in R_S is equal to:

$$P_{(RS)} = (1.5\ A)^2 \times 0.080\ \Omega \times (1 - 0.139) = 155\ mW \quad (18)$$

When in current limit the maximum power dissipation in R_S calculates to

$$P_{(RS)} = (1.83\ A + 0.472\ A / 4)^2 \times 0.080\ \Omega = 304\ mW \quad (19)$$

Duty cycle is not included in this power calculation because the on-time duty cycle is typically <5% when in current limit.

C_{OUT}: The output capacitor should typically be no smaller than 3.3 µF, although that is dependent on the frequency and the desired output characteristics. C_{OUT} should be a low ESR good-quality ceramic capacitor. Experimentation is usually necessary to determine the minimum value for C_{OUT}, as the nature of the load may require a larger value. A load which creates significant transients requires a larger value for C_{OUT} than a non-varying load.

C_{IN} and C_{BYP}: The purpose of C_{IN} is to supply most of the switch current during the on-time, and limit the voltage ripple at V_{IN}, because it is assumed the voltage source feeding V_{IN} has some amount of source impedance. When the buck switch turns on, the current into V_{IN} suddenly increases to the lower peak of the inductor ripple current, then ramps up to the upper peak, and finally drops to zero at turn-off. The average current during the on-time is the average load current. For a worst case calculation, C_{IN} must supply this average load current during the maximum on-time, without letting the voltage at the VIN pin drop below a minimum operating level of 5.5 V. For this exercise 0.5 V is chosen as the maximum allowed input ripple voltage. Using the maximum load current, the minimum value for C_{IN} is calculated from:

$$C_{IN} = \frac{I_{OUT(max)} \times t_{ON(max)}}{\Delta V} = \frac{1.5A \times 672\ ns}{0.5V} = 2.02\ \mu F \quad (20)$$

where t_{ON} is the maximum on-time, and ΔV is the allowable ripple voltage at V_{IN}. The purpose of C_{BYP} is to minimize transients and ringing due to long lead inductance leading to the VIN pin. A low ESR 0.1-µF ceramic chip capacitor is recommended, and C_{BYP} must be located close to the VIN and SGND pins.

C_{BST}: The recommended value for C_{BST} is 0.1 µF. A high-quality ceramic capacitor with low ESR is recommended as C_{BST} supplies a surge current to charge the buck switch gate at each turn-on. A low ESR also helps ensure a complete recharge during each off-time.

C_{SS}: The capacitor at the SS pin determines the soft-start time, that is, the time for the output voltage to reach its final value (t1 in Figure 17). For a soft-start time of 5 ms, the capacitor value is determined from the following:

$$C_{SS} = \frac{5\ ms \times 10\ \mu A}{2.51V} = 0.02\ \mu F \quad (21)$$

D1: A Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high-speed transitions at the SW pin may affect the regulator operation due to the reverse recovery transients of the diode. The diode must be rated for the maximum input voltage, the maximum load current, and the peak current which occurs when the current limit and maximum ripple current are reached simultaneously. The average power dissipation of the diode is calculated from:

$$P_{D1} = V_F \times I_{OUT} \times (1 - D) \quad (22)$$

where V_F is the forward voltage drop of the diode, and D is the on-time duty cycle.

8.2.1.3 Application Curves

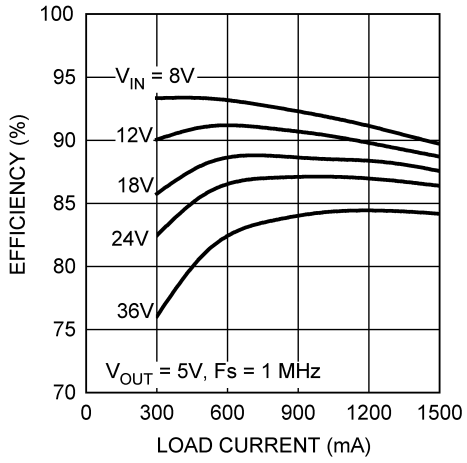


Figure 20. Efficiency (Circuit of Figure 19)

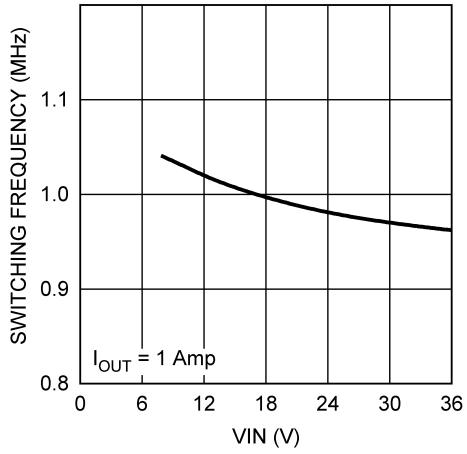


Figure 21. Frequency vs V_{IN} (Circuit of Figure 19)

8.2.2 Output Ripple Control

High frequency applications of the LM25011 or LM25011A are likely to require more ripple voltage than is internally generated across the R_S resistor. Additional ripple can be supplied to the FB pin, in phase with the switching waveform at the SW pin, for proper operation. The required ripple can be supplied from ripple generated at V_{OUT}, through the feedback resistors, as described in *Option A: Lowest Cost Configuration* . *Option B: Intermediate V_{OUT} Ripple Configuration* and *Option C: Minimum V_{OUT} Ripple Configuration* use one or two additional components to provide ripple at the FB pin with lower output ripple at V_{OUT}.

The amount of additional ripple voltage needed at the FB pin is typically in the range of 30 mV to 150 mV. Higher switching frequencies or higher inductor values (less ripple current) require more external ripple voltage injected at the FB pin. Insufficient ripple voltage will result in frequency jitter. For a particular application, add only as much ripple as needed to stabilize the switching frequency over the required input voltage.

8.2.2.1 Option A: Lowest Cost Configuration

In this configuration R1 is installed in series with the output capacitor (C_{OUT}) as shown in Figure 22. The ripple current of the inductor passes through R1, generating a ripple voltage at V_{OUT}. The minimum value for R1 is:

$$R1 = \frac{V_{RIPPLE} \times (R_{FB2} + R_{FB1})}{\Delta I \times R_{FB1}} \tag{23}$$

where ΔI is the minimum ripple current amplitude, which occurs at minimum V_{IN}, and V_{RIPPLE} is the peak to peak ripple voltage injected at the FB pin.

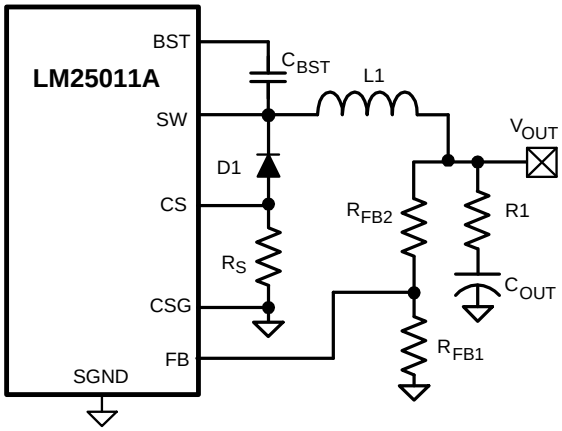


Figure 22. Option A – Lowest Cost Ripple Configuration

8.2.2.2 Option B: Intermediate V_{OUT} Ripple Configuration

This configuration generates less ripple at V_{OUT} than Option A by the addition of capacitor (Cff) as shown in Figure 23.

Because the output ripple is passed by Cff to the FB pin with little or no attenuation, the R1 value and V_{OUT} ripple can be smaller than in Option A. The minimum value for R1 is calculated from:

$$R1 = \frac{V_{RIPPLE}}{\Delta I} \tag{24}$$

where ΔI is the minimum ripple current amplitude, which occurs at minimum V_{IN}, and V_{RIPPLE} is the peak-to-peak ripple voltage injected at the FB pin. The minimum value for Cff is calculated from:

$$Cff > \frac{3 \times t_{ON(max)}}{R_{FB1} // R_{FB2}} \tag{25}$$

where $t_{ON(max)}$ is the maximum on-time (at minimum V_{IN}), and $R_{FB1}//R_{FB2}$ is the parallel equivalent of the feedback resistors.

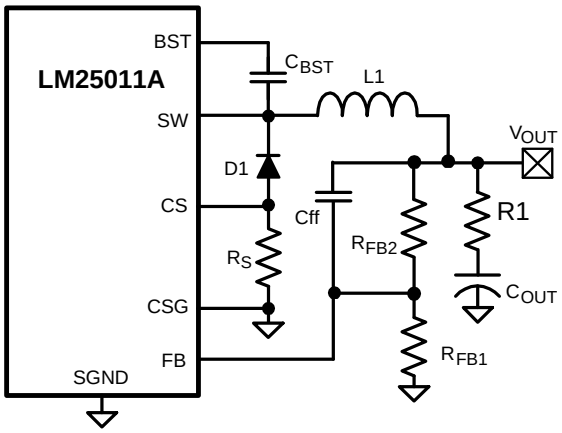


Figure 23. Option B – Intermediate Ripple Configuration

8.2.2.3 Option C: Minimum V_{OUT} Ripple Configuration

In some applications, the V_{OUT} ripple induced by series resistor R1 may not be acceptable. When low V_{OUT} ripple is required, an external ripple circuit, as shown in Figure 24, can be used to provide the required ripple at the FB pin.

1. The time constant Rr × Cr should be more than 8 to 10 times the switching period to generate a triangular waveform at the junction of Rr, Cr and Cac.
2. The minimum ripple at FB (at minimum V_{IN}) is equal to: $V_{RIPPLE} = (V_{IN(min)} - V_{OUT}) \times T_{ON(max)} / (Rr \times Cr)$.
3. The ripple capacitor Cr should much smaller than the ac coupling capacitor Cac. Typically Cac = 100 nF, Cr = 1 nF, and Rr is chosen to satisfy conditions 1 and 2 above.

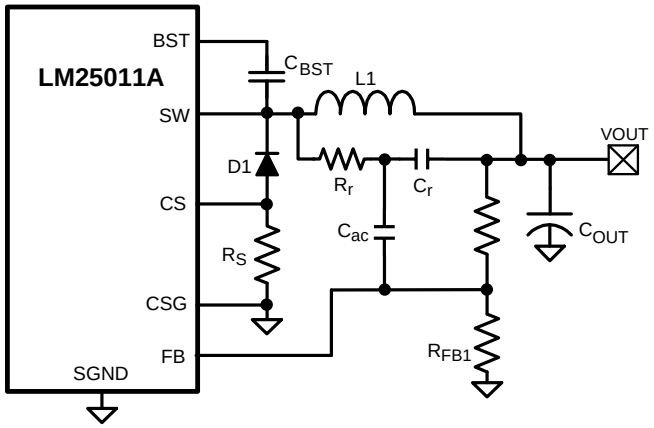


Figure 24. Option C: Minimum Output Ripple Configuration

9 Power Supply Recommendations

The LM25011 is designed to operate with an input power supply capable of supplying a voltage range between 6 V and 42 V. The power supply should be well regulated and capable of supplying sufficient current to the regulator during peak load operation. Also, like in all applications, the power supply source impedance must be small compared to the module input impedance to maintain the stability of the converter.

10 Layout

10.1 Layout Guidelines

The LM25011 regulation and current limit comparators are very fast, and respond to short-duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all of the components must be as close as possible to their associated pins. The two major current loops conduct currents which switch very fast, and therefore those loops must be as small as possible to minimize conducted and radiated EMI. The first loop is formed by C_{IN}, through the VIN to SW pins, L_{IND}, C_{OUT}, and back to C_{IN}. The second current loop is formed by R_S, D1, L_{IND}, C_{OUT}, and back to R_S. The ground connection from CSG to the ground end of C_{IN} should be as short and direct as possible.

10.2 Layout Example

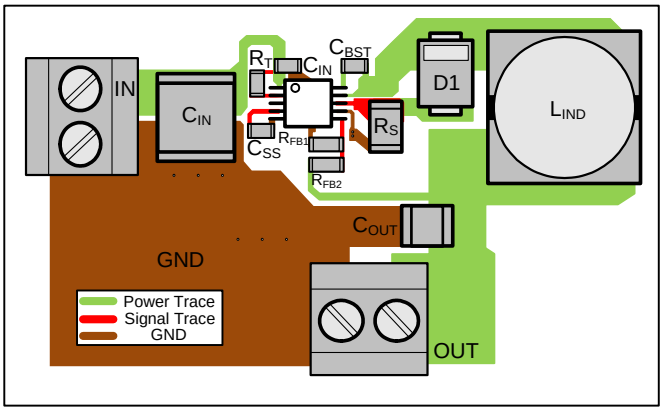


Figure 25. Typical Layout

10.3 Power Dissipation

The power dissipation within the LM25011 can be approximated by determining the total conversion loss ($P_{IN} – P_{OUT}$) of the circuit, and then subtracting the power losses in the free-wheeling diode, the sense resistor, and the inductor. The power loss in the diode is approximately:

$$P_{D1} = I_{OUT} \times V_F \times (1 – D) \quad (26)$$

where I_{OUT} is the load current, V_F is the forward voltage drop of the diode, and D is the on-time duty cycle. The power loss in the sense resistor is:

$$P_{RS} = (I_{OUT})^2 \times R_S \times (1 – D) \quad (27)$$

The power loss in the inductor is approximately:

$$P_{L1} = I_{OUT}{}^2 \times R_L \times 1.1 \quad (28)$$

where R_L is the dc resistance of the inductor, and the 1.1 factor is an approximation for the ac losses. If it is expected that the internal dissipation of the LM25011 will produce excessive junction temperatures during normal operation, good use of the ground plane of the PC board can help to dissipate heat. Additionally the use of wide PC board traces, where possible, can help conduct heat away from the IC pins. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

11 デバイスおよびドキュメントのサポート

11.1 WEBENCHツールによるカスタム設計

ここをクリックすると、LM25011デバイスを使用するカスタム設計を WEBENCH® Power Designerにより作成できます。

1. 最初に、V_{IN}、V_{OUT}、I_{OUT}の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化し、この設計と、テキサス・インスツルメンツによる他の可能なソリューションとを比較します。
3. WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格や部品の在庫情報と併せて参照できます。
4. ほとんどの場合、次の操作も実行できます。
   - 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
   - 熱シミュレーションを実行し、基板の熱特性を把握する。
   - カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
   - 設計のレポートをPDFで印刷し、同僚と設計を共有する。
5. WEBENCHツールの詳細は、www.ti.com/webenchでご覧になれます。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LM25011	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM25011-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 商標

WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25011AMY	ACTIVE	HVSSOP	DGQ	10	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SN9B	Samples
LM25011AMYE	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SN9B	Samples
LM25011AMYX	ACTIVE	HVSSOP	DGQ	10	3500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SN9B	Samples
LM25011AQ1MY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SZZA	Samples
LM25011AQ1MYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SZZA	Samples
LM25011MY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SVUB	Samples
LM25011MYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SVUB	Samples
LM25011Q1MY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SZFB	Samples
LM25011Q1MYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SZFB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM25011, LM25011-Q1 :

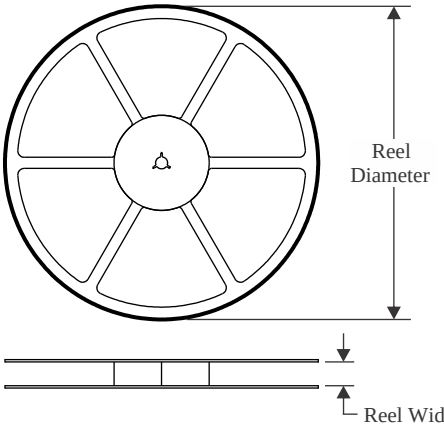
- Catalog : LM25011
- Automotive : LM25011-Q1

NOTE: Qualified Version Definitions:

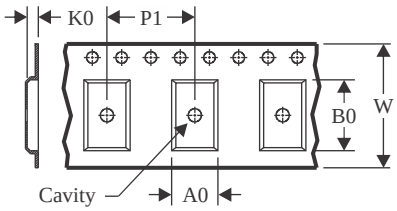
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

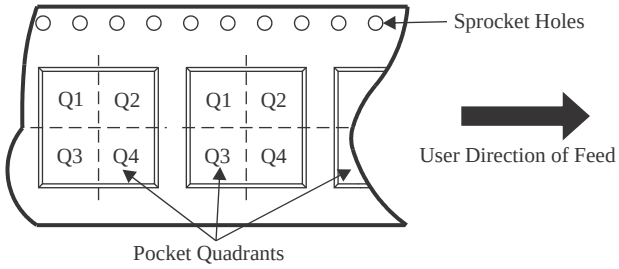


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

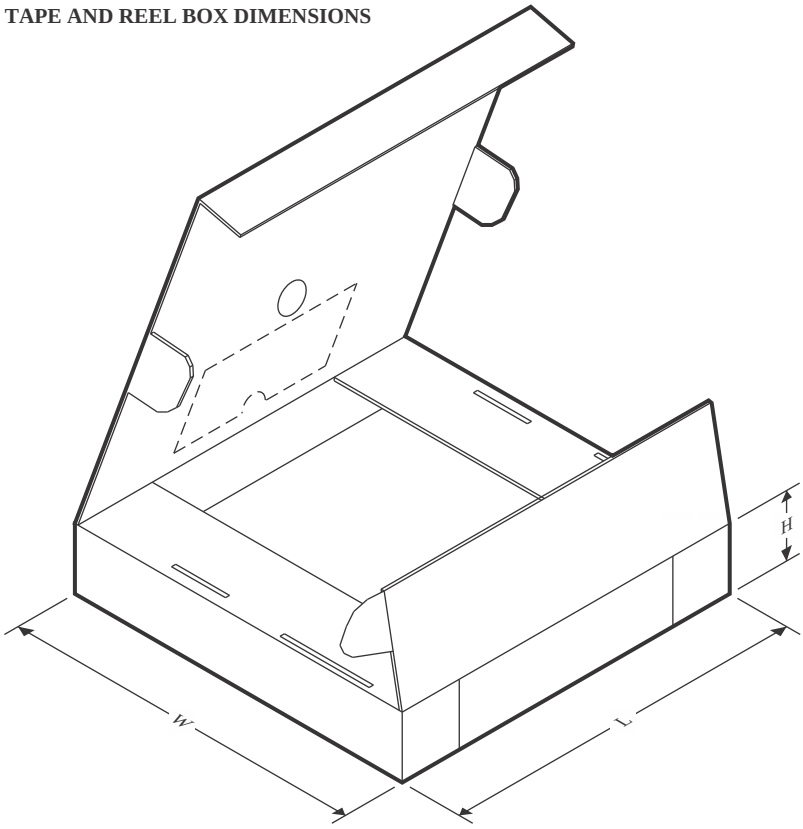
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25011AMY	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25011AMYE	HVSSOP	DGQ	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25011AMYX	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25011AQ1MY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25011AQ1MYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25011MY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25011MYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25011Q1MY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25011Q1MYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

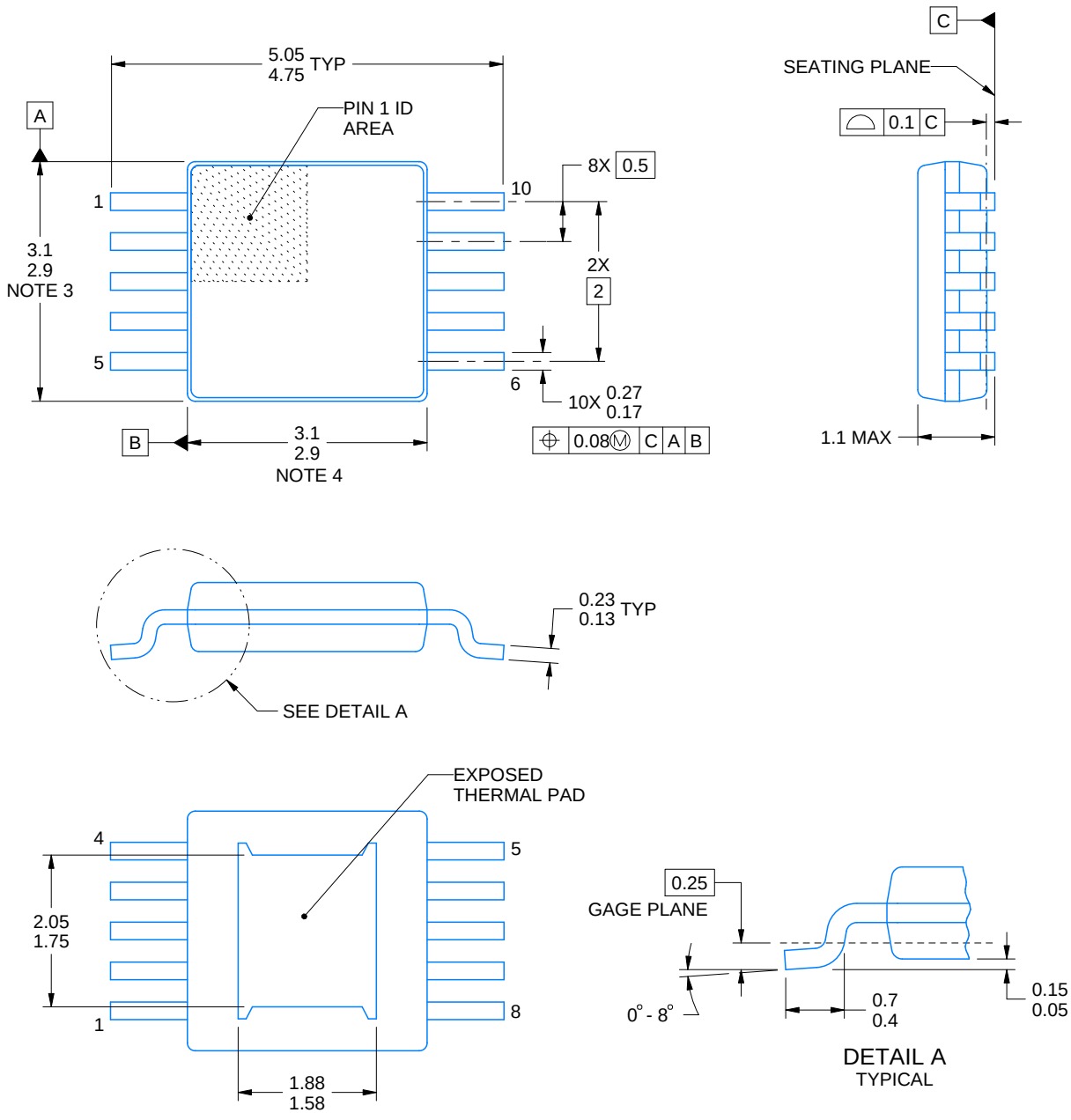
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25011AMY	HVSSOP	DGQ	10	1000	208.0	191.0	35.0
LM25011AMYE	HVSSOP	DGQ	10	250	208.0	191.0	35.0
LM25011AMYX	HVSSOP	DGQ	10	3500	356.0	356.0	36.0
LM25011AQ1MY/NOPB	HVSSOP	DGQ	10	1000	208.0	191.0	35.0
LM25011AQ1MYX/NOPB	HVSSOP	DGQ	10	3500	356.0	356.0	36.0
LM25011MY/NOPB	HVSSOP	DGQ	10	1000	208.0	191.0	35.0
LM25011MYX/NOPB	HVSSOP	DGQ	10	3500	356.0	356.0	36.0
LM25011Q1MY/NOPB	HVSSOP	DGQ	10	1000	208.0	191.0	35.0
LM25011Q1MYX/NOPB	HVSSOP	DGQ	10	3500	356.0	356.0	36.0

PACKAGE OUTLINE

DGQ0010A

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



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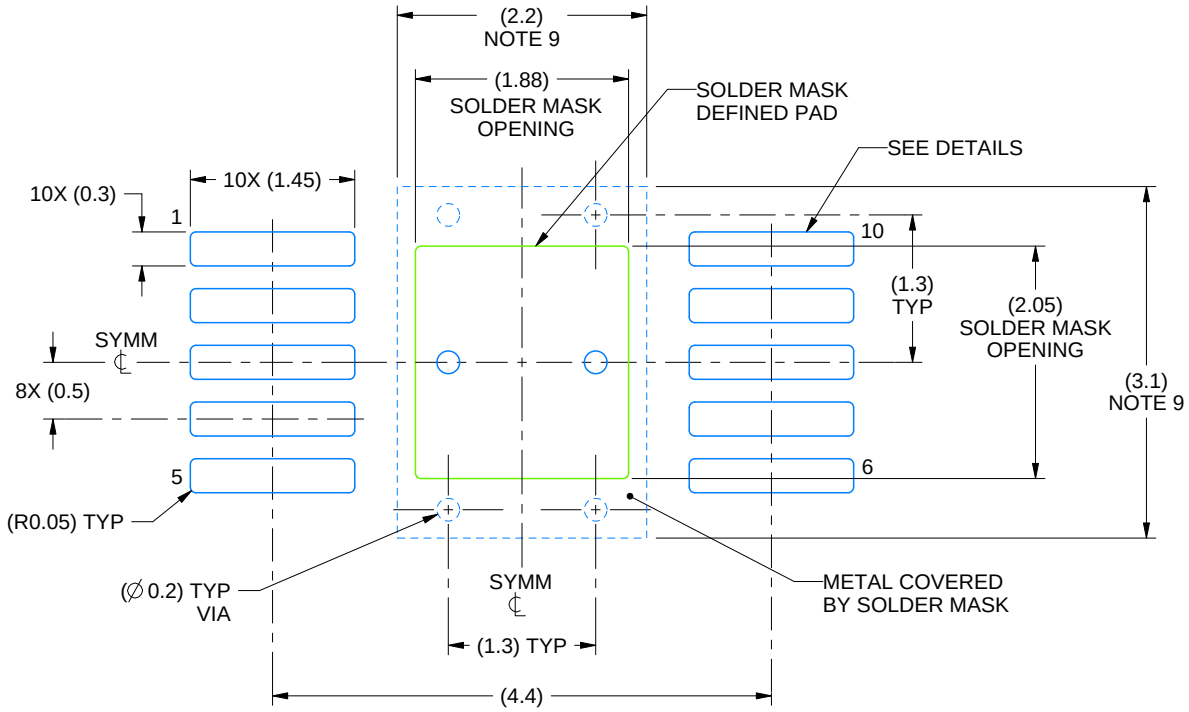
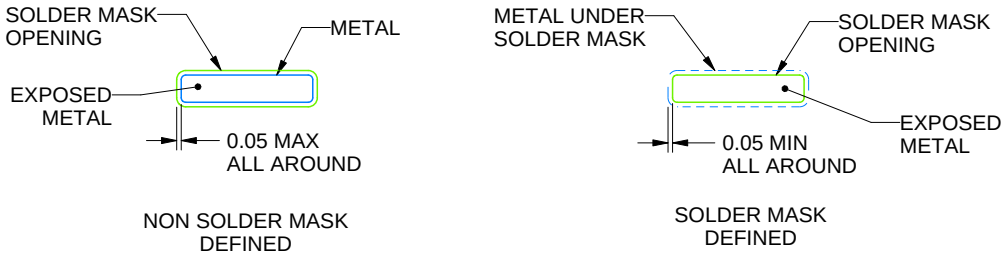
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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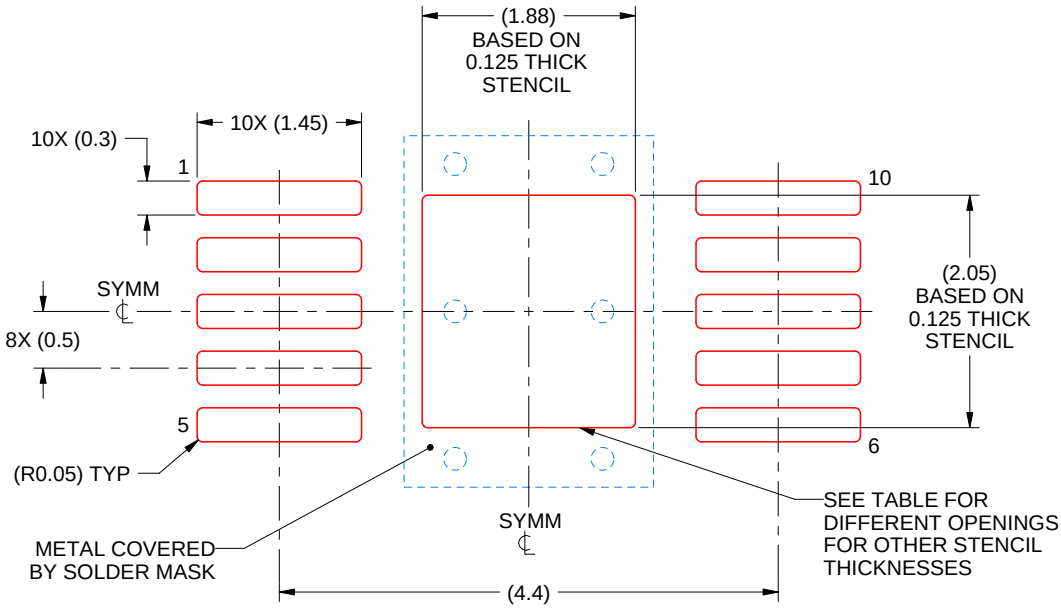
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.29
0.125	1.88 X 2.05 (SHOWN)
0.150	1.72 X 1.87
0.175	1.59 X 1.73

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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