# ISO782xLL 高性能、8000$V_{PK}$強化絶縁デュアルLVDSバッファ

## 1 特長

- TIA/EIA-644-A LVDS標準に準拠
- 信号速度: 最大100Mbps
- 広い電源電圧範囲: 2.25V～5.5V
- 広い温度範囲: 周囲温度-55℃～+125℃
- 低消費電力: 100Mbpsでチャネルごとの標準値
  - 9.3mA (ISO7820LL)
  - 9.5mA (ISO7821LL)
- 低い伝搬遅延: 17ns (標準値)
- 業界最先端のCMTI (最小値): ±100kV/μs
- 堅牢な電磁気互換性(EMC)
- システム・レベルでのESD、EFT、サージ耐性
- 低い放射
- 絶縁バリアの寿命: 40年以上
- ワイド・ボディ、および超ワイド・ボディの SOIC-16パッケージ・オプション
- 絶縁サージ耐久電圧12800$V_{PK}$
- 安全関連の認定
  - 8000$V_{PK}$の、DIN V VDE V 0884-10 (VDE V 0884-10):2006-12準拠の強化絶縁
  - UL 1577に準拠した絶縁耐圧: 5700$V_{RMS}$ (1分間)
  - CSA Component Acceptance Notice 5A、IEC-60950-1、およびIEC 60601-1最終機器標準
  - EN 61010-1およびEN 60950-1準拠のTUV認定
  - GB4943.1-2011 CQC認定
  - すべての認定は計画中

## 2 アプリケーション

- モーター制御
- 試験/測定機器
- 産業用オートメーション
- 医療用機器
- 通信システム

## 3 概要

ISO782xLLファミリのデバイスは高性能の絶縁されたデュアルLVDSバッファで、8000$V_{PK}$の絶縁耐圧があります。このデバイスは、高い電磁気耐性、低い放射、低い消費電力を実現し、同時にLVDSバス信号が絶縁されています。それぞれの絶縁チャネルにはLVDS受信および送信バッファがあり、二酸化シリコン($SiO_2$)絶縁バリアにより分離されています。

ISO7820LLデバイスには、2つの順方向チャネルがあります。ISO7821LLデバイスには、1つの順方向チャネルと1つの逆方向チャネルがあります。

革新的なチップ設計およびレイアウト技法により、ISO782xLLファミリのデバイスは電磁環境適合性が大幅に強化されているため、システム・レベルのESD、EFT、サージ、および放射に関するコンプライアンスを簡単に実現できます。

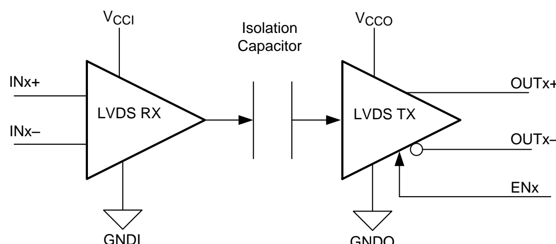
ISO782xLLファミリのデバイスは、16ピンのSOICワイド・ボディ(DW)パッケージと、超ワイド・ボディ(DWW)パッケージで供給されます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| ISO7820LL<br>ISO7821LL | DW (16) | 10.30mm×7.50mm |
| | DWW (16) | 10.30mm×14.00mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

**概略回路図**

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$V_{CCI}$およびGNDIは、それぞれ入力チャネルの電源およびグランド接続です。

$V_{CCO}$およびGNDOは、それぞれ出力チャネルの電源およびグランド接続です。

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| **2016年3月発行のものから更新** | **Page** |
|---|---|
| • データシートの完全版をリリース、デバイスの状態を製品プレビューから量産データへ 変更 | 1 |


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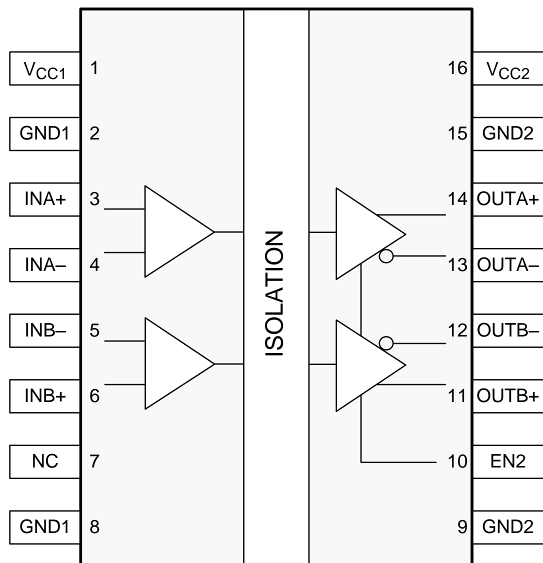
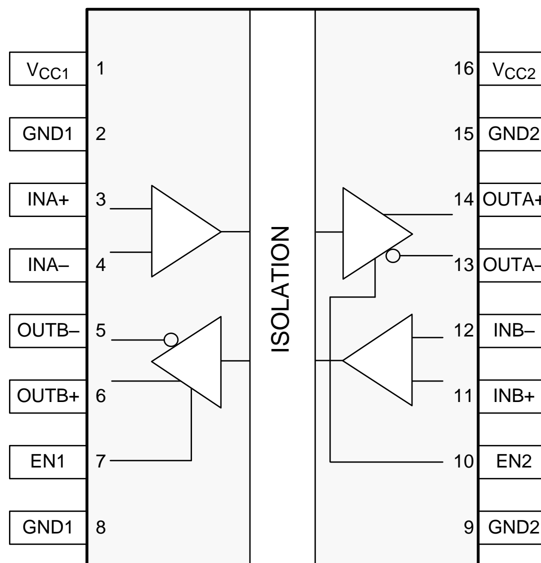
# 5 Pin Configuration and Functions

**ISO7820LL DW and DWW Packages**
**16-Pin SOIC**
**Top View**




**ISO7821LL DW and DWW Packages**
**16-Pin SOIC**
**Top View**




## Pin Functions

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| | ISO7820LL | ISO7821LL | | |
| EN1 | — | 7 | I | Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high impedance state when EN1 is low. |
| EN2 | 10 | 10 | I | Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high impedance state when EN2 is low. |
| GND1 | 2 | 2 | — | Ground connection for $V_{CC1}$ |
| | 8 | 8 | | |
| GND2 | 9 | 9 | — | Ground connection for $V_{CC2}$ |
| | 15 | 15 | | |
| INA+ | 3 | 3 | I | Positive differential input, channel A |
| INA– | 4 | 4 | I | Negative differential input, channel A |
| INB+ | 6 | 11 | I | Positive differential input, channel B |
| INB– | 5 | 12 | I | Negative differential input, channel B |
| NC | 7 | — | — | Not connected |
| OUTA+ | 14 | 14 | O | Positive differential output, channel A |
| OUTA– | 13 | 13 | O | Negative differential output, channel A |
| OUTB+ | 11 | 6 | O | Positive differential output, channel B |
| OUTB– | 12 | 5 | O | Negative differential output, channel B |
| $V_{CC1}$ | 1 | 1 | — | Power supply, side 1, $V_{CC1}$ |
| $V_{CC2}$ | 16 | 16 | — | Power supply, side 2, $V_{CC2}$ |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCx}$ | Supply voltage[2] | $V_{CC1}$, $V_{CC2}$ | –0.5 | 6 | V |
| V | Voltage on input, output, and enable pins | OUTx, INx, ENx | –0.5 | $V_{CCx}$ + 0.5[3] | V |
| $I_O$ | Maximum current through OUTx pins | | –20 | 20 | mA |
| $T_J$ | Junction temperature | | –55 | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±4500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply voltage | | 2.25 | 3.3 | 5.5 | V |
| $\|V_{ID}\|$ | Magnitude of RX input differential voltage | Driven with voltage sources on RX pins | 100 | | 600 | mV |
| $V_{IC}$ | RX input common-mode voltage | $V_{CC1}$, $V_{CC2}$ ≥ 3 V | 0.5 $\|V_{ID}\|$ | | 2.4 – 0.5 $\|V_{ID}\|$ | V |
| | | $V_{CC1}$, $V_{CC2}$ < 3 V | 0.5 $\|V_{ID}\|$ | | $V_{CCx}$ – 0.6 – 0.5 $\|V_{ID}\|$ | V |
| $R_L$ | TX far end differential termination | | | 100 | | Ω |
| DR | Signaling rate | | 0 | | 100 | Mbps |
| $T_A$ | Ambient temperature | | –55 | 25 | 125 | °C |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## 6.4 Thermal Information

| THERMAL METRIC[(1)] | | ISO7820LL ISO7821LL | | UNIT |
|---|---|---|---|---|
| | | DW (SOIC) | DWW (SOIC) | |
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 82 | 84.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 44.6 | 46.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 46.6 | 55.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 17.8 | 18.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 46.1 | 54.5 | °C/W |
| $R_{\theta JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Power Ratings

$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 5$ pF, input a 50-MHz 50% duty-cycle square wave, EN1 = EN2 = 5.5 V, $R_L = 100$-Ω differential

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO7821LL** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | | | | 156 | mW |
| $P_{D1}$ | Maximum power dissipation (side 1) | | | | 78 | mW |
| $P_{D2}$ | Maximum power dissipation (side 2) | | | | 78 | mW |
| **ISO7820LL** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | | | | 152 | mW |
| $P_{D1}$ | Maximum power dissipation (side 1) | | | | 36 | mW |
| $P_{D2}$ | Maximum power dissipation (side 2) | | | | 116 | mW |

## 6.6 Insulation Specifications

over operating free-air temperature range (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | SPECIFICATION | | UNIT |
|---|---|---|---|---|---|
| | | | DW | DWW | |
| **GENERAL** | | | | | |
| CLR | External clearance[1] | Shortest terminal-to-terminal distance through air | >8 | >14.5 | mm |
| CPG | External creepage[1] | Shortest terminal-to-terminal distance across the package surface | >8 | >14.5 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | >21 | >21 | μm |
| CTI | Tracking resistance (comparative tracking index) | DIN EN 60112 (VDE 0303–11); IEC 60112; UL 746A | >600 | >600 | V |
| | Material group | According to IEC 60664-1 | I | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 600 $V_{RMS}$ | I–IV | I–IV | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I–III | I–IV | |
| **DIN V VDE V 0884–10 (VDE V 0884–10):2006–12**[2] | | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 2121 | 2828 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum isolation working voltage | AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test; see Figure 1 and Figure 2 | 1500 | 2000 | $V_{RMS}$ |
| | | DC voltage | 2121 | 2828 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$<br>t = 60 s (qualification)<br>t = 1 s (100% production) | 8000 | 8000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage[3] | Test method per IEC 60065, 1.2/50 µs waveform,<br>$V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification) | 8000 | 8000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge[4] | Method a: After I/O safety test subgroup 2/3,<br>$V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s;<br>$V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$ (DW) and 3394 $V_{PK}$ (DWW), $t_m = 10$ s | ≤5 | ≤5 | pC |
| | | Method a: After environmental tests subgroup 1,<br>$V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s;<br>$V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$ (DW) and 4525 $V_{PK}$ (DWW), $t_m = 10$ s | ≤5 | ≤5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test)<br>$V_{ini} = V_{IORM}$, $t_{ini} = 1$ s;<br>$V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$ (DW) and 5303 $V_{PK}$ (DWW), $t_m = 1$ s | ≤5 | ≤5 | |
| $C_{IO}$ | Barrier capacitance, input to output[5] | $V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz | ~0.7 | ~0.7 | pF |
| $R_{IO}$ | Isolation resistance, input to output[5] | $V_{IO}$ = 500 V, $T_A$ = 25°C | $>10^{12}$ | $>10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | $>10^{11}$ | $>10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | $>10^{9}$ | $>10^{9}$ | |
| | Pollution degree | | 2 | 2 | |
| | Climatic category | | 55/125/21 | 55/125/21 | |
| **UL 1577** | | | | | |
| $V_{ISO}$ | Withstanding isolation voltage | $V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 s (qualification);<br>$V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$,<br>t = 1 s (100% production) | 5700 | 5700 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.


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## 6.7 Safety-Related Certifications

| VDE | CSA | UL | CQC | TUV |
|---|---|---|---|---|
| Plan to certify according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01 | Plan to certify under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 | Plan to certify according to UL 1577 Component Recognition Program | Plan to certify according to GB 4943.1-2011 | Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/ A12:2011/A2:2013 |
| Reinforced insulation Maximum transient isolation voltage, 8000 $V_{PK}$; Maximum repetitive peak isolation voltage, 2121 $V_{PK}$ (DW), 2828 $V_{PK}$ (DWW); Maximum surge isolation voltage, 8000 $V_{PK}$ | Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 $V_{RMS}$ (DW package) and 1450 $V_{RMS}$ (DWW package) max working voltage (pollution degree 2, material group I);<br>2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 $V_{RMS}$ (354 $V_{PK}$) max working voltage (DW package) | Single protection, 5700 $V_{RMS}$ | Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 $V_{RMS}$ maximum working voltage | 5700 $V_{RMS}$ Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 $V_{RMS}$ (DW package) and 1000 $V_{RMS}$ (DWW package)<br>5700 $V_{RMS}$ Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/ A12:2011/A2:2013 up to working voltage of 800 $V_{RMS}$ (DW package) and 1450 $V_{RMS}$ (DWW package) |
| Certification planned | Certification planned | Certification planned | Certification planned | Certification planned |

## 6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DW PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 82°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 3 | | | 277 | mA |
| | | $R_{\theta JA}$ = 82°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 3 | | | 423 | |
| | | $R_{\theta JA}$ = 82°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 3 | | | 554 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 82°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 5 | | | 1524 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |
| **DWW PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 84.6°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 4 | | | 269 | mA |
| | | $R_{\theta JA}$ = 84.6°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 4 | | | 410 | |
| | | $R_{\theta JA}$ = 84.6°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 4 | | | 537 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 84.6°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6 | | | 1478 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* is that of a device installed on a High-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## 6.9 DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IN(EN)}$ | Leakage Current on ENx pins | Internal pullup on ENx pins | | 13 | 40 | µA |
| $V_{CC+(UVLO)}$ | Positive-going undervoltage-lockout (UVLO) threshold | | | | 2.25 | V |
| $V_{CC-(UVLO)}$ | Negative-going UVLO threshold | | 1.7 | | | V |
| $V_{HYS(UVLO)}$ | UVLO threshold hysteresis | | | 0.2 | | V |
| $V_{EN(ON)}$ | EN pin turn-on threshold | | | | 0.7 $V_{CCx}$ | V |
| $V_{EN(OFF)}$ | EN pin turn-off threshold | | 0.3 $V_{CCx}$ | | | V |
| $V_{EN(HYS)}$ | EN pin threshold hysteresis | | | 0.1 $V_{CCx}$ | | V |
| CMTI | Common-mode transient immunity | $V_I = V_{CCI}$ [(1)] or 0 V; $V_{CM}$ = 1000 V; see Figure 25 | 100 | 120 | | kV/µs |
| **LVDS TX** | | | | | | |
| $\|V_{OD}\|$ | TX DC output differential voltage | $R_L$ = 100 Ω, See Figure 26 | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in TX DC output differential between logic 1 and 0 states | $R_L$ = 100 Ω, see Figure 26 | –10 | 0 | 10 | mV |
| $V_{OC}$ | TX DC output common mode voltage | $R_L$ = 100 Ω, see Figure 26 | 1.125 | 1.2 | 1.375 | V |
| $\Delta V_{OC}$ | TX DC common mode voltage difference | $R_L$ = 100 Ω, see Figure 26 | –25 | 0 | 25 | mV |
| $I_{OS}$ | TX output short circuit current through OUTx | OUTx = 0 | | | 10 | mA |
| | | OUTxP = OUTxM | | | 10 | |
| $I_{OZ}$ | TX output current when in high impedance | ENx = 0, OUTx from 0 to $V_{CC}$ | –5 | | 5 | µA |
| $C_{OUT}$ | TX output pad capacitance on OUTx at 1 MHz | DW package: ENx = 0, DC offset = $V_{CC}$ / 2, Swing = 200 mV, f = 1 MHz | | 10 | | pF |
| | | DWW package: ENx = 0, DC offset = $V_{CC}$ / 2, Swing = 200 mV, f = 1 MHz | | 10 | | |
| **LVDS RX** | | | | | | |
| $V_{IC}$ | RX input common mode voltage | $V_{CC1}$, $V_{CC2}$ ≥ 3 V | 0.5 $\|V_{ID}\|$ | 1.2 | 2.4 – 0.5 $\|V_{ID}\|$ | V |
| | | $V_{CC1}$, $V_{CC2}$ < 3 V | 0.5 $\|V_{ID}\|$ | 1.2 | $V_{CCx}$ – 0.6 – 0.5 $\|V_{ID}\|$ | |
| $V_{IT1}$ | Positive going RX input differential threshold | Across $V_{IC}$ | | | 50 | mV |
| $V_{IT2}$ | Negative going RX input differential threshold | Across $V_{IC}$ | –50 | | | mV |
| $I_{INx}$ | Input current on INx | From 0 to $V_{CCx}$ (each input independently) | | 10 | 20 | µA |
| $I_{INxP} - I_{INxM}$ | Input current balance | From 0 to $V_{CCx}$ | –6 | | 6 | µA |
| $C_{IN}$ | RX input pad capacitance on INx at 1 MHz | DW package: DC offset = 1.2 V, Swing = 200 mV, f = 1 MHz | | 6.6 | | pF |
| | | DWW package: DC offset = 1.2 V, Swing = 200 mV, f = 1 MHz | | 7.5 | | |

(1) $V_{CCI}$ = Input-side $V_{CCx}$; $V_{CCO}$ = Output-side $V_{CCx}$.


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### 6.10 DC Supply Current Characteristics

(over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO7821LL** | | | | | | | |
| $I_{CC1}$ $I_{CC2}$ | Supply current side 1 and side 2 | 2.25 V < $V_{CC1}$, $V_{CC2}$ < 3.6 V | EN1 = EN2 = 0, OUTx floating, $V_{ID}$ ≥ 50 mV | | 2.2 | 3.3 | mA |
| | | | EN1 = EN2 = 0, OUTx floating, $V_{ID}$ ≤ –50 mV | | 3.4 | 5.1 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID}$ ≥ 50 mV | | 6.1 | 9.2 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID}$ ≤ –50 mV | | 7.4 | 11.1 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 1 Mbps | | 6.7 | 10.2 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 50 Mbps | | 7.4 | 11.5 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 100 Mbps | | 8.3 | 12.5 | |
| | | 4.5 V < $V_{CC1}$, $V_{CC2}$ < 5.5 V | EN1 = EN2 = 0, OUTx floating, $V_{ID}$ ≥ 50 mV | | 2.2 | 3.4 | |
| | | | EN1 = EN2 = 0, OUTx floating, $V_{ID}$ ≤ –50 mV | | 3.5 | 5.2 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID}$ ≥ 50 mV | | 6.4 | 9.8 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID}$ ≤ –50 mV | | 7.8 | 11.7 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 1 Mbps | | 7.1 | 10.8 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 50 Mbps | | 8.1 | 12.1 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 100 Mbps | | 9.5 | 14.1 | |
| **ISO7820LL** | | | | | | | |
| $I_{CC1}$ | Supply current side 1 | 2.25 V < $V_{CC1}$, $V_{CC2}$ < 3.6 V | EN1 = EN2 = 0, OUTx floating, $V_{ID}$ ≥ 50 mV | | 2.7 | 4.3 | mA |
| | | | EN1 = EN2 = 0, OUTx floating, $V_{ID}$ ≤ –50 mV | | 5.3 | 7.9 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID}$≥ 50 mV | | 2.7 | 4.2 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID}$ ≤ –50 mV | | 5.2 | 8 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 1 Mbps | | 4 | 6.1 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 50 Mbps | | 4.1 | 6.2 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 100 Mbps | | 4.3 | 6.4 | |
| | | 4.5 V < $V_{CC1}$, $V_{CC2}$ < 5.5 V | EN1 = EN2 = 0, OUTx floating, $V_{ID}$ ≥ 50 mV | | 2.8 | 4.4 | |
| | | | EN1 = EN2 = 0, OUTx floating, $V_{ID}$ ≤ –50 mV | | 5.5 | 8.2 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID}$ ≥ 50 mV | | 2.9 | 4.5 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID}$ ≤ –50 mV | | 5.5 | 8.2 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 1 Mbps | | 4.2 | 6.3 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 50 Mbps | | 4.3 | 6.4 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 100 Mbps | | 4.5 | 6.6 | |

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## DC Supply Current Characteristics (continued)

(over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO7820LL (continued)** | | | | | | | |
| $I_{CC2}$ | Supply current side 2 | $2.25\ V < V_{CC1}$, $V_{CC2} < 3.6\ V$ | EN1 = EN2 = 0, OUTx floating, $V_{ID} \geq 50$ mV | | 1.1 | 1.7 | mA |
| | | | EN1 = EN2 = 0, OUTx floating, $V_{ID} \leq –50$ mV | | 1.1 | 1.7 | |
| | | | $V_{ID} \geq 50$ mV | | 9.1 | 13.7 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID} \leq –50$ mV | | 9.2 | 13.9 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 1 Mbps | | 9.2 | 13.8 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 50 Mbps | | 10.3 | 15.5 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 100 Mbps | | 12.1 | 17.9 | |
| | | $4.5\ V < V_{CC1}$, $V_{CC2} < 5.5\ V$ | EN1 = EN2 = 0, OUTx floating, $V_{ID} \geq 50$ mV | | 1.2 | 1.8 | |
| | | | EN1 = EN2 = 0, OUTx floating, $V_{ID} \leq –50$ mV | | 1.2 | 1.8 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID} \geq 50$ mV | | 9.7 | 14.7 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, $V_{ID} \leq –50$ mV | | 9.7 | 14.8 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 1 Mbps | | 9.7 | 14.7 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 50 Mbps | | 11.5 | 17.3 | |
| | | | EN1 = EN2 = 1, $R_L$ = 100-Ω differential, data communication at 100 Mbps | | 14.2 | 21 | |


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## 6.11 Switching Characteristics

(over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVDS CHANNEL** | | | | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | | | 17 | 25 | ns |
| PWD | Pulse width distortion $\|t_{PHL} – t_{PLH}\|$ | | | 0 | 4.5 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time | Same directional channels, same voltage and temperature | | | 2.5 | ns |
| $t_{sk(pp)}$ | Part-part skew | Same directional channels, same voltage and temperature | | | 4.5 | ns |
| $t_{CMset}$ | Common-mode settling time after EN = 0 to EN = 1 transition. | Common-mode capacitive load = 100 pF to 0.5 nF | | | 20 | µs |
| $t_{fs}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.7 V, see Figure 24 | | 0.2 | 9 | µs |
| $t_{ie}$ | Time interval error, or peak-to-peak jitter | $2^{16}$ – 1 PRBS data at 100 Mbps; RX $V_{ID}$ = 350 $mV_{PP}$, 1 ns $t_{rf}$ 10% to 90%, $T_A$ = 25°C, $V_{CC1}$, $V_{CC2}$ = 3.3 V | | 1 | | ns |
| **LVDS TX AND RX** | | | | | | |
| $t_{rf}$ | TX differential rise/fall times (20% to 80%) | See Figure 22 | 300 | 780 | 1380 | ps |
| $\Delta V_{OC(pp)}$ | TX common-mode voltage peak-to-peak at 100 Mbps | | | 0 | 150 | $mV_{PP}$ |
| $t_{PLZ}$, $t_{PHZ}$ | TX disable time—valid output to HiZ | See Figure 23 | | 10 | 20 | ns |
| $t_{PZH}$ | Enable propagation delay, high impedance-to-high output | See Figure 23 | | 10 | 20 | ns |
| $t_{PZL}$ | Enable propagation delay, high impedance-to-low output | See Figure 23 | | 2 | 2.5 | µs |
| $\|V_{ID}\|$ | Magnitude of RX input differential voltage for valid operation | Driven with voltage sources on RX pins, see the figures in the *Parameter Measurement Information* section | 100 | | 600 | mV |
| $t_{rf(RX)}$ | Allowed RX input differential rise and fall times (20% to 80%) | See Figure 27 | | 1 | 0.3 × UI(1) | ns |

(1) UI is the unit interval.

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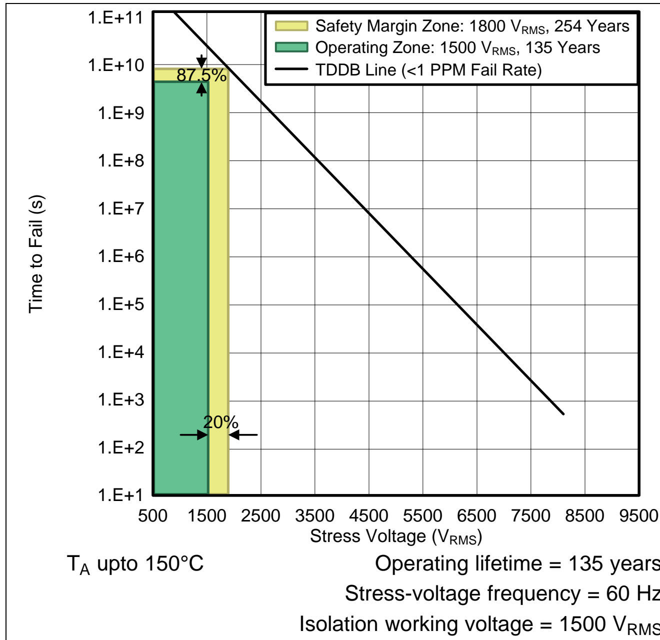
## 6.12 Insulation Characteristics Curves



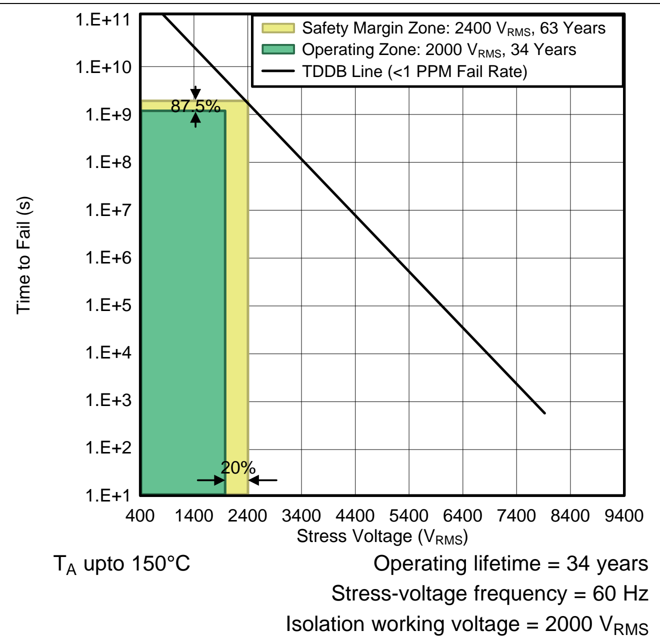

$T_A$ upto 150°C

Operating lifetime = 135 years

Stress-voltage frequency = 60 Hz

Isolation working voltage = 1500 $V_{RMS}$

**Figure 1. Reinforced Isolation Capacitor Lifetime Projection for Devices in DW Package**




$T_A$ upto 150°C

Operating lifetime = 34 years

Stress-voltage frequency = 60 Hz

Isolation working voltage = 2000 $V_{RMS}$

**Figure 2. Reinforced Isolation Capacitor Lifetime Projection for Devices in DWW Package**

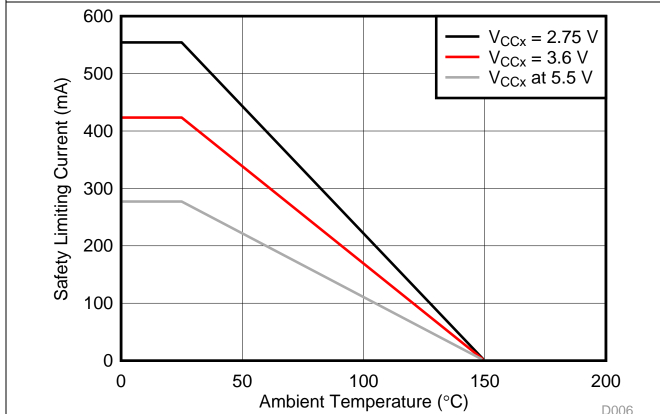



**Figure 3. Thermal Derating Curve for Limiting Current for DW Package**

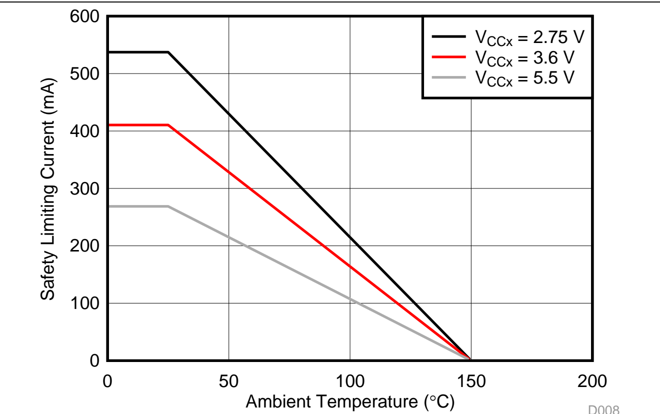



**Figure 4. Thermal Derating Curve for Limiting Current for DWW Package**

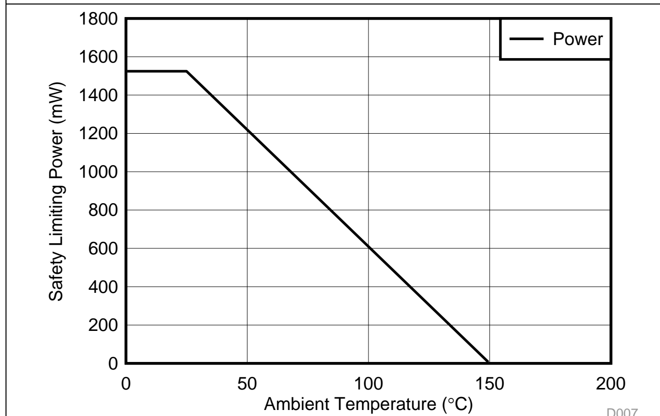



**Figure 5. Thermal Derating Curve for Limiting Power for DW Package**

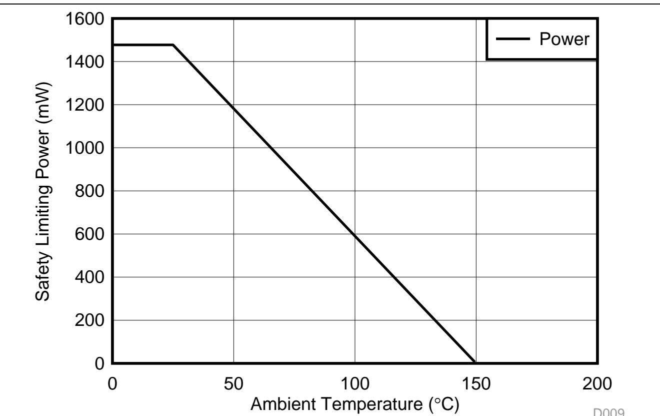



**Figure 6. Thermal Derating Curve for Limiting Power for DWW Package**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## 6.13 Typical Characteristics

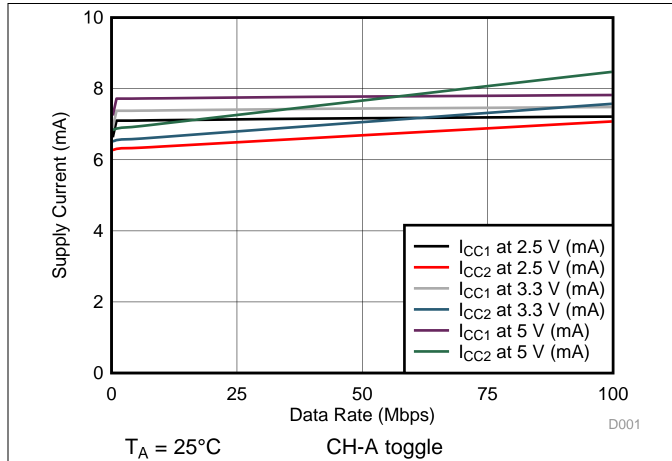



**Figure 7. ISO7821LL Supply Current vs Data Rate (CH-A)**

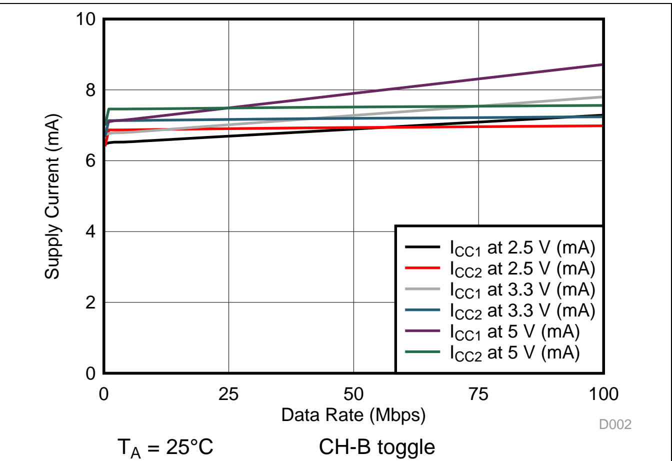



**Figure 8. ISO7821LL Supply Current vs Data Rate (CH-B)**

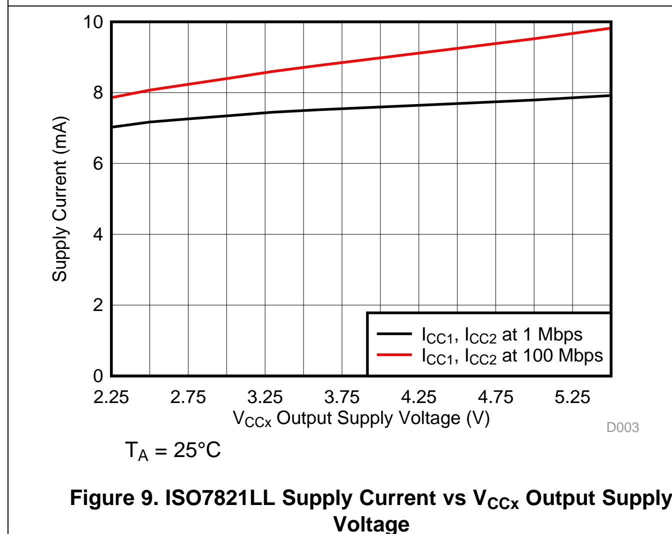



**Figure 9. ISO7821LL Supply Current vs $V_{CCx}$ Output Supply Voltage**

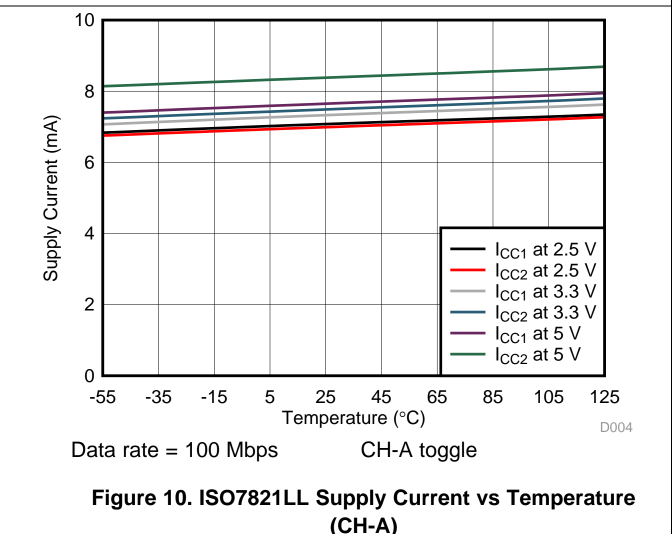



**Figure 10. ISO7821LL Supply Current vs Temperature (CH-A)**

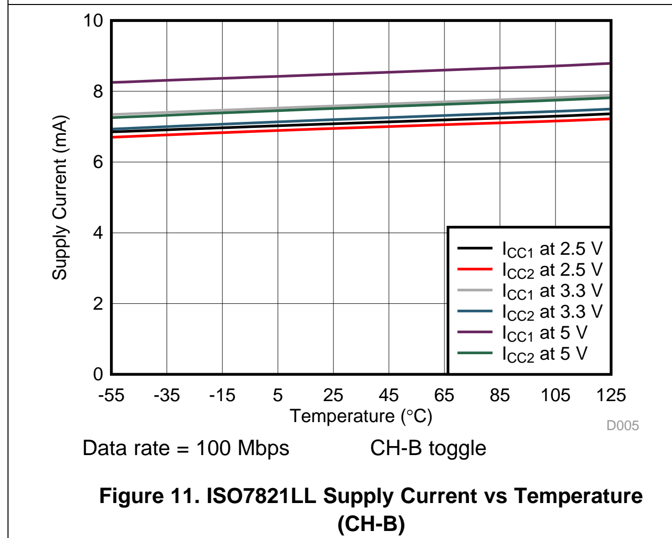



**Figure 11. ISO7821LL Supply Current vs Temperature (CH-B)**

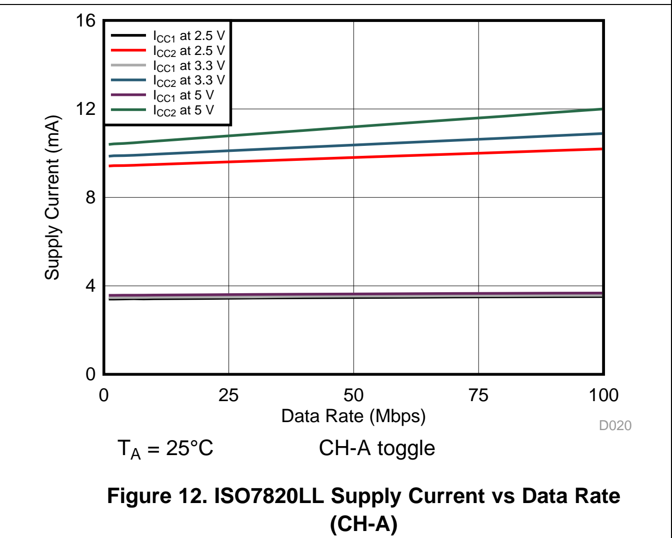
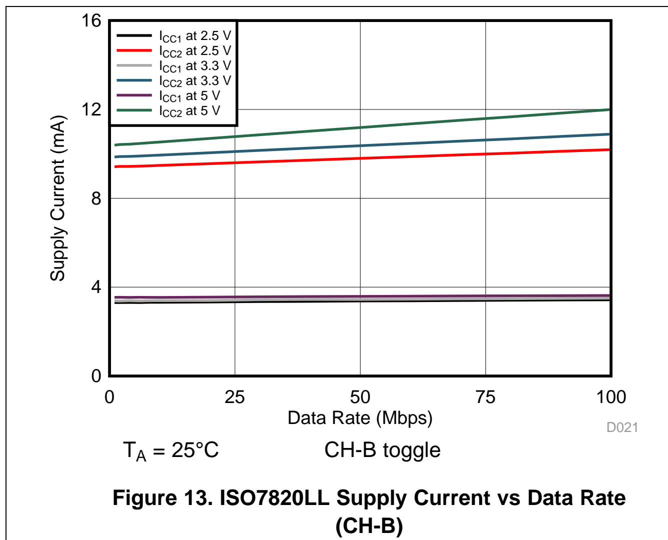


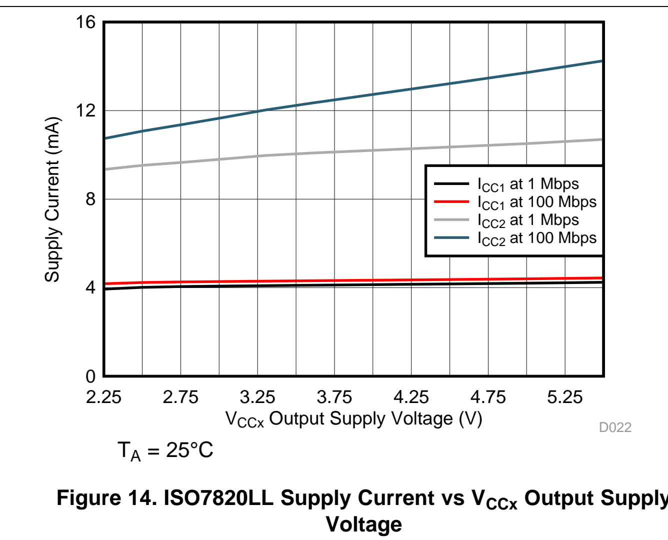

**Figure 12. ISO7820LL Supply Current vs Data Rate (CH-A)**

## Typical Characteristics (continued)



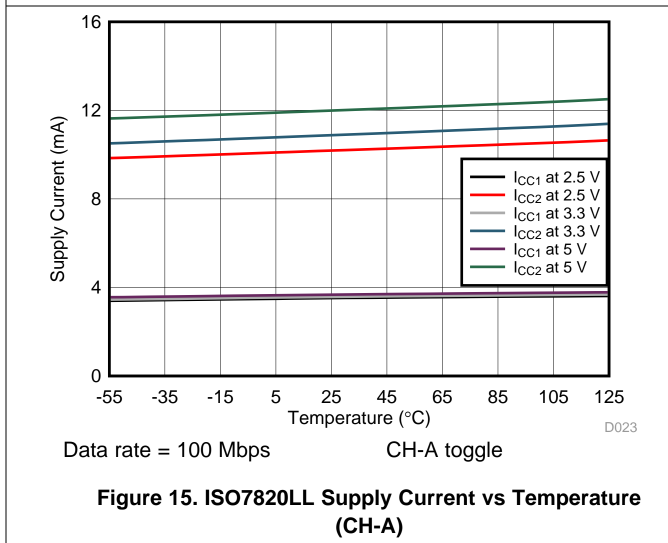

$T_A$ = 25°C CH-B toggle

**Figure 13. ISO7820LL Supply Current vs Data Rate (CH-B)**



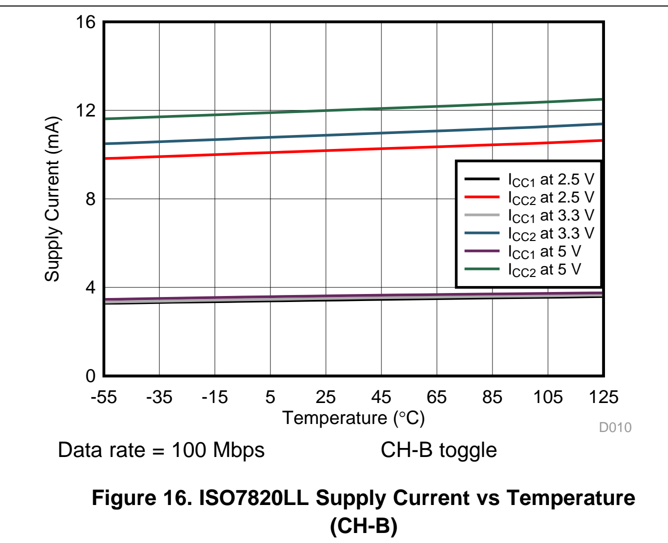

$T_A$ = 25°C

**Figure 14. ISO7820LL Supply Current vs $V_{CCx}$ Output Supply Voltage**




Data rate = 100 Mbps CH-A toggle

**Figure 15. ISO7820LL Supply Current vs Temperature (CH-A)**




Data rate = 100 Mbps CH-B toggle

**Figure 16. ISO7820LL Supply Current vs Temperature (CH-B)**

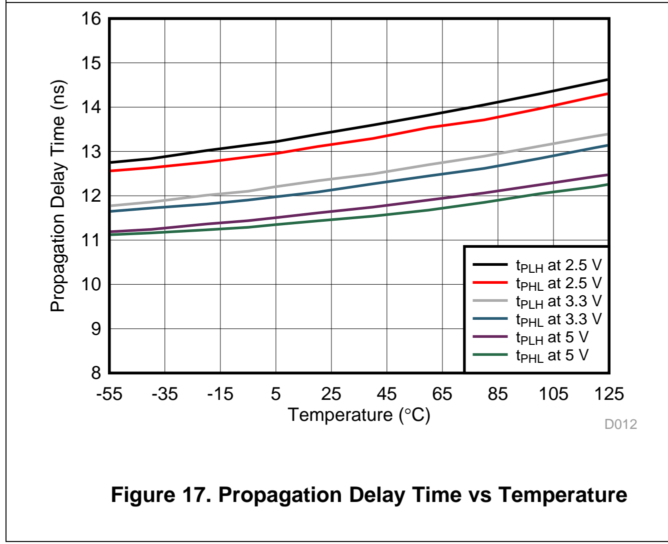
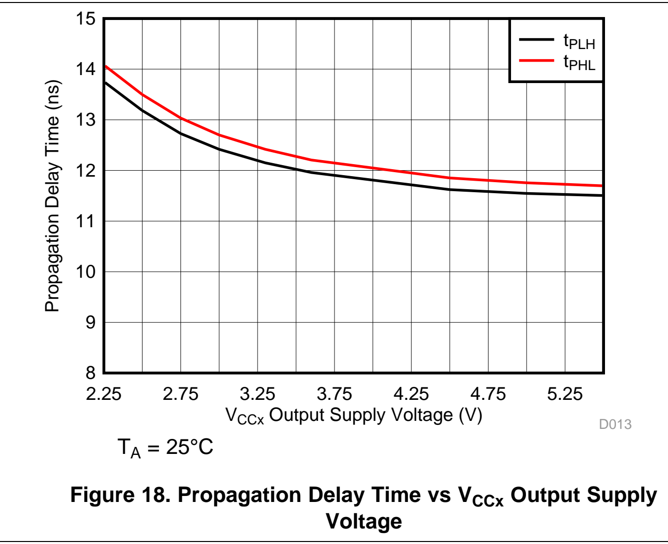



**Figure 17. Propagation Delay Time vs Temperature**




$T_A$ = 25°C

**Figure 18. Propagation Delay Time vs $V_{CCx}$ Output Supply Voltage**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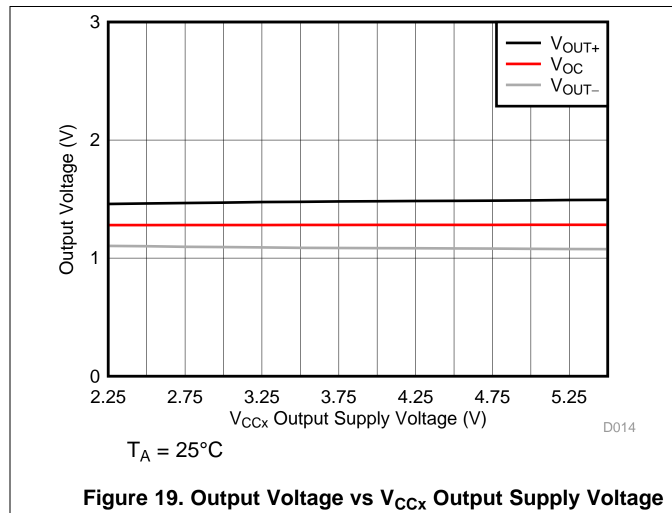
## Typical Characteristics (continued)




$T_A$ = 25°C

**Figure 19. Output Voltage vs $V_{CCx}$ Output Supply Voltage**

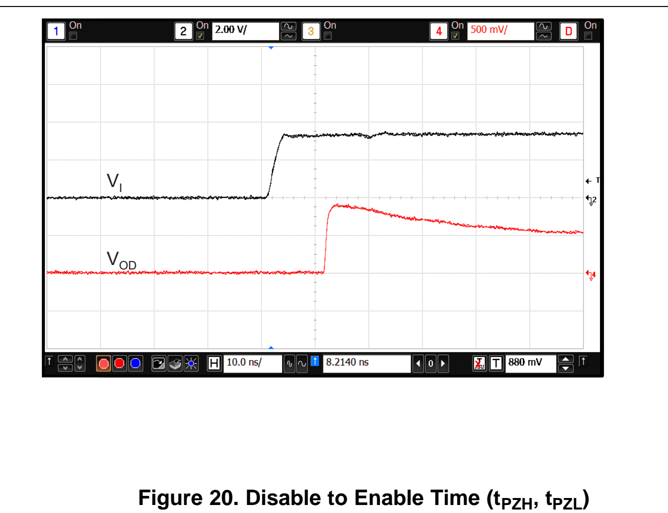



**Figure 20. Disable to Enable Time ($t_{PZH}$, $t_{PZL}$)**

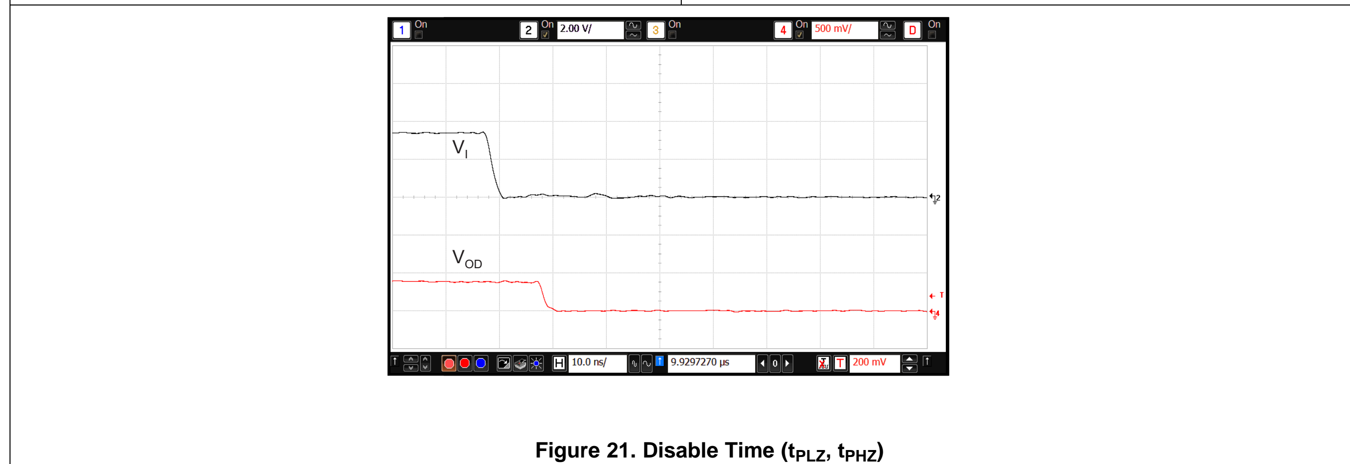
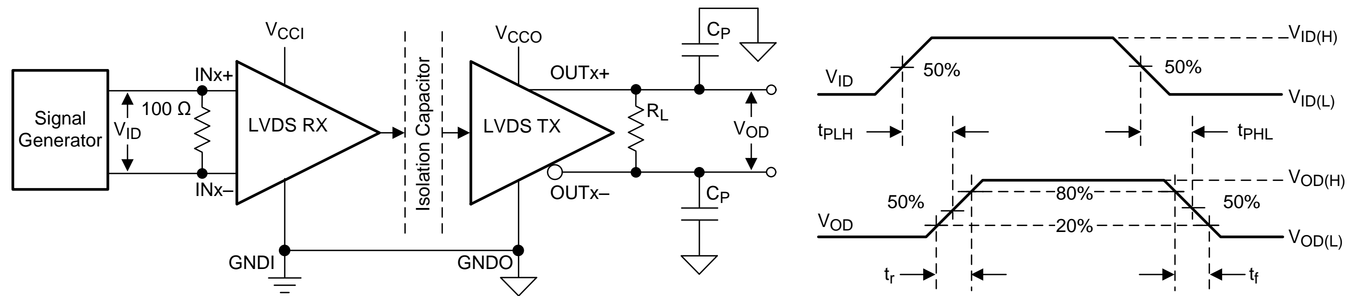



**Figure 21. Disable Time ($t_{PLZ}$, $t_{PHZ}$)**

# 7 Parameter Measurement Information




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50 Ω.

B. $C_P$ = 5 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 22. Switching Characteristics Test Circuit and Voltage Waveforms**

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50 Ω.

B. $C_L$ = 5 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 23. Enable and Disable Propagation Delay Time Test Circuit and Waveform**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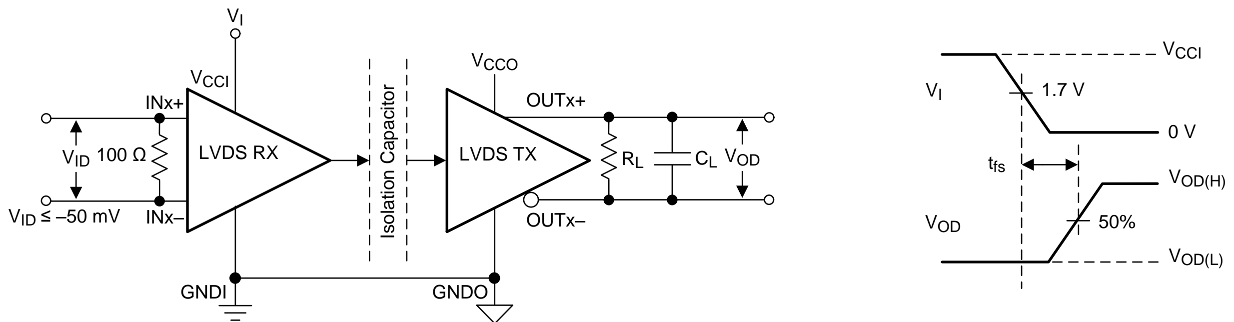
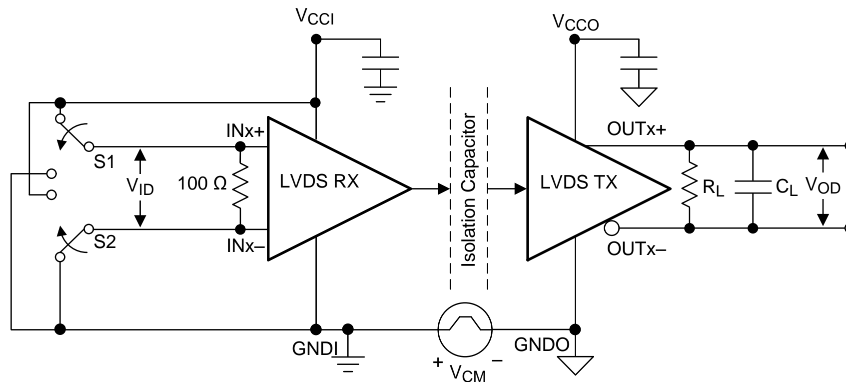
## Parameter Measurement Information (continued)




A. $C_L$ = 5 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 24. Default Output Delay Time Test Circuit and Voltage Waveforms**




A. $C_L$ = 5 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 25. Common-Mode Transient Immunity Test Circuit**

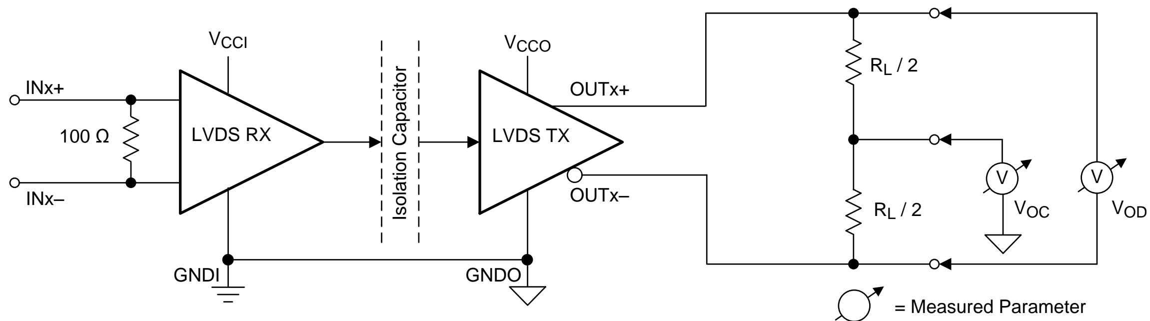



**Figure 26. Driver Test Circuit**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## Parameter Measurement Information (continued)

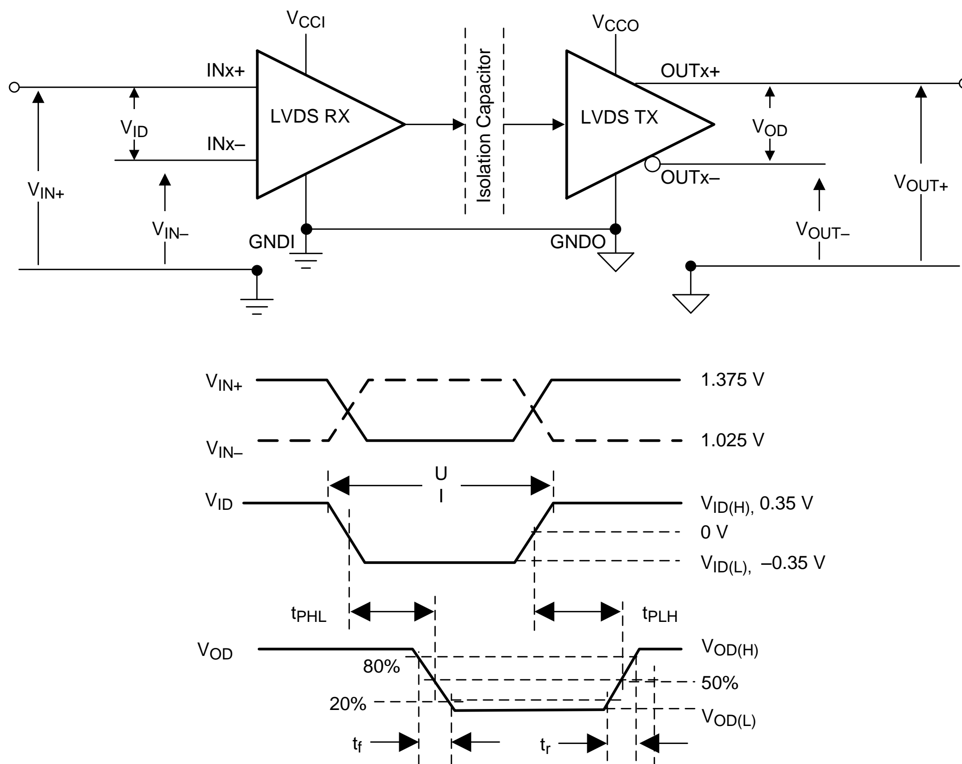


**Figure 27. Voltage Definitions and Waveforms**


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# 8 Detailed Description

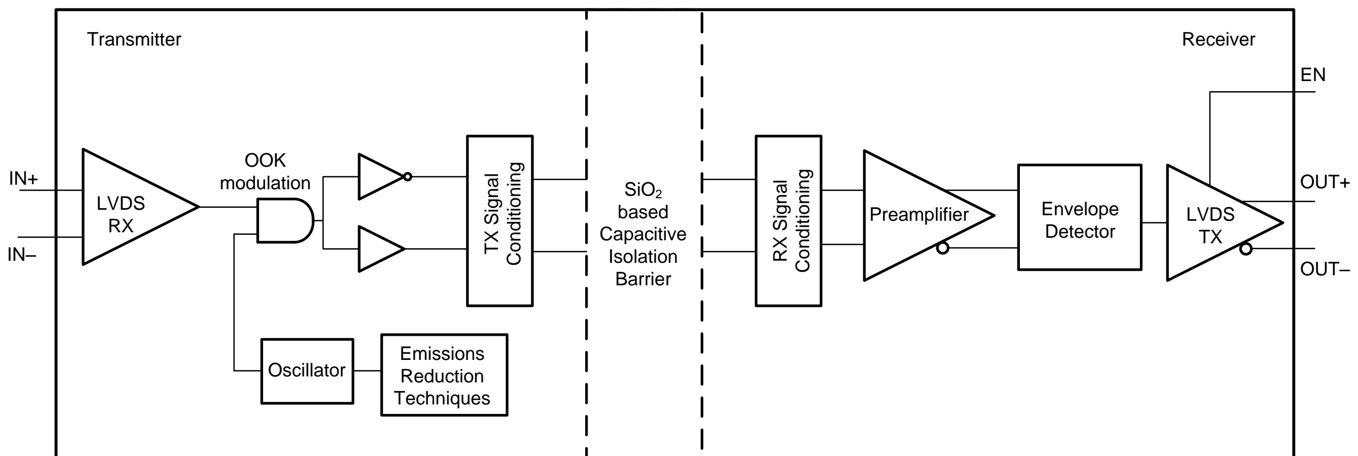
## 8.1 Overview

The ISO782xLL is a family of isolated LVDS buffers. The differential signal received on the LVDS input pins is first converted to CMOS logic levels. The signal is then transmitted across a silicon-dioxide ($SiO_2$) based capacitive-isolation barrier using an on-off keying (OOK) modulation scheme. A high frequency carrier transmitted across the barrier represents one logic state and an absence of a carrier represents the other logic state. On the other side of the barrier a demodulator converts the OOK signal back to logic levels, which is then converted to LVDS outputs by a differential driver. These devices incorporate advanced circuit techniques to maximize CMTI performance and minimize radiated emissions.

The ISO782xLL family of devices is TIA/EIA-644-A standard compliant. The LVDS transmitters drive a minimum differential-output voltage magnitude of 250 mV into a 100-Ω load, and the LVDS receivers are capable of detecting differential signals ≥50 mV in magnitude. The device consumes 10 mA per channel at 100 Mbps with 5-V supplies.

The *Functional Block Diagram* section shows a conceptual block diagram of one channel of the ISO782xLL family of devices.

## 8.2 Functional Block Diagram

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## 8.3 Feature Description

The ISO782xLL family of devices is available in two channel configurations with a default differential high-output state.

| PART NUMBER | CHANNEL DIRECTION | RATED ISOLATION | MAXIMUM DATA RATE | DEFAULT DIFFERENTIAL OUTPUT |
|---|---|---|---|---|
| ISO7820LL | 2 Forward | $5700\ V_{RMS}$ / $8000\ V_{PK}$ (1) | 100 Mbps | High |
| ISO7821LL | 1 Forward, 1 Reverse | | | |

(1) See the *Safety-Related Certifications* section for detailed isolation ratings.

## 8.4 Device Functional Modes

Table 1 lists the functional modes for the ISO782xLL family of devices.

**Table 1. ISO782xLL Function Table(1)**

| $V_{CCI}$ | $V_{CCO}$ | INPUT (INx±)(2) | OUTPUT ENABLE (ENx) | OUTPUT (OUTx±)(3) | COMMENTS |
|---|---|---|---|---|---|
| PU | PU | H | H or open | H | Normal Operation: A channel output assumes the logic state of the input. |
| | | L | H or open | L | |
| | | I | H or open | H or L | |
| X | PU | X | L | Z | A low-logic state at the output enable causes the outputs to be in high impedance. |
| PD | PU | X | H or open | H | Default mode: When $V_{CCI}$ is unpowered, a channel output assumes the logic high state.<br>When $V_{CCI}$ transitions from unpowered to powered up, a channel output assumes the logic state of the input.<br>When $V_{CCI}$ transitions from powered up to unpowered, a channel output assumes the selected default high state. |
| X | PD | X | X | Undetermined | When $V_{CCO}$ is unpowered, a channel output is undetermined.<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input |

(1) $V_{CCI}$ = input-side $V_{CC}$; $V_{CCO}$ = output-side $V_{CC}$; PU = powered up ($V_{CCx} \geq 2.25$ V); PD = powered down ($V_{CCx} \leq 1.7$ V); X = irrelevant
(2) Input (INx±): H = high level ($V_{ID} \geq 50$ mV); L = low level ($V_{ID} \leq -50$ mV); I = indeterminate ($-50$ mV $< V_{ID} < 50$ mV)
(3) Output (OUTx±): H = high level ($V_{OD} \geq 250$ mV); L = low level ($V_{OD} \leq -250$ mV); Z = high impedance.

### 8.4.1 Device I/O Schematics

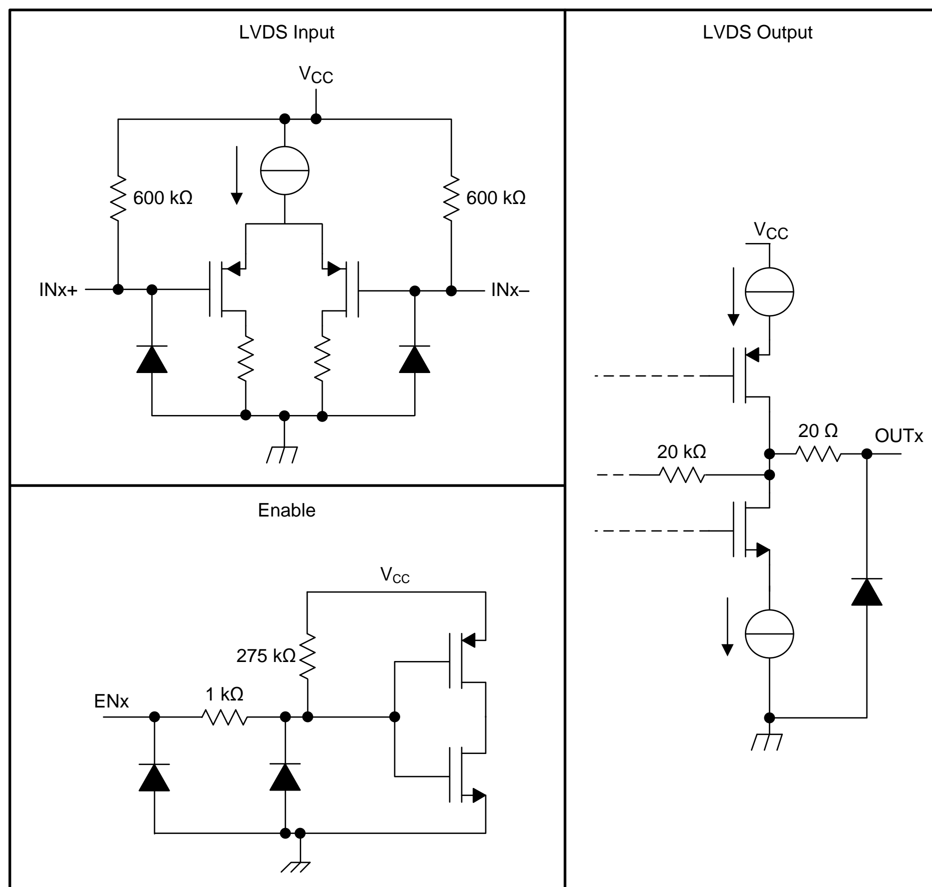


**Figure 28. Device I/O Schematics**


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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The ISO782xLL is a family of high-performance, reinforced isolated dual-LVDS buffers. Isolation can be used to help achieve human and system safety, to overcome ground potential difference (GPD), or to improve noise immunity and system performance.

The LVDS signaling can be used over most interfaces to achieve higher data rates because the LVDS is only a physical layer. LVDS can also be used for a proprietary communication scheme implemented between a host controller and a slave. Example use cases include connecting a high-speed I/O module to a host controller, a subsystem connecting to a backplane, and connection between two high-speed subsystems. Many of these systems operate under harsh environments making them susceptible to electromagnetic interferences, voltage surges, electrical fast transients (EFT), and other disturbances. These systems must also meet strict limits on radiated emissions. Using isolation in combination with a robust low-noise signaling standard such as LVDS, achieves both high immunity to noise and low emissions.

Example end applications that could benefit from the ISO782xLL family of devices include high-voltage motor control, test and measurement, industrial automation, and medical equipment.

## 9.2 Typical Application

One application for isolated LVDS buffers is for point-to-point communication between two high-speed capable, application-specific integrated circuits (ASICs) or FPGAs. In a high-voltage motor control application, for example, Node 1 could be a controller on a low-voltage or earth referenced board, and Node 2, could be controller placed on the power board, biased to high voltage. Figure 29 and Figure 30 show the application schematics.

Figure 30 provides further details of using the ISO782xLL family of devices to isolate the LVDS interface. The LVDS connection to the ISO782xLL family of devices can be traces on a board (shown as straight lines between Node 1 and the ISO782xLL device), a twisted pair cable (as shown between Node 2 and the ISO782xLL device), or any other controlled impedance channel. Differential 100-Ω terminations are placed near each LVDS receiver. The characteristic impedance of the channel should also be 100-Ω differential.

In the example shown in Figure 29 and Figure 30, the ISO782xLL family of devices provides reinforced or safety isolation between the high-voltage elements of the motor drive and the low-voltage control circuitry. This configuration also ensures reliable communication, regardless of the high conducted and radiated noise present in the system.

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## Typical Application (continued)

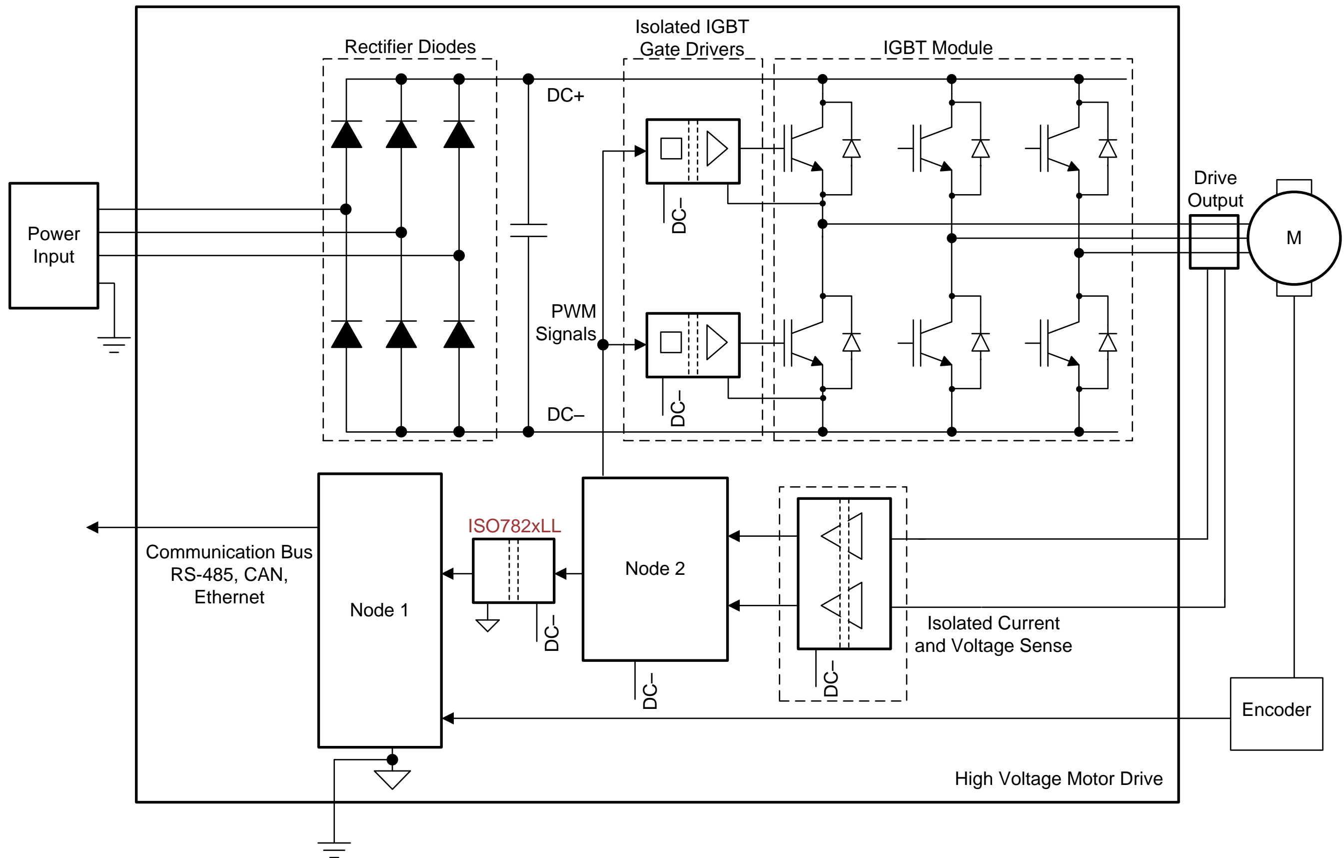


**Figure 29. Isolated LVDS Interface in Motor Control Application**

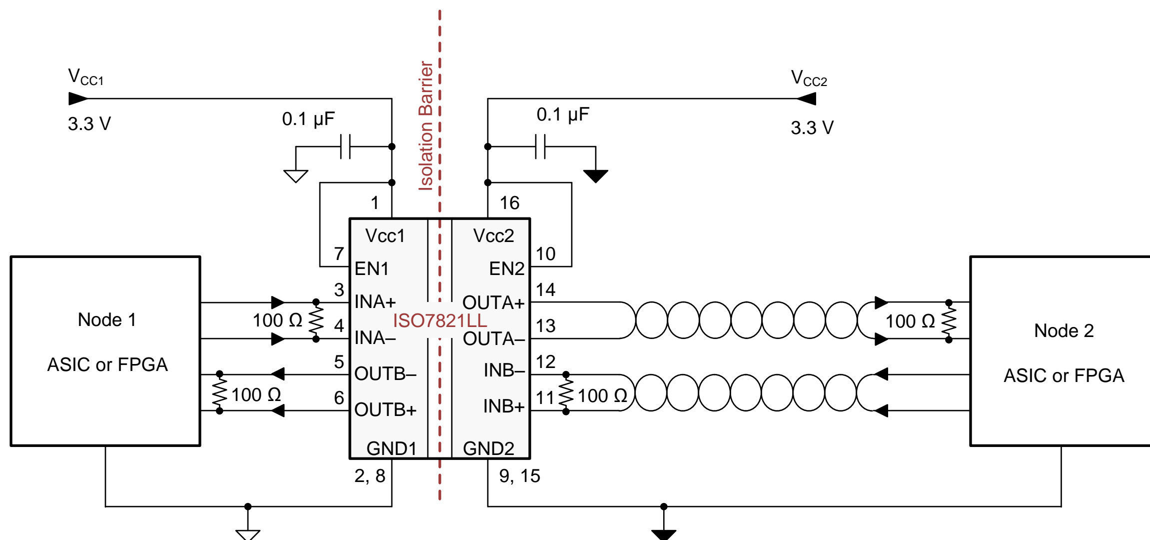


**Figure 30. Isolated LVDS Interface Between Two Nodes (ASIC or FPGA)**


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## Typical Application (continued)

### 9.2.1 Design Requirements

For the ISO782xLL family of devices, use the parameters listed in Table 2.

**Table 2. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Supply voltage range, $V_{CC1}$ and $V_{CC2}$ | 2.25 V to 5.5 V |
| Receiver common-mode voltage range | For $V_{CCx} \geq 3$ V: 0.5 $\lvert V_{ID} \rvert$ to 2.4 – 0.5 $\lvert V_{ID} \rvert$ |
| | For $V_{CCx} < 3$ V: 0.5 $\lvert V_{ID} \rvert$ to $V_{CCx}$ – 0.6 – 0.5 $\lvert V_{ID} \rvert$ |
| External termination resistance | 100 Ω |
| Interconnect differential characteristic impedance | 100 Ω |
| Signaling rate | 0 to 100 Mbps |
| Decoupling capacitor from $V_{CC1}$ and GND1 | 0.1 µF |
| Decoupling capacitor from $V_{CC2}$ and GND2 | 0.1 µF |

### 9.2.2 Detailed Design Procedure

The ISO782xLL family of devices has minimum requirements on external components for correct operation. External bypass capacitors (0.1 µF) are required for both supplies ($V_{CC1}$ and $V_{CC2}$). A termination resistor with a value of 100 Ω is required between each differential input pair (INx+ and INx–), with the resistors placed as close to the device pins as possible. A differential termination resistor with a value of 100 Ω is required on the far end for the LVDS transmitters. Figure 31 and Figure 32 show these connections.

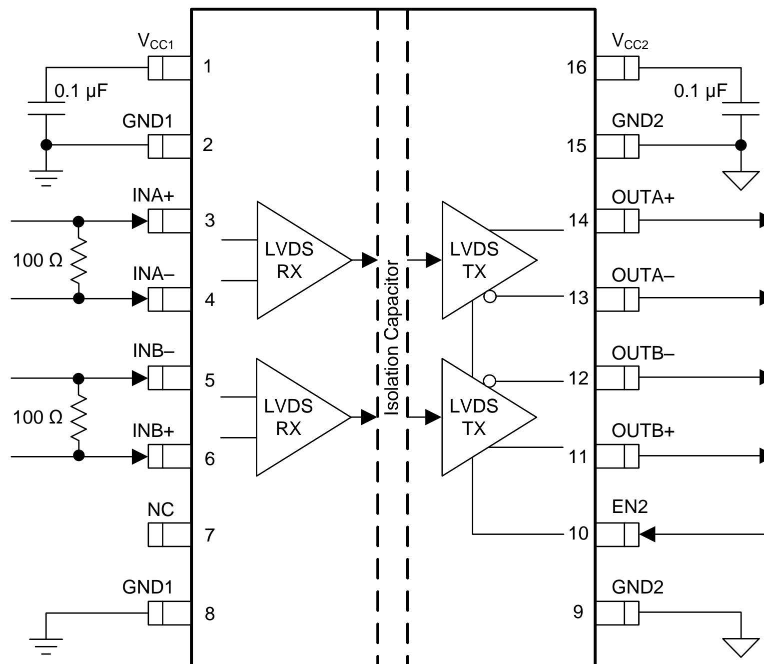


**Figure 31. Typical ISO7820LL Circuit Hook-Up**

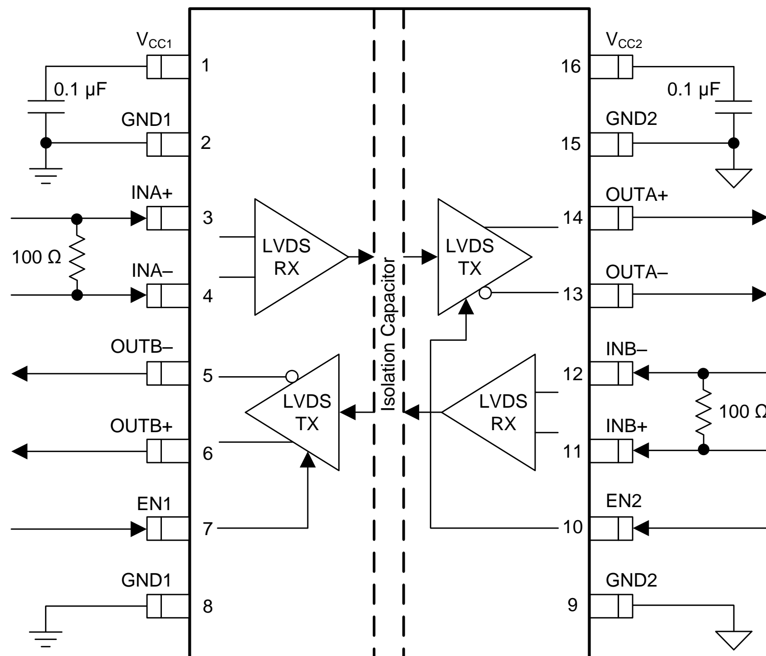


**Figure 32. Typical ISO7821LL Circuit Hook-Up**

#### *9.2.2.1 Electromagnetic Compatibility (EMC) Considerations*

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO782xLL family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.


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### 9.2.3 Application Curve

Figure 33 shows a typical eye diagram of the ISO782xLL family of devices which indicates low jitter and a wide-open eye at the maximum data rate of 100 Mbps.

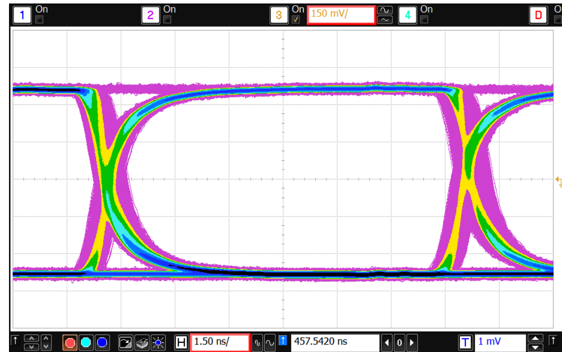


**Figure 33. Eye Diagram at 100 Mbps PRBS, 3.3 V and 25°C**

## 10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins ($V_{CC1}$ and $V_{CC2}$). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505. For such applications, detailed power supply design and transformer selection recommendations are available in the following data sheets: *SN6501 Transformer Driver for Isolated Power Supplies* (SLLSEA0) and *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* (SLLSEP9).

# 11 Layout

## 11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 34). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in$^2$.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- While routing differential traces on a board, TI recommends that the distance between two differential pairs be much higher (at least 2x) than the distance between the traces in a differential pair. This distance minimizes crosstalk between the two differential pairs.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

The ISO782xLL family of devices requires no special layout considerations to mitigate electromagnetic emissions.

For detailed layout recommendations, see the *Digital Isolator Design Guide* (SLLA284).

### 11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps (or rise and fall times higher than 1 ns) and trace lengths of up to 10 inches, use standard FR–4 UL94V-0 epoxy-glass as PCB material. ThisPCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

## 11.2 Layout Example

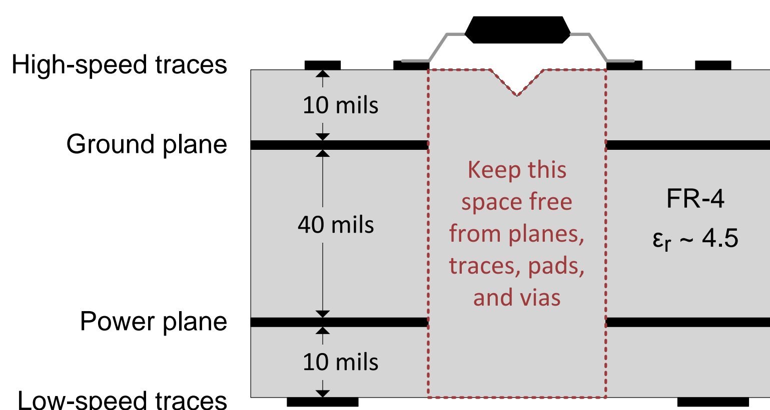


**Figure 34. Layout Example**


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# 12 デバイスおよびドキュメントのサポート

## 12.1 ドキュメントのサポート

### 12.1.1 関連資料

関連資料については、以下を参照してください:

- *『デジタル・アイソレータ設計ガイド』*(SLLA284)
- *『ISO782xLLx 絶縁デュアルLVDSバッファ評価モジュール』*(SLLU240)
- *『絶縁の用語集』*(SLLA353)
- *『LVDSオーナー・マニュアル』*(SNLA187)
- *『SN6501 絶縁電源用の変圧器ドライバ』*(SLLSEA0)
- *『SN6505 絶縁電源用の低ノイズ1A変圧器ドライバ』*(SLLSEP9)

## 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comで、お使いのデバイスの製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」ボタンをクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.3 コミュニティ・リソース

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**設計サポート** ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

## 12.4 商標

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## 12.5 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 12.6 用語集

SLYZ022 — *TI用語集*.
この用語集には、用語や略語の一覧および定義が記載されています。

# 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7820LLDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7820LL | Samples |
| ISO7820LLDWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7820LL | Samples |
| ISO7820LLDWW | ACTIVE | SOIC | DWW | 16 | 45 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -55 to 125 | ISO7820LL | Samples |
| ISO7820LLDWWR | ACTIVE | SOIC | DWW | 16 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -55 to 125 | ISO7820LL | Samples |
| ISO7821LLDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7821LL | Samples |
| ISO7821LLDWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7821LL | Samples |
| ISO7821LLDWW | ACTIVE | SOIC | DWW | 16 | 45 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -55 to 125 | ISO7821LL | Samples |
| ISO7821LLDWWR | ACTIVE | SOIC | DWW | 16 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -55 to 125 | ISO7821LL | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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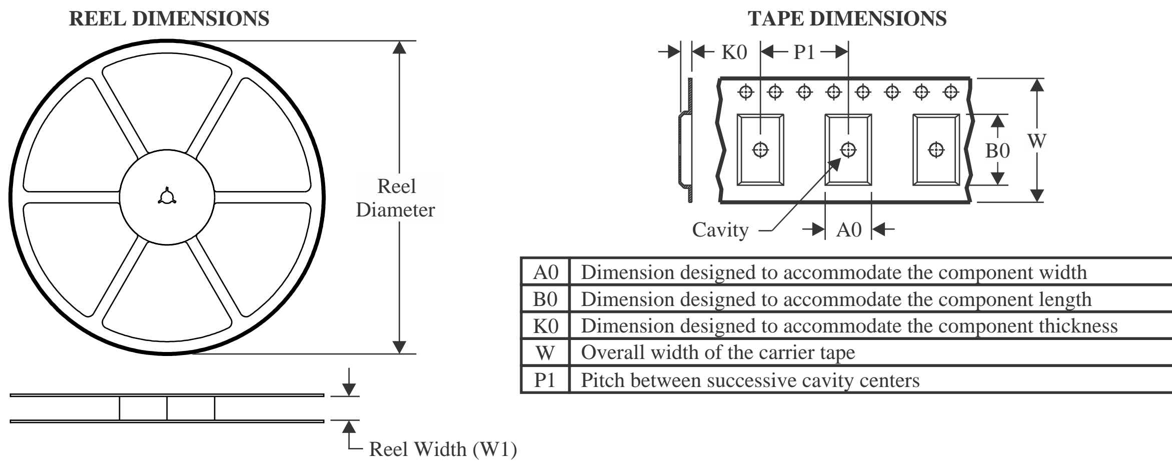
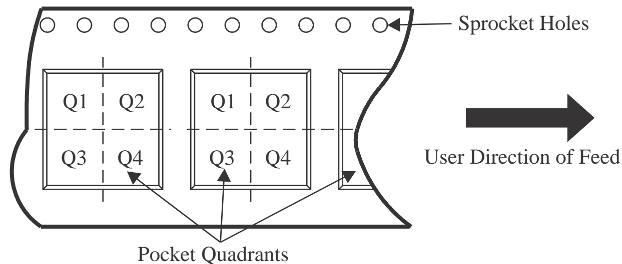
## TAPE AND REEL INFORMATION

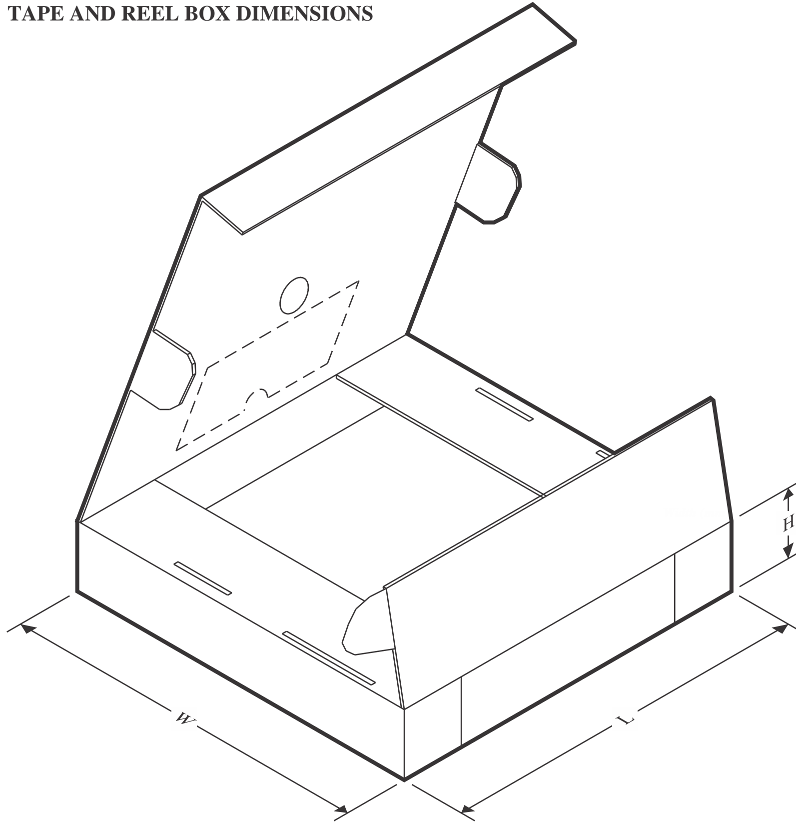



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7820LLDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7820LLDWWR | SOIC | DWW | 16 | 1000 | 330.0 | 24.4 | 18.0 | 10.0 | 3.0 | 20.0 | 24.0 | Q1 |
| ISO7821LLDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7821LLDWWR | SOIC | DWW | 16 | 1000 | 330.0 | 24.4 | 18.0 | 10.0 | 3.0 | 20.0 | 24.0 | Q1 |

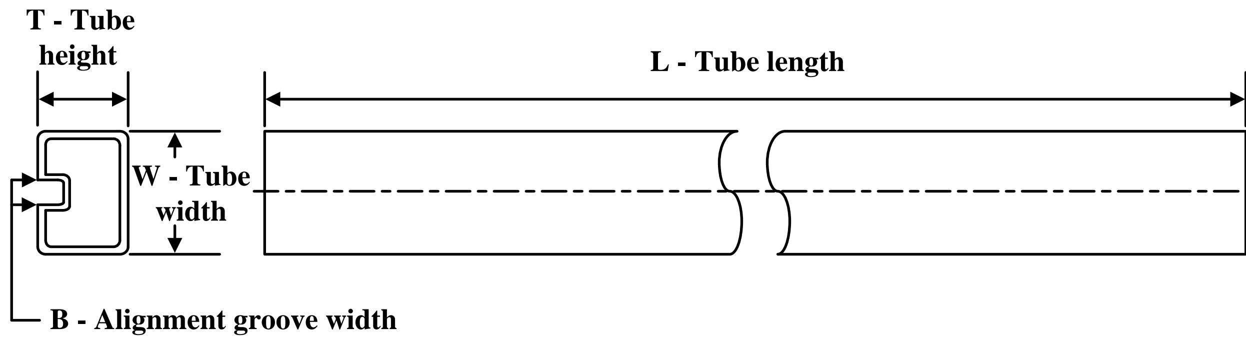
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7820LLDWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7820LLDWWR | SOIC | DWW | 16 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO7821LLDWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7821LLDWWR | SOIC | DWW | 16 | 1000 | 350.0 | 350.0 | 43.0 |

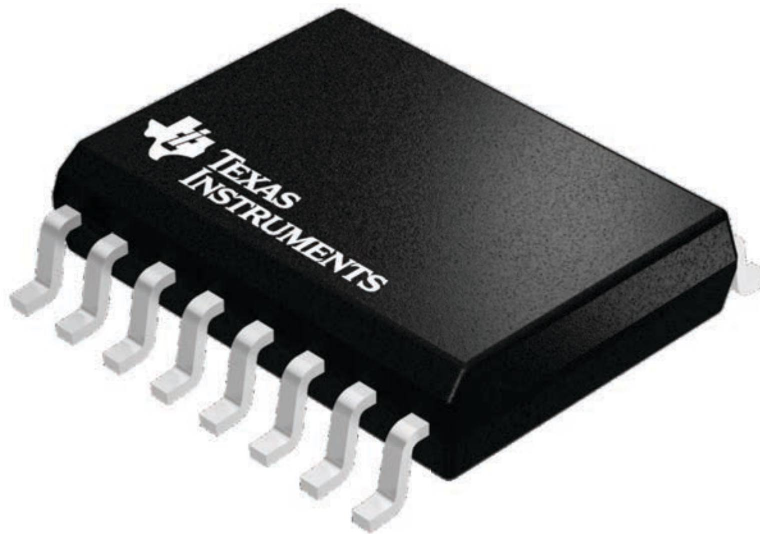
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| ISO7820LLDW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7820LLDWW | DWW | SOIC | 16 | 45 | 507 | 20 | 5000 | 9 |
| ISO7821LLDW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7821LLDWW | DWW | SOIC | 16 | 45 | 507 | 20 | 5000 | 9 |

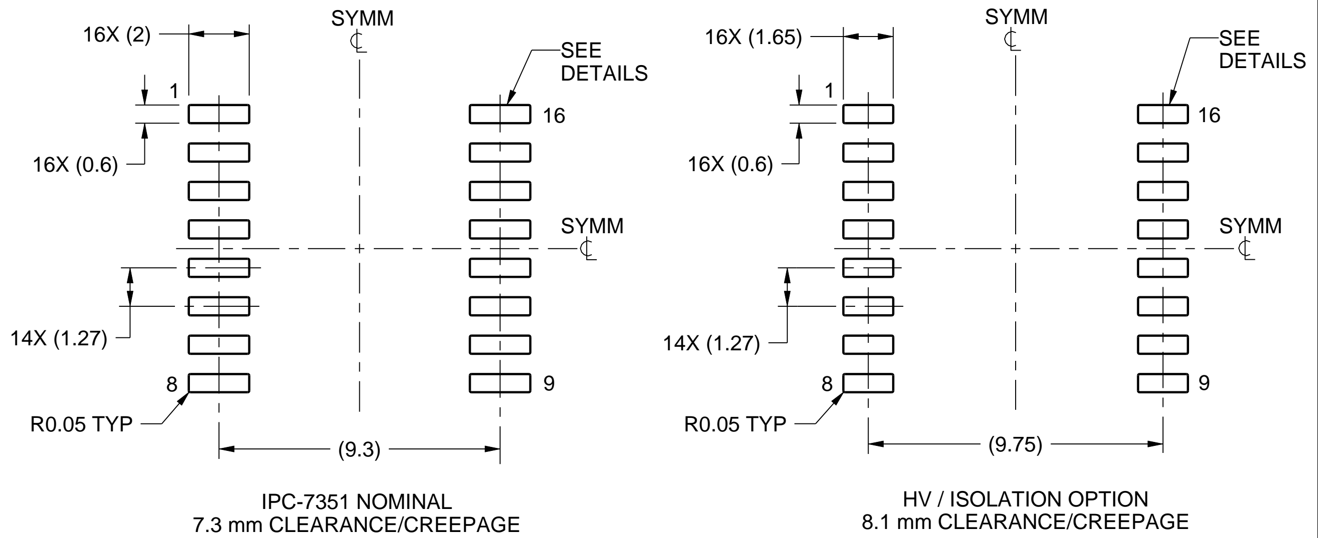
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



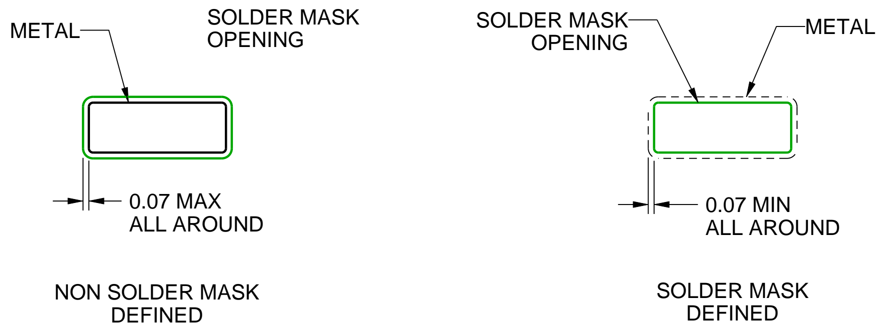

4224780/A

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:4X

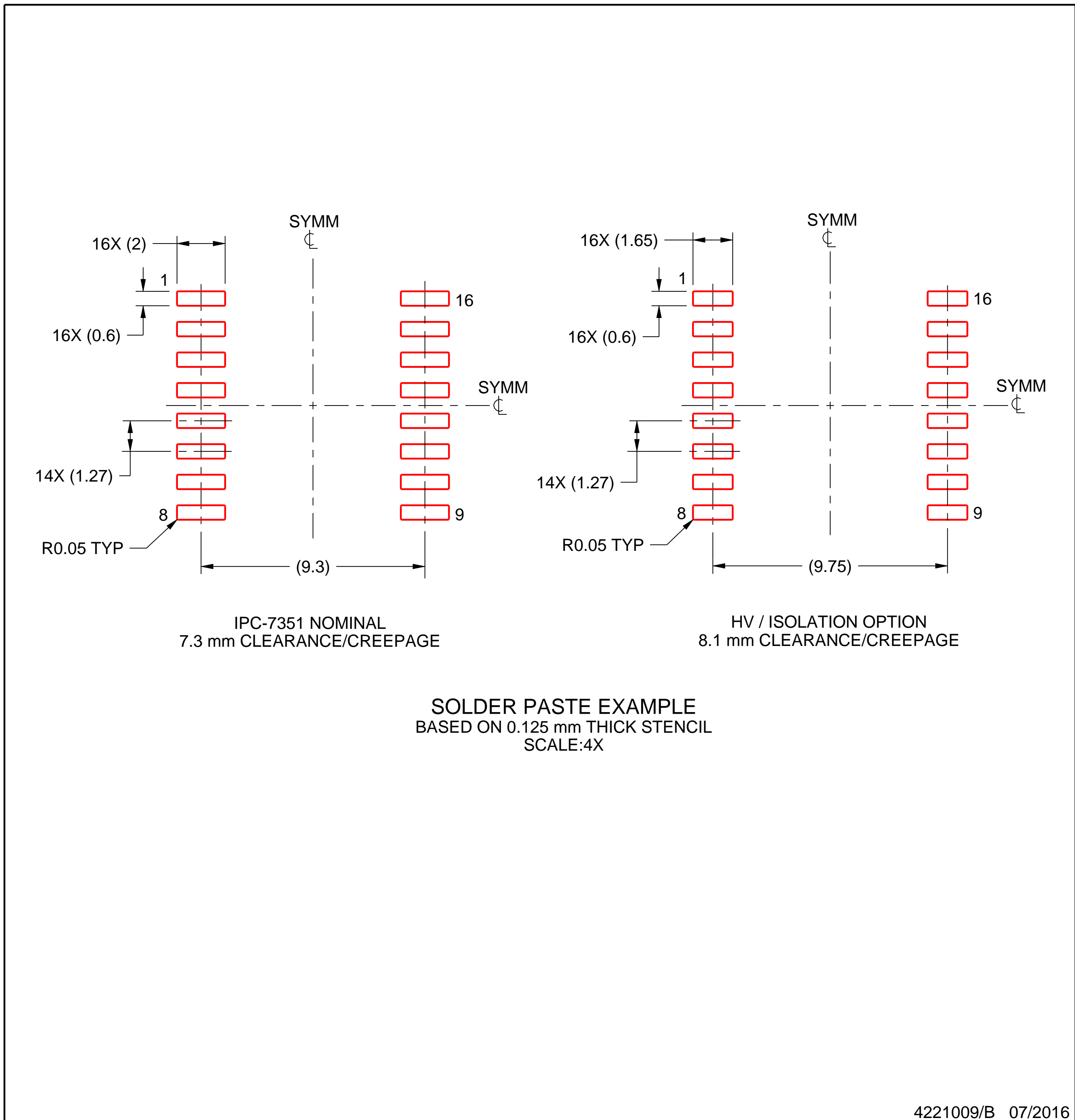



SOLDER MASK DETAILS

4221009/B 07/2016

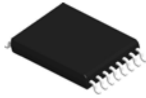
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



17.4
17.1

PIN 1 ID AREA

A

1

16

14X 1.27

C

SEATING PLANE

0.1 C

10.4
10.2
NOTE 3

2X 8.89

8

9

16X 0.51 0.31

0.25 Ⓜ A B C

B

14.1
13.9
NOTE 4

(2.286)

2.65 MAX

SEE DETAIL A

0.28
0.22 TYP

(1.625)

0.25
GAGE PLANE

0°-8°

1.1
0.6

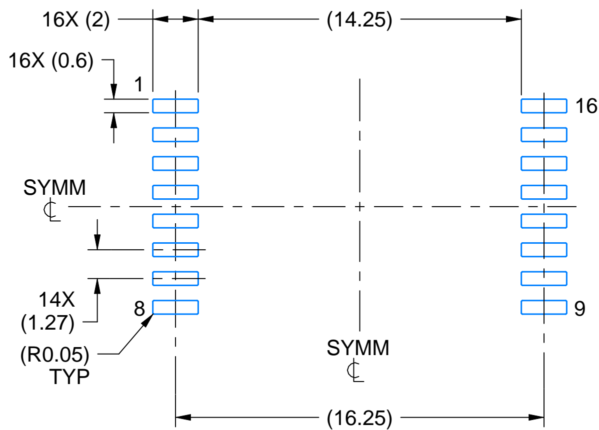
0.3
0.1

DETAIL A
TYPICAL

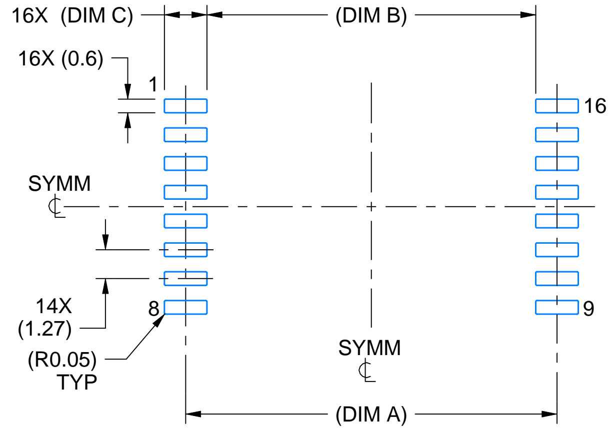
4221501/B 10/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

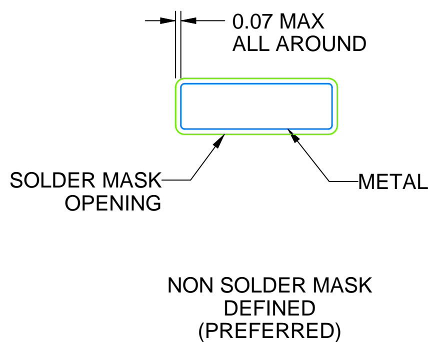



LAND PATTERN EXAMPLE
STANDARD
SCALE:3X

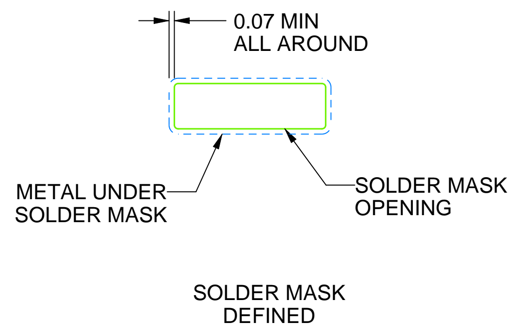



LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X

| OPTION | DIM A | DIM B | DIM C |
|---|---|---|---|
| 01 | 16.375 | 14.5 | 1.875 |
| 02 | 16.625 | 15 | 1.625 |
| 03 | 16.725 | 15.2 | 1.525 |




NON SOLDER MASK
DEFINED
(PREFERRED)



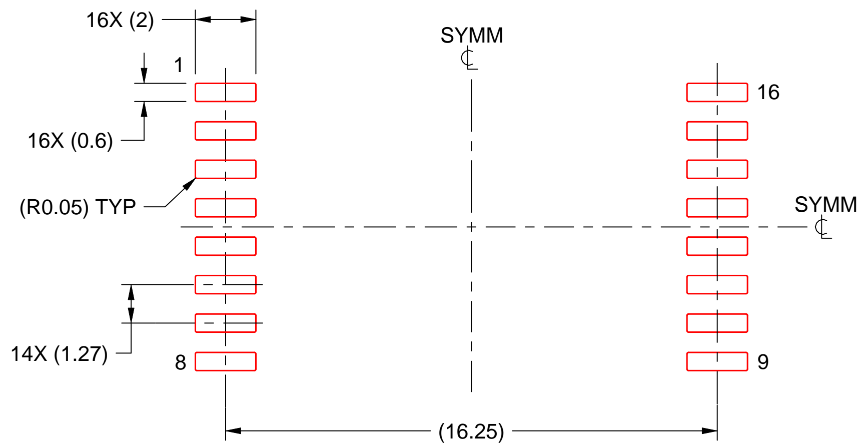

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

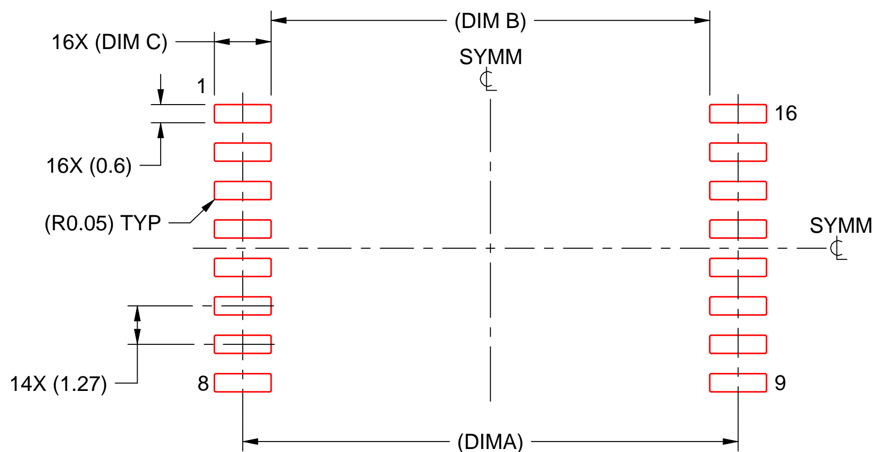
4221501/B 10/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X




SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

| OPTION | DIM A | DIM B | DIM C |
|---|---|---|---|
| 01 | 16.375 | 14.5 | 1.875 |
| 02 | 16.625 | 15 | 1.625 |
| 03 | 16.725 | 15.2 | 1.525 |

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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