ISO7741TA-Q1, ISO7741TB-Q1, ISO7742TA-Q1, ISO7742TB-Q1
ISO7741FTA-Q1, ISO7741FTB-Q1, ISO7742FTA-Q1, ISO7742FTB-Q1
JAJSUA0B – APRIL 2024 – REVISED JANUARY 2025

ISO774xT-Q1、高速、、強化、4 チャネルのデジタル アイソレータ 統合トランス ドライバを搭載

1 特長

- 車載アプリケーション用の AEC-Q100 に認定済み
- デバイス温度グレード 1:–40℃ ～ 125℃ の動作時周囲温度
- 機能安全対応
  - ISO 26262 システムの設計に役立つ資料を利用可能
- 100Mbps のデータ レート
- 堅牢な絶縁バリア:
  - 1500V_{RMS} の動作電圧で 30 年を超える予測寿命
  - 定格絶縁電圧 5000V_{RMS}
  - 最高 12.8kV のサージ耐量
  - デジタル アイソレータ向けの CMTI の代表値: ±150kV/µs
- 幅広い電源電圧範囲:2.25V～5.5V
- 2.25V から 5.5V への電圧変換
- デフォルト出力が *HIGH* (ISO774xT) と *LOW* (ISO774xFT) のオプション
- 低い消費電力:1Mbps でチャネルごとに標準値 1.5mA
- 短い伝搬遅延:5V で 10.7ns (標準値)
- 堅牢な電磁両立性 (EMC)
  - システム レベルでの ESD、EFT、サージ耐性
- トランス用のプッシュプル ドライバ
- 高出力ドライブ:5V 電源で最大 0.7A
- 低い R_{ON}:4.5V 電源で最大値 0.4Ω
- スペクトラム拡散クロック
- 5V 電源でのトランスドライバの標準的な電流制限は 1.75A です。
- 安全性関連の認定 (予定):
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 部品認定プログラム
  - IEC 61010-1、IEC 62368-1、IEC 60601-1、GB 4943.1 認証

2 アプリケーション

ハイブリッド、電気自動車、およびパワートレイン システム (EV/HEV)

- バッテリ管理システム (BMS)
- オンボード チャージャ
- トラクション インバータおよびモーター制御
- DC/DC コンバータ

ボディ エレクトロニクス

- 車載パーキング ヒーター モジュール
- HVAC (エアコン) 制御モジュール

3 概要

ISO774xT-Q1 は、UL 1577 に準拠した定格絶縁電圧 5000V_{RMS} を利用する統合トランスフォーマーを搭載した 1 級高性能 4 チャネル デジタル アイソレータです。これは、VDE、CSA、TUV、CQC に従って絶縁定格が強化されています。

ISO774xT-Q1 デバイスは電磁気耐性が高く、エミッションが少なく、低消費電力を実現し、CMOS または LVCMOS デジタル I/O が絶縁されています。それぞれの絶縁チャネルにはロジック入力および出力バッファがあり、二重の容量性二酸化ケイ素 (SiO_2) 絶縁バリアによって分離されています。入力電源または入力信号が失われた場合のデフォルト出力は、接尾辞 F のないデバイスでは HIGH、接尾辞 F のあるデバイスでは LOW になります。詳細は「デバイスの機能モード」のセクションを参照してください。

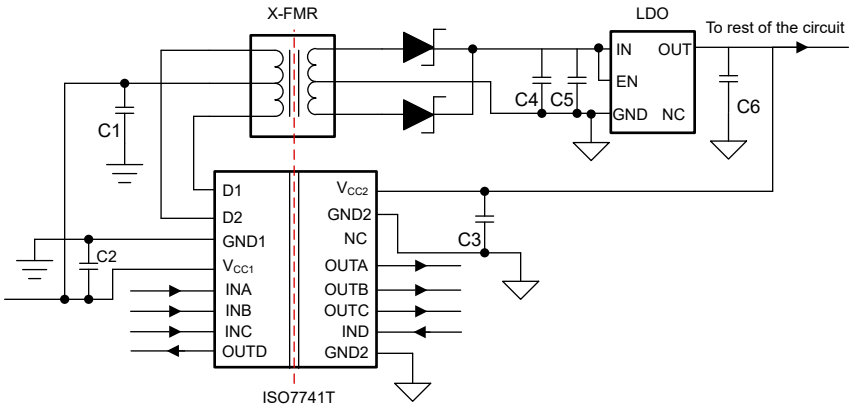
ISO774xT-Q1 は低ノイズ、低 EMI のプッシュプル トランスドライバで、小型の絶縁電源に特化して設計されています。低背のセンター タップ付き変圧器を 2.25V～5.5V の DC 電源で駆動できます。出力スイッチ電圧のスルーレート制御と、スペクトラム拡散クロック (SSC) により、非常に低いノイズと EMI を実現しています。ISO774xT-Q1 は、発振器と、それに続くゲート ドライブ回路とで構成され、ゲート ドライブ回路はグランドを基準とする N チャネル パワー スイッチを駆動するための相補出力信号を供給します。このデバイスには、重負荷時のスタートアップを確保するため、2 つの 0.7A パワー MOSFET スイッチが内蔵されています。内部保護機能として、1.75A の電流制限、低電圧誤動作防止、サーマル シャットダウン、Break-Before-Make 回路が搭載されています。ISO774xT-Q1 は、ソフトスタート機能を備えており、大きい負荷コンデンサでの電源オン時に大きい突入電流を防止します。ISO774xTA-Q1 には、放射の最小化を必要とするアプリケーション向けに 160kHz の内部発振器が搭載されています。これに対して、ISO774xTB-Q1 には、高効率とサイズの小さい変圧器を必要とするアプリケーション向けに 420kHz の内部発振器が搭載されています。

ISO774xT-Q1 は、16 ピンの DW パッケージで供給されます。このデバイスは、–40℃～125℃の温度範囲で動作が規定されています。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)	パッケージ サイズ(2)
ISO7741Tx-Q1	DW (SOIC、16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO7741FTx-Q1	DW (SOIC、16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO7742Tx-Q1	DW (SOIC、16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO7742FTx-Q1	DW (SOIC、16)	10.30mm × 7.50mm	10.30mm × 10.30mm

(1) 供給されているすべてのパッケージについては、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Pin Configuration and Functions

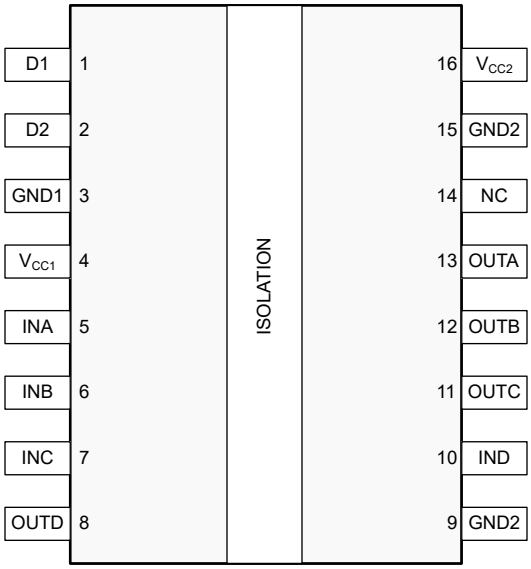


図 4-1. ISO7741T DW Package Top View

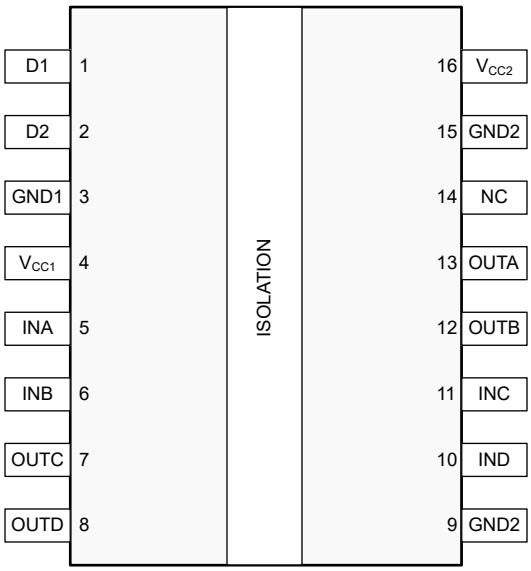


図 4-2. ISO7742T DW Package Top View

Pin Functions

NAME	PIN		Type[1]	DESCRIPTION
	ISO7741Tx/ ISO7741FTx	ISO7742Tx/ ISO7742FTx		
D1	1	1	O	Open drain output of the first power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, the external traces must be kept short.
D2	2	2	O	Open drain output of the second power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, the external traces must be kept short.
GND1	3	3	—	Ground connection for V_{CC1}
GND2	9	9	—	Ground connection for V_{CC2}
	15	15		
INA	5	5	I	Input, channel A
INB	6	6	I	Input, channel B
INC	7	11	I	Input, channel C
IND	10	10	I	Input, channel D
NC	14	14	—	Not connected
OUTA	13	13	O	Output, channel A
OUTB	12	12	O	Output, channel B
OUTC	11	7	O	Output, channel C
OUTD	8	8	O	Output, channel D
V_{CC1}	4	4	—	Power supply, side 1
V_{CC2}	16	16	—	Power supply, side 2

(1) I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

See(1)

			MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage (2)		-0.5	6	V
V	Voltage at INx, OUTx		-0.5	V_{CCX} + 0.5 (3)	V
D1, D2	Output switch voltage	D1, D2		16	V
$I_{(D1)Pk}$, $I_{(D2)Pk}$	Peak output switch current	$I_{(D1)Pk}$, $I_{(D2)Pk}$		2.4	A
I_O	Output current		-15	15	mA
T_J	Junction temperature		-40	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 HBM ESD Classification Level 3A (1)	±6000	V
		Charged-device model (CDM), per AEC Q100-011 V CDM ESD Classification Level C6	±1500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply Voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{D1}, I_{D2}	Output switch current - Primary side	2.25V ≤ V_{CC} ≤ 2.8V			0.7	A
I_{D1}, I_{D2}	Output switch current - Primary side	2.8V < V_{CC} ≤ 5.5V			0.7	A
I_{OH}	High level output current	V_{CCO} = 5V (1)	-4			mA
		V_{CCO} = 3.3V	-2			
		V_{CCO} = 2.5V	-1			
I_{OL}	Low level output current	V_{CCO} = 5V			4	mA
		V_{CCO} = 3.3V			2	
		V_{CCO} = 2.5V			1	
V_{IH}	High level Input voltage		0.7 x V_{CCI} (1)		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
DR	Data Rate(2)		0		100	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) 100Mbps is the maximum specified data rate, although higher data rates are possible.

5.4 Thermal Information

THERMAL METRIC(1)		ISO7741T-Q1	UNIT
		DW (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7741T-Q1						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 50MHz 50% duty cycle square wave, $I_{D1,}$ I_{D2}= 700mA			401	mW
P_{D1}	Maximum power dissipation (side-1)	V_{CC1} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 50MHz 50% duty cycle square wave, $I_{D1,}$ I_{D2}= 700mA			266	mW
P_{D2}	Maximum power dissipation (side-2)	V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 50MHz 50% duty cycle square wave, $I_{D1,}$ I_{D2}= 700mA			135	mW
ISO7742T-Q1						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 50MHz 50% duty cycle square wave, $I_{D1,}$ I_{D2}= 700mA			411	mW
P_{D1}	Maximum power dissipation (side-1)	V_{CC1} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 50MHz 50% duty cycle square wave, $I_{D1,}$ I_{D2}= 700mA			309	mW
P_{D2}	Maximum power dissipation (side-2)	V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 50MHz 50% duty cycle square wave, $I_{D1,}$ I_{D2}= 700mA			102	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤5	
		Method b: At routine test (100% production); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 x sin (2πft), f = 1MHz	≅1	pF
R_{IO}	Isolation resistance(6)	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 64°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C, I_L = 700mA see Figure 5-1			319	mA
		$R_{\theta JA}$ = 64°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C, I_L = 700mA see Figure 5-1			480	
		$R_{\theta JA}$ = 64°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C, I_L = 700mA see Figure 5-1			630	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 64°C/W, T_J = 150°C, T_A = 25°C see Figure 5-2			1953	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S must not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

5.9 Electrical Characteristics Transformer

over full-range of recommended operating conditions, unless otherwise noted. All typical values are at T_A = 25°C, V_{CC} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLK						
F_{SW}	D1, D2 average switching Frequency (ISO774xTA-Q1)	R_L = 50Ω to V_{CC1}	138	160	203	kHz
	D1, D2 average switching Frequency (ISO774xTB-Q1)	R_L = 50Ω to V_{CC1}	363	424	517	kHz
OUTPUT STAGE						
DMM	Average ON time mismatch between D1 and D2	R_L = 50Ω		0%		
$R_{(ON)}$	Output switch on resistance	V_{CC} = 4.5V, I_{D1}, I_{D2} = 700mA		0.22	0.4	Ω
		V_{CC} = 2.8V, I_{D1}, I_{D2} = 700mA		0.24	0.45	Ω
		V_{CC} = 2.25V, I_{D1}, I_{D2} = 0.5A		0.26	0.5	Ω
$V_{(SLEW)}$	Voltage slew rates on D1 and D2 for ISO774xTA-Q1	R_L = 50Ω to V_{CC1}		48		V/µs
$I_{(SLEW)}$	Current slew rates at D1 and D2 for ISO774xTA-Q1	R_L = 5Ω through transformer		11		A/µs
$V_{(SLEWHF)}$	Voltage slew rates on D1 and D2 for ISO774xTB-Q1	R_L = 50Ω to V_{CC1}		152		V/µs
$I_{(SLEWHF)}$	Current slew rates at D1 and D2 for ISO774xTB-Q1	R_L = 5Ω through transformer		41		A/µs
I_{LIM}	Current clamp limit (2.8V < V_{CC} ≤ 5.5V)		1.42	1.75	2.15	A
	Current clamp limit (2.25V ≤ V_{CC} ≤ 2.8V)		0.65		1.85	A
THERMAL SHUT DOWN						
T_{SD+}	T_{SD} turn on temperature		154	168	181	°C
T_{SD-}	T_{SD} turn off temperature		135	150	166	°C
T_{SD-}	T_{SD} hysteresis		13	17		°C

5.10 Electrical Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4mA	V_{CCO} - 0.4 (1)	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI(3)	Common mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1200V	100	150		kV/µs
C_I	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.
(3) CMTI is measured only on digital isolator independent of transformer driver

5.11 Supply Current Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10%, R_L = 50Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7741TA-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7741T)(1) V_I = 0V (ISO7741FT)		I_{CC1}		3	4.2	mA
			I_{CC2}		2.4	3.7	
	V_I =0V_I (ISO7741T)(1) V_I = V_{CCI} (ISO7741FT)		I_{CC1}		6.3	7.8	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.7	6.1	
			I_{CC2}		3.2	4.6	
		10Mbps	I_{CC1}		5.4	6.8	
			I_{CC2}		4.8	6.5	
		100Mbps	I_{CC1}		11.5	13.7	
			I_{CC2}		20	23.5	
ISO7741TB-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7741T)(1) V_I = 0V (ISO7741FT)		I_{CC1}		3.6	5	mA
			I_{CC2}		2.4	3.7	
	V_I =0V_I (ISO7741T)(1) V_I = V_{CCI} (ISO7741FT)		I_{CC1}		6.9	8.6	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		5.3	6.9	
			I_{CC2}		3.2	4.6	
		10Mbps	I_{CC1}		5.9	7.7	
			I_{CC2}		4.8	6.5	
		100Mbps	I_{CC1}		12.1	14.6	
			I_{CC2}		20	23.5	
ISO7742TA-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7742T)(1) V_I = 0V (ISO7742FT)		I_{CC1}		3.3	4.8	mA
			I_{CC2}		2.4	3.5	
	V_I =0V_I (ISO7742T)(1) V_I = V_{CCI} (ISO7742FT)		I_{CC1}		5.6	7.3	
			I_{CC2}		4.7	6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.6	6.2	
			I_{CC2}		3.6	4.9	
		10Mbps	I_{CC1}		5.7	7.4	
			I_{CC2}		4.7	6.1	
		100Mbps	I_{CC1}		16.6	19.6	
			I_{CC2}		15.7	18.4	

V_{CC1} = V_{CC2} = 5V ±10%, R_L = 50Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7742TB-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7742T)(1) V_I = 0V (ISO7742FT)		I_{CC1}		3.9	5.6	mA
			I_{CC2}		2.4	3.5	
	V_I =0V_I (ISO7742T)(1) V_I = V_{CCI} (ISO7742FT)		I_{CC1}		6.2	8.2	
			I_{CC2}		4.7	6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		5.2	7	
			I_{CC2}		3.6	4.9	
		10Mbps	I_{CC1}		6.2	8.3	
			I_{CC2}		4.7	6.1	
		100Mbps	I_{CC1}		17.3	20.5	
			I_{CC2}		15.7	18.4	

(1) V_{CCI} = Input-side V_{CC}

5.12 Electrical Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10%, R_L = 50Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA	V_{CCO} - 0.3 (1)	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA		0.1	0.3	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-10			µA
CMTI(2)	Common mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1200V	100	150		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) CMTI is measured only on digital isolator independent of transformer driver

5.13 Supply Current Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10%, R_L = 50Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7741TA-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7741T)(1) V_I = 0V (ISO7741FT)		I_{CC1}		2.8	3.9	mA
			I_{CC2}		2.3	3.7	
	V_I =0V_I (ISO7741T)(1) V_I = V_{CCI} (ISO7741FT)		I_{CC1}		6.1	7.5	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.5	5.7	
			I_{CC2}		3.1	4.5	
		10Mbps	I_{CC1}		4.9	6.3	
			I_{CC2}		4.2	5.9	
		100Mbps	I_{CC1}		9.2	11.1	
			I_{CC2}		15.1	18.2	
ISO7741TB-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7741T)(1) V_I = 0V (ISO7741FT)		I_{CC1}		3.1	4.4	mA
			I_{CC2}		2.3	3.7	
	V_I =0V_I (ISO7741T)(1) V_I = V_{CCI} (ISO7741FT)		I_{CC1}		6.5	8	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.9	6.3	
			I_{CC2}		3.1	4.5	
		10Mbps	I_{CC1}		5.3	6.9	
			I_{CC2}		4.2	5.9	
		100Mbps	I_{CC1}		9.6	11.7	
			I_{CC2}		15.1	18.2	
ISO7742TA-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7742T)(1) V_I = 0V (ISO7742FT)		I_{CC1}		3.2	4.5	mA
			I_{CC2}		2.4	3.4	
	V_I =0V_I (ISO7742T)(1) V_I = V_{CCI} (ISO7742FT)		I_{CC1}		5.4	7	
			I_{CC2}		4.6	6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.4	5.9	
			I_{CC2}		3.6	4.8	
		10Mbps	I_{CC1}		5.1	6.7	
			I_{CC2}		4.3	5.6	
		100Mbps	I_{CC1}		12.8	15.6	
			I_{CC2}		12	14.4	

V_{CC1} = V_{CC2} = 3.3V ±10%, R_L = 50Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7742TB-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7742T)(1) V_I = 0V (ISO7742FT)		I_{CC1}		3.5	5	mA
			I_{CC2}		2.4	3.4	
	V_I =0V_I (ISO7742T)(1) V_I = V_{CCI} (ISO7742FT)		I_{CC1}		5.8	7.6	
			I_{CC2}		4.6	6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.7	6.4	
			I_{CC2}		3.6	4.8	
		10Mbps	I_{CC1}		5.5	7.3	
			I_{CC2}		4.3	5.6	
		100Mbps	I_{CC1}		13.2	16	
			I_{CC2}		12	14.4	

(1) V_{CCI} = Input-side V_{CC}

5.14 Electrical Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA	V_{CCO} - 0.2(1)	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA		0.05	0.2	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-10			µA
CMTI(2)	Common mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1200V	100	150		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) CMTI is measured only on digital isolator independent of transformer driver

5.15 Supply Current Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10%, R_L = 50 Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7741TA-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7741T)(1) V_I = 0V (ISO7741FT)		I_{CC1}		2.7	3.7	mA
			I_{CC2}		2.3	3.7	
	V_I =0V_I (ISO7741T)(1) V_I = V_{CCI} (ISO7741FT)		I_{CC1}		6	7.3	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.4	5.6	
			I_{CC2}		3	4.5	
		10Mbps	I_{CC1}		4.7	6.1	
			I_{CC2}		3.9	5.5	
		100Mbps	I_{CC1}		8	9.7	
			I_{CC2}		12.1	14.7	
ISO7741TB-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7741T)(1) V_I = 0V (ISO7741FT)		I_{CC1}		3	4.2	mA
			I_{CC2}		2.3	3.7	
	V_I =0V_I (ISO7741T)(1) V_I = V_{CCI} (ISO7741FT)		I_{CC1}		6.3	7.8	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.7	6	
			I_{CC2}		3	4.5	
		10Mbps	I_{CC1}		5	6.5	
			I_{CC2}		3.9	5.5	
		100Mbps	I_{CC1}		8.3	10.1	
			I_{CC2}		12.1	14.7	
ISO7742TA-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7742T)(1) V_I = 0V (ISO7742FT)		I_{CC1}		3.1	4.3	mA
			I_{CC2}		2.3	3.4	
	V_I =0V_I (ISO7742T)(1) V_I = V_{CCI} (ISO7742FT)		I_{CC1}		5.3	6.9	
			I_{CC2}		4.6	5.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.3	5.7	
			I_{CC2}		3.5	4.7	
		10Mbps	I_{CC1}		4.8	6.4	
			I_{CC2}		4.1	5.4	
		100Mbps	I_{CC1}		10.6	13	
			I_{CC2}		9.9	12	

V_{CC1} = V_{CC2} = 2.5V ±10%, R_L = 50 Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7742TB-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7742T)(1) V_I = 0V (ISO7742FT)		I_{CC1}		3.4	4.8	mA
			I_{CC2}		2.3	3.4	
	V_I =0V_I (ISO7742T)(1) V_I = V_{CCI} (ISO7742FT)		I_{CC1}		5.6	7.3	
			I_{CC2}		4.6	5.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		4.5	6.1	
			I_{CC2}		3.5	4.7	
		10Mbps	I_{CC1}		5.1	6.8	
			I_{CC2}		4.1	5.4	
		100Mbps	I_{CC1}		10.9	13.4	
			I_{CC2}		9.9	12	

(1) V_{CCI} = Input-side V_{CC}

5.16 Switching Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		6	10.7	17	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0	6.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.4	ns
t_r	Output signal rise time			2.4	3.9	ns
t_f	Output signal fall time			2.4	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.8		ns
t_{BBM}	Break-before-make time (ISO774xTA-Q1)	Measured as voltage with R_L = 50Ω to V_{CC}		115		ns
t_{BBM}	Break-before-make time (ISO774xTB-Q1)	Measured as voltage with R_L = 50Ω to V_{CC}		90		ns
t_{SS}	Soft-start time (ISO774xTA-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	1	2.2	8	ms
t_{SS}	Soft-start time (ISO774xTB-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	1	4.25	8	ms
$t_{SSdelay}$	Soft-start time delay	From power up to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	3.5	8.5	18	ms

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.17 Switching Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		6	12	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.1	6.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5	ns
t_r	Output signal rise time			1.3	3	ns
t_f	Output signal fall time			1.3	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.9		ns
t_{BBM}	Break-before-make time (ISO774xTA-Q1)	Measured as voltage with R_L = 50Ω to V_{CC}		115		ns
t_{BBM}	Break-before-make time (ISO774xTB-Q1)	Measured as voltage with R_L = 50Ω to V_{CC}		90		ns
t_{SS}	Soft-start time (ISO774xTA-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	1	2.2	8	ms
t_{SS}	Soft-start time (ISO774xTB-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	1	4.25	8	ms
$t_{SSdelay}$	Soft-start time delay	From power up to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	3.5	8.5	18	ms

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.18 Switching Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		7.5	13	21	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	6.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5.3	ns
t_r	Output signal rise time			1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.7		ns
t_{BBM}	Break-before-make time (ISO774xTA-Q1)	Measured as voltage with R_L = 50Ω to V_{CC}		115		ns
t_{BBM}	Break-before-make time (ISO774xTB-Q1)	Measured as voltage with R_L = 50Ω to V_{CC}		90		ns
t_{SS}	Soft-start time (ISO774xTA-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	1	2.2	8	ms
t_{SS}	Soft-start time (ISO774xTB-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	1	4.25	8	ms
$t_{SSdelay}$	Soft-start time delay	From power up to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	3.5	8.5	18	ms

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.19 Insulation Characteristics Curves

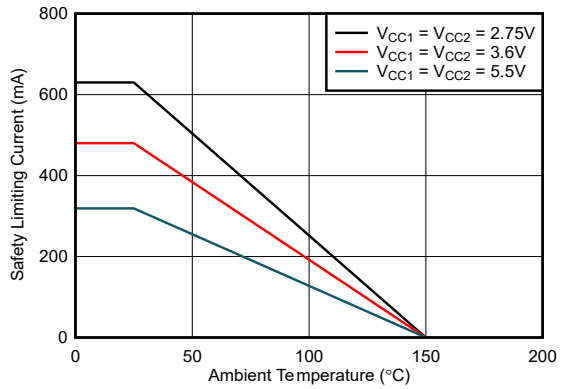


図 5-1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

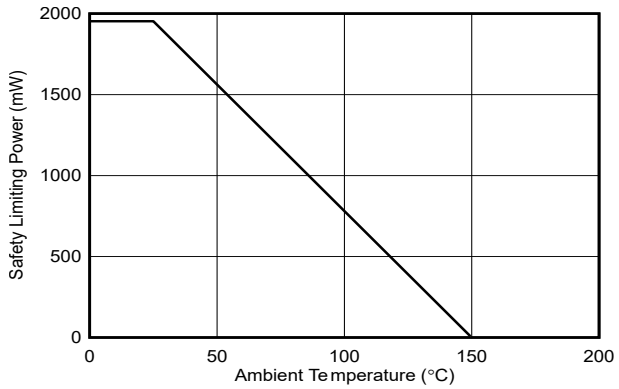
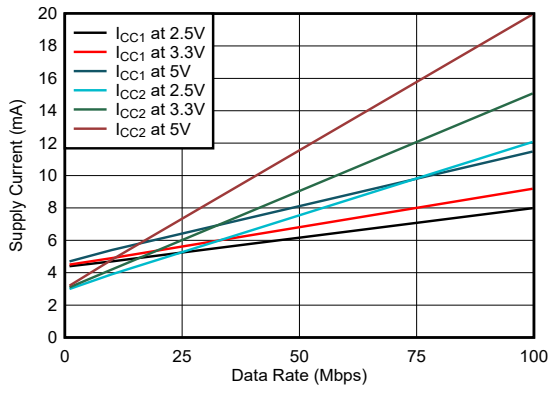


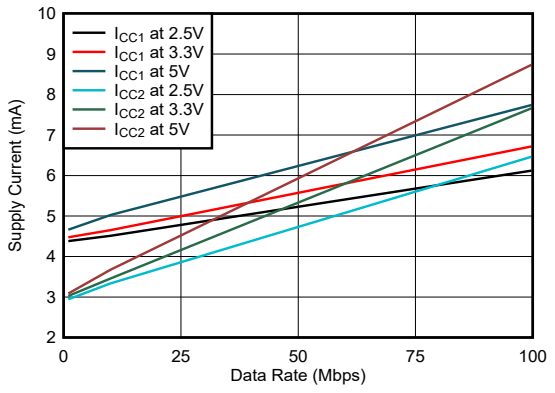
図 5-2. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

5.20 Typical Characteristics



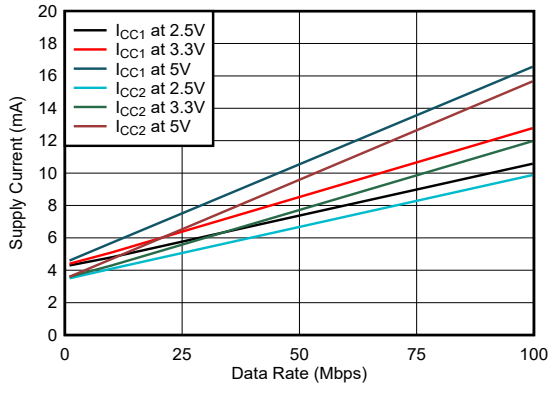
T_A = 25°C C_L = 15pF

図 5-3. ISO7741Tx-Q1 Supply Current vs. Data Rate (With 15pF Load)



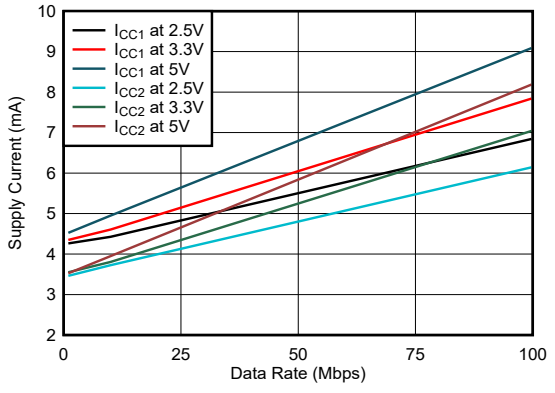
T_A = 25°C C_L = No Load

図 5-4. ISO7741Tx-Q1 Supply Current vs. Data Rate (With No Load)



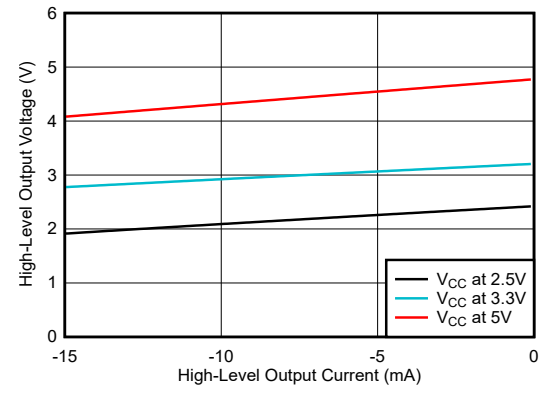
T_A = 25°C C_L = 15pF

図 5-5. ISO7742Tx-Q1 Supply Current vs. Data Rate (With 15pF Load)



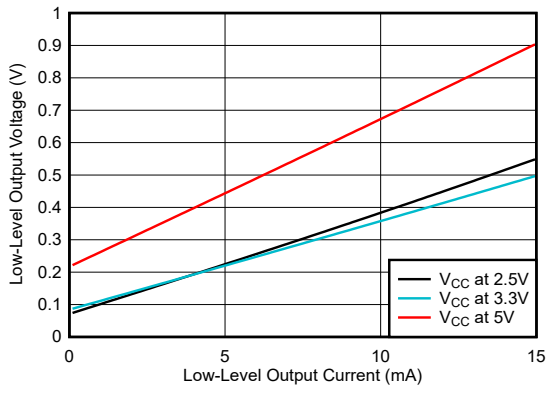
T_A = 25°C C_L = No Load

図 5-6. ISO7742Tx-Q1 Supply Current vs. Data Rate (With No Load)



T_A = 25°C

図 5-7. High-Level Output Voltage vs. High-level Output Current



T_A = 25°C

図 5-8. Low-Level Output Voltage vs. Low-Level Output Current

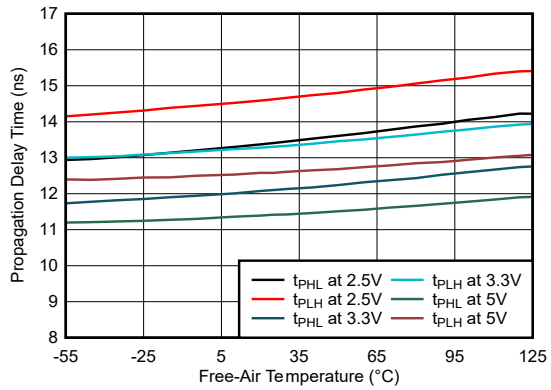
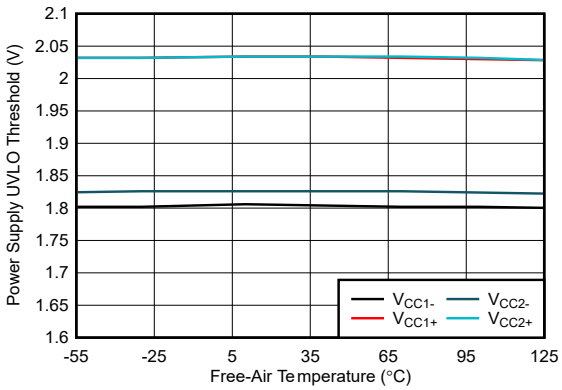
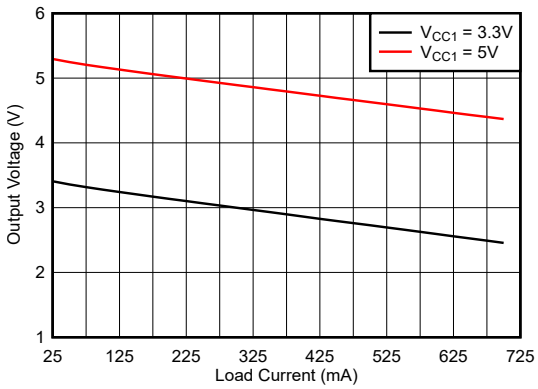


図 5-9. Propagation Delay Time vs. Free-Air Temperature



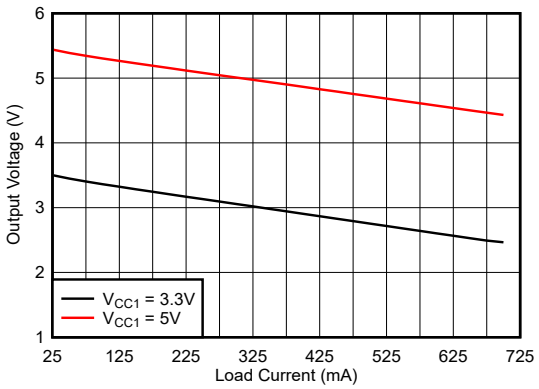
T_A = 25°C C_L = No Load

図 5-10. Power Supply Undervoltage Threshold vs. Free-Air Temperature



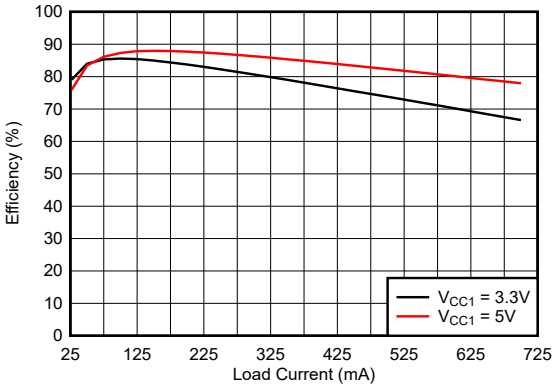
ISO774xTA-Q1 + Wurth 750315240

図 5-11. ISO774xTA-Q1 Output Voltage vs. Load Current



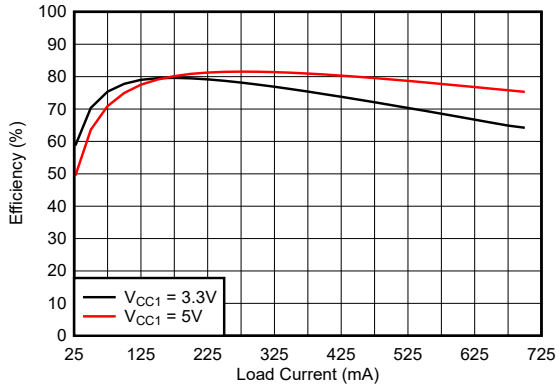
ISO774xTB-Q1 + Wurth 750315371

図 5-12. ISOO774xTB-Q1 Output Voltage vs. Load Current



ISO774xTA-Q1 + Wurth 750315240

図 5-13. ISO774xTA-Q1 Efficiency vs. Load Current



ISO774xTB-Q1 + Wurth 750315371

図 5-14. ISOO774xTB-Q1 Efficiency vs. Load Current

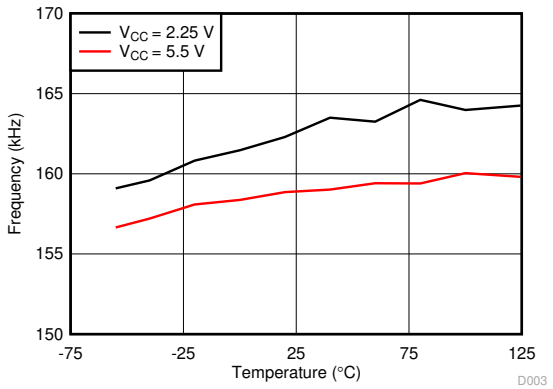


図 5-15. ISO774xTA-Q1 Frequency vs. Free-Air Temperature

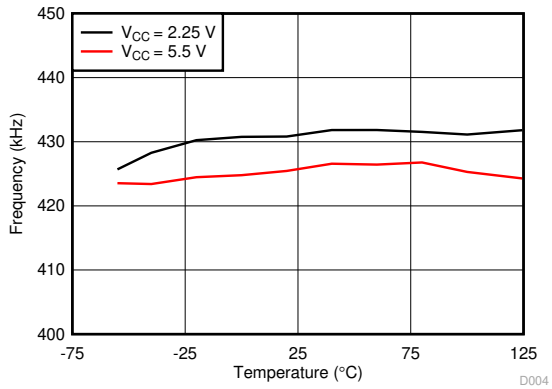
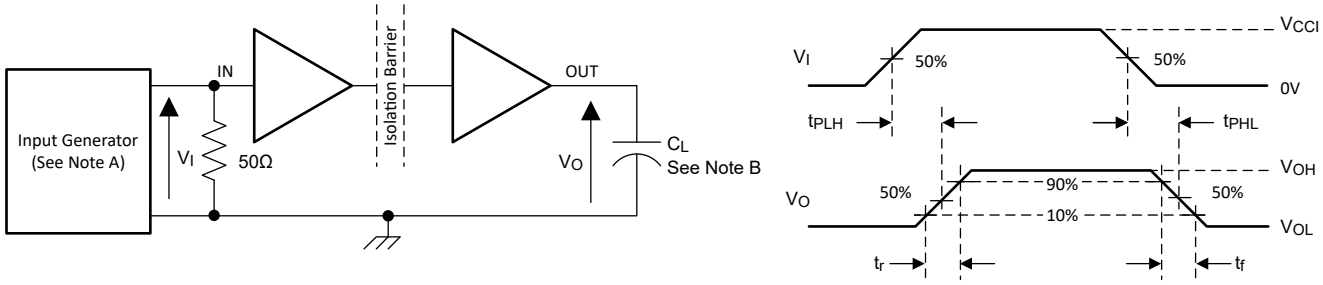


図 5-16. ISO774xTB-Q1 Frequency vs. Free-Air Temperature

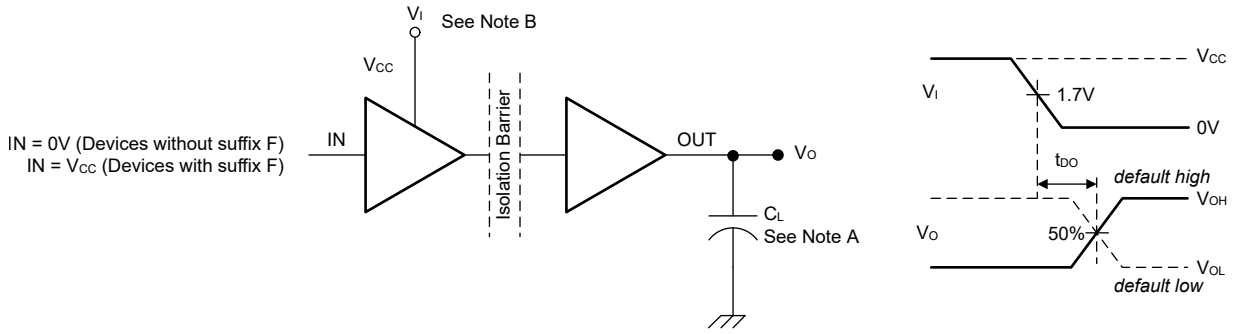
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω. At the input, 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor is not needed in actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

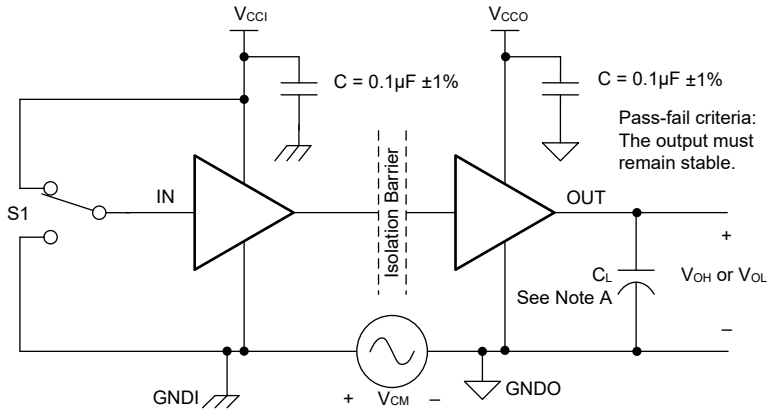
図 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10mV/ns

図 6-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

図 6-3. Common-Mode Transient Immunity Test Circuit

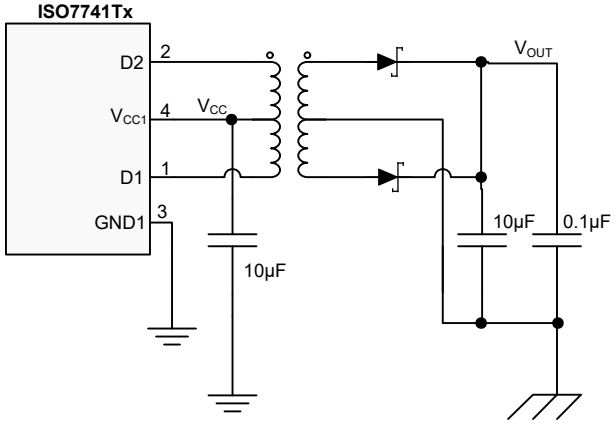


図 6-4. Measurement Circuit for Unregulated Output (TP1)

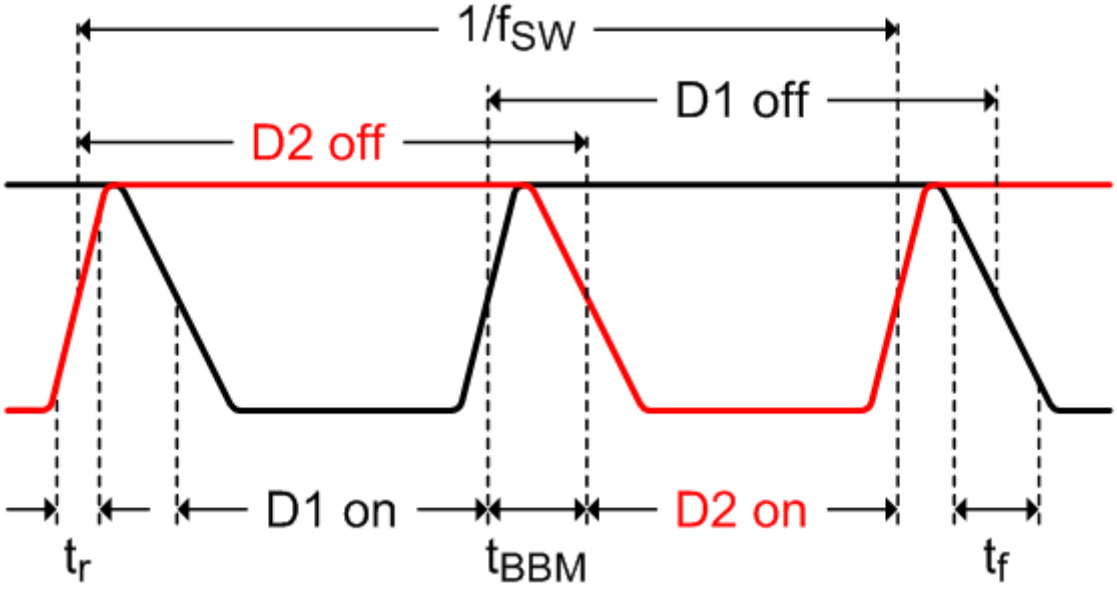


図 6-5. Timing Diagram

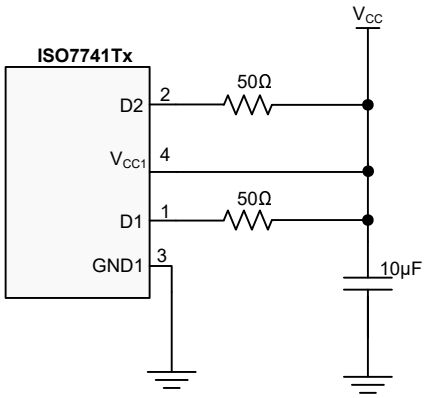


図 6-6. Test Circuit for FSW, V(slew), tBBM

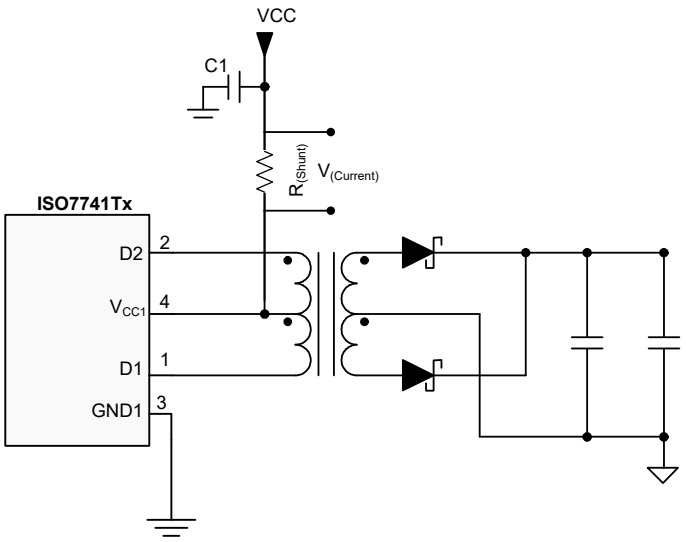


図 6-7. I(slew) Test Setup

7 Detailed Description

7.1 Overview

The ISO774xT devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO774xT also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching.

The transformer driver in ISO774xT is designed for cost competitive designs/applications, small form-factor, isolated DC/DC converters utilizing the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off. The output frequency of the oscillator is divided down by two. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. Before either one of the gates can assume logic high, the BBM logic provides a short time period during which both signals are low and both transistors are high-impedance. This short period, is required to avoid shorting out both ends of the primary. The resulting output signals, present the gate-drive signals for the output transistors.

The conceptual block diagram of a digital capacitive isolator with integrated transformer driver, 図 7-1 and 図 7-2, shows a functional block diagram of a typical channel and transformer driver.

7.2 Functional Block Diagram

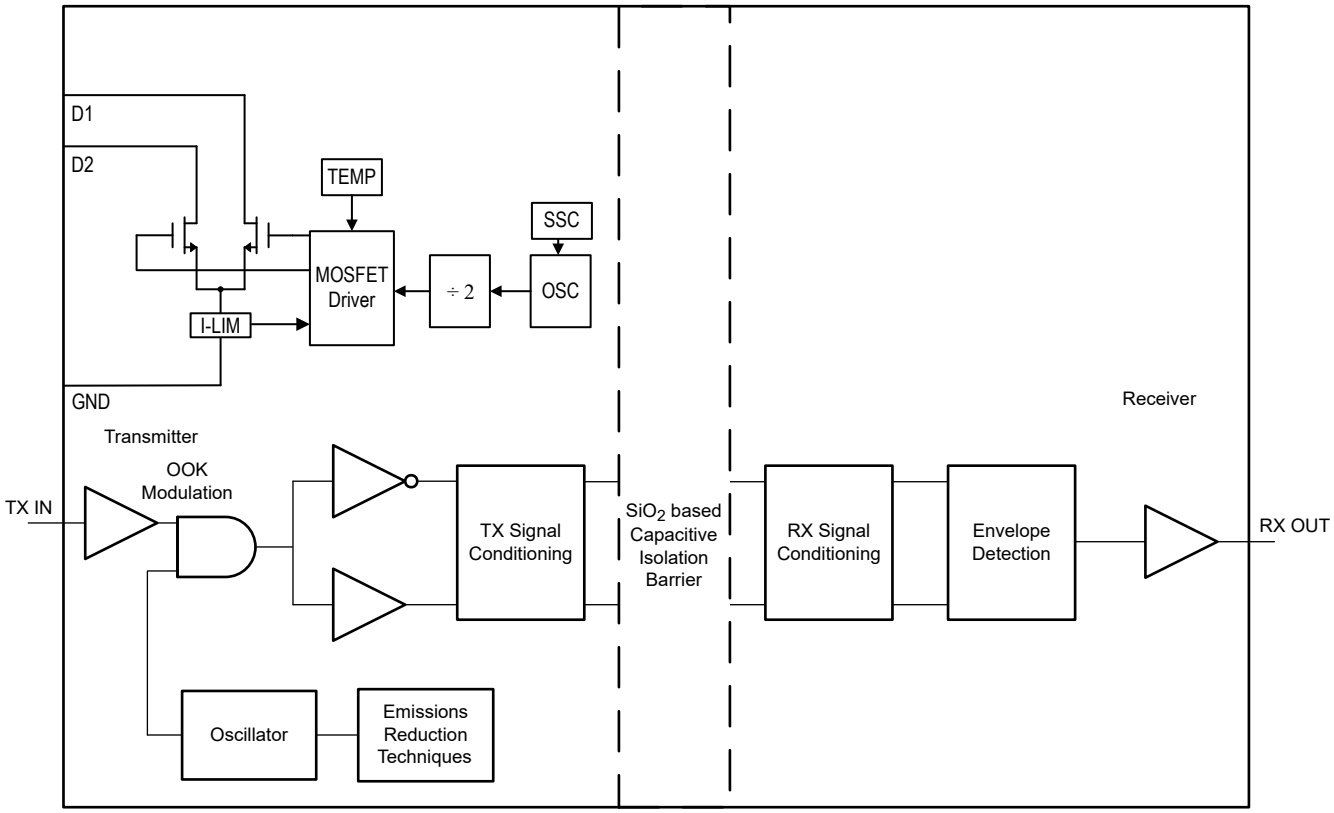


図 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

図 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

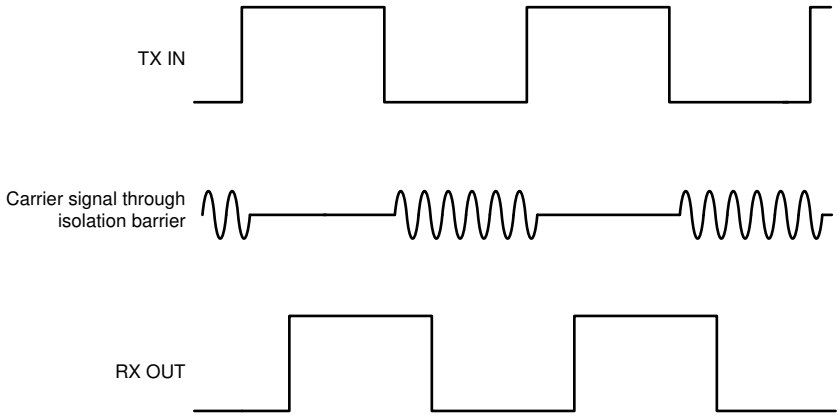


図 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

表 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	TYPICAL SWITCHING FREQUENCY	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION
ISO7741TA	3 Forward, 1 Reverse	160kHz	100Mbps	High	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7741FTA		160kHz	100Mbps	Low	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7741TB		424kHz	100Mbps	High	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7741FTB		424kHz	100Mbps	Low	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7742TA	2 Forward, 2 Reverse	160kHz	100Mbps	High	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7742FTA		160kHz	100Mbps	Low	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7742TB		424kHz	100Mbps	High	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7742FTB		424kHz	100Mbps	Low	DW-16	$5000V_{RMS}$ / $7071V_{PK}$

See *セクション 5.7* for detailed isolation ratings.

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO774xT devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

7.3.2 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary (see 図 7-3).

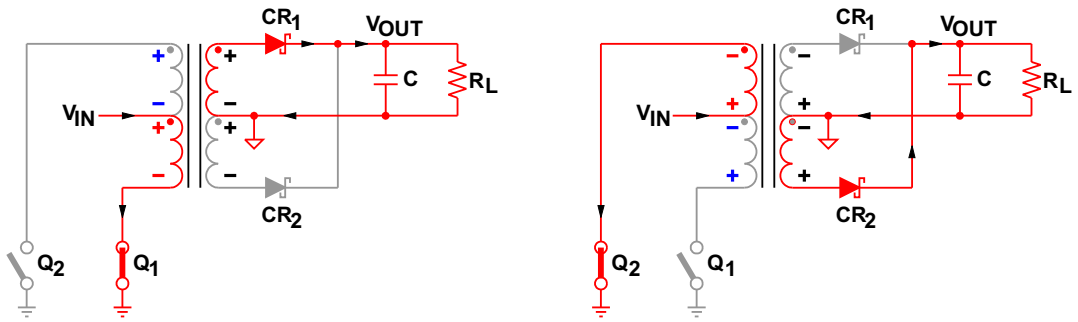


図 7-3. Switching Cycles of a Push-Pull Converter

When Q_1 conducts, V_{IN} drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the V_{IN} potential at the center-tap.

At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap to maintain the previously established current flow through Q_2, which now has turned high-impedance. The two voltage sources, each of which equaling V_{IN}, appear in series and cause a voltage potential at the open end of the primary of $2\times V_{IN}$ with regards to ground.

Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode CR_1. The secondary current starting from the upper secondary end flows through CR_1, charges capacitor C, and returns through the load impedance R_L back to the center-tap.

When Q_2 conducts, Q_1 goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a $2\times V_{IN}$ potential against ground. In this case CR_2 is forward biased while CR_1 is reverse biased and current flows from the lower secondary end through CR_2, charging the capacitor and returning through the load to the center-tap.

7.3.3 Core Magnetization

図 7-4 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q_1 conducts the magnetic flux is pushed from A to A', and when Q_2 conducts the flux is pulled back from A' to A. The difference in flux and thus in flux density is proportional to the product of the primary voltage, V_P, and the time, t_{ON}, the voltage is applied to the primary: $B \cong V_P \times t_{ON}$.

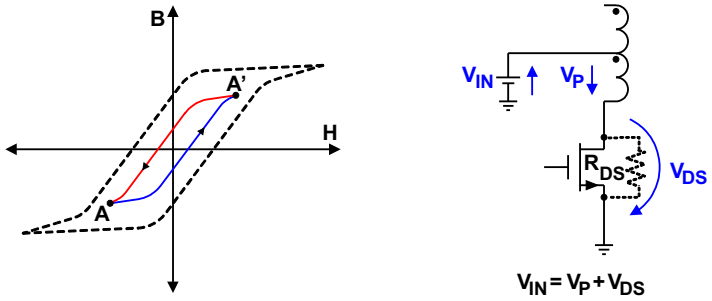


図 7-4. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of $R_{DS(on)}$

This volt-seconds (V-t) product is important as the product determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

7.4 Device Functional Modes

表 7-2 lists the functional modes for the ISO774xT devices.

表 7-2. Function Table

V_{CCI} 1	V_{CCO}	INPUT (INx)3	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is *High* for ISO774xTx and *Low* for ISO774xFTx.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO774xTx and *Low* for ISO774xFTx. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.

表 7-2. Function Table (続き)

V_{CCI} [1]	V_{CCO}	INPUT (INx)[3]	OUTPUT (OUTx)	COMMENTS
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined [2]. When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

1. V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25V); PD = Powered down (V_{CC} ≤ 1.7V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance
2. The outputs are in undetermined state when 1.7V < V_{CCI}, V_{CCO} < 2.25V.
3. A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

7.4.1 Device I/O Schematics

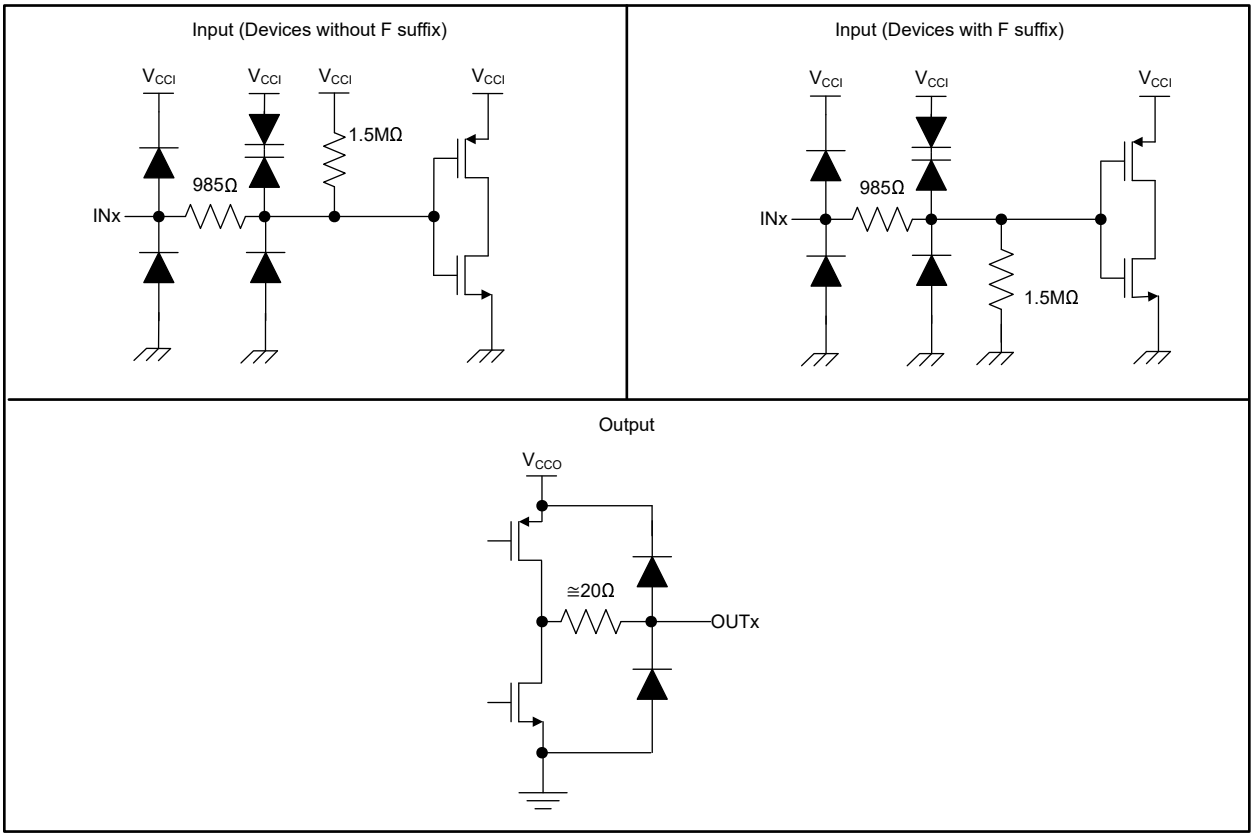


図 7-5. Device I/O Schematics

7.4.2 Start-Up Mode

When the supply voltage at V_{CC1} ramps up to 2.25V, the internal oscillator starts operating. The output stage begins switching but the amplitude of the drain signals at D1 and D2 has not reached the full maximum yet.

ISO774xT-Q1 devices support soft-start feature. Upon power up, the gate drive of the output power-MOSFET is gradually increased over a period of time from 0V to V_{CC1}. Soft-start prevents high inrush current from V_{CC1} while charging large secondary side decoupling capacitors, and also prevents overshoot in secondary voltage during power-up.

7.4.3 Operating Mode

When the device supply has reached the nominal value ±10% the oscillator is fully operating. However variations over supply voltage and operating temperature can vary the switching frequencies at D1 and D2.

7.4.4 Spread Spectrum Clocking

Radiated emissions is an important concern in high current switching power supplies. ISO774xT-Q1 transformer driver addresses this by modulating the internal clock in such a way that the emitting energy is spread over multiple frequency bins. This Spread Spectrum clocking feature greatly improves the emissions performance of the entire power supply block and hence relieves the system designer from one major concern in isolated power supply design.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a high-performance, quad-channel digital isolator with integrated high efficiency transformer driver. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to integrated transformer driver, with external transformer, the isolated supply can be generated to power the isolated side of the device and peripherals on isolated side, thus saving board space without compromising on efficiency. The voltage range is from 2.25V to 5.5V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

The device is designed for applications that have limited board space and desire more integration. The device is also designed for very high voltage applications with power transformer supporting high voltage isolation.

8.2 Typical Application

The following application circuit is shown for a 3.3V input supply commonly taken from the local, regulated microcontroller supply for SPI isolation. For 5V input voltages requiring different turn ratios refer to the transformer manufacturers and the web sites listed in Transformer Manufacturers

表 8-1. Transformer Manufacturers

MANUFACTURER	MORE INFORMATION
Coilcraft Inc.	http://www.coilcraft.com
Halo-Electronics Inc.	http://www.haloelectronics.com
Murata Power Solutions	http://www.murata-ps.com
Wurth Electronics Midcom Inc	http://www.midcom-inc.com

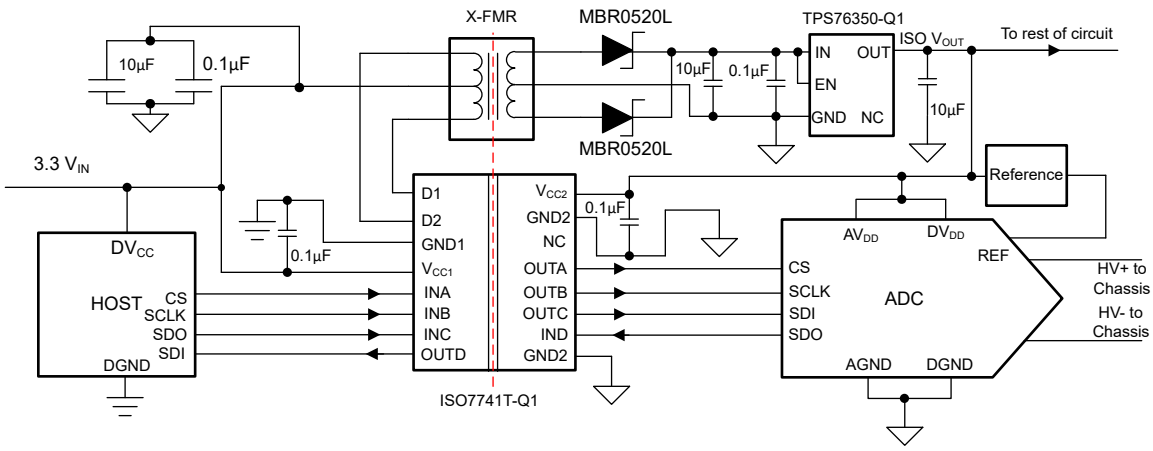


図 8-1. Isolated Power and SPI for ADC Sensing Application With ISO774xT-Q1

8.2.1 Design Requirements

To design with these devices, use the parameters listed in Design Parameters.

表 8-2. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1}	2.25V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF +1µF to 10µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF +1µF to 10µF

8.2.2 Detailed Design Procedure

The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Contrary to popular belief, the output voltage of the unregulated converter output drops significantly over a wide range in load current. The characteristic curve in 図 8-2 and 図 8-3 for example, shows that the difference between V_{OUT} at minimum load and V_{OUT} at maximum load exceeds a transceiver supply range. Therefore, to provide a stable, load independent supply while maintaining maximum possible efficiency the implementation of a low dropout regulator (LDO) is strongly advised.

8.2.2.1 Drive Capability

The transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 2.25V to 5.5V. While converter designs with higher output voltages are possible, care must be taken that higher turns ratios do not lead to primary currents that exceed the specified current limits of the device.

8.2.2.2 LDO Selection

The minimum requirements for a suitable low dropout regulator are:

- The current drive capability must slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore, for a load current of 550mA, choose a 600mA to 700mA LDO. While regulators with higher drive capabilities are acceptable, these regulators also typically possess higher dropout voltages that reduce the overall converter efficiency.
- The internal dropout voltage, V_{DO}, at the specified load current must be as low as possible to maintain efficiency. For a low-cost 700mA LDO, a V_{DO} of 600mV at 700mA is common. Be aware; however, that this lower value is typically specified at room temperature and can increase by a factor of 2 over temperature, which in turn raises the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max} \quad (1)$$

  To determine V_I for worst-case condition, the user must take the maximum values for V_{DO} and V_O specified in the LDO data sheet for rated output current (that is, 600mA) and add these values together. The user must also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than $V_{I\text{-}min}$. If the output voltage is not, the LDO loses line-regulation and any variations at the input passes straight through to the output. Hence, below $V_{I\text{-}min}$ the output voltage follows the input and the regulator behaves like a simple conductor.
- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across $R_{DS\text{-}on}$ negligible and allowing the entire converter input voltage to drop across the primary. At this point, the secondary reaches the maximum voltage of

$$V_{S\text{-}max} = V_{IN\text{-}max} \times n \quad (2)$$

with $V_{IN\text{-}max}$ as the maximum converter input voltage and n as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than $V_{S\text{-}max}$. 表 8-3 lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters.

表 8-3. Required Maximum LDO Input Voltages for Various Push-Pull Configurations

PUSH-PULL CONVERTER				LDO
CONFIGURATION	$V_{IN\text{-}max}$ [V]	TURNS-RATIO	$V_{S\text{-}max}$ [V]	$V_{I\text{-}max}$ [V]
$3.3V_{IN}$ to $3.3V_{OUT}$	3.6	1.5 ± 3%	5.6	6 to 10
$3.3V_{IN}$ to $5V_{OUT}$	3.6	2.2 ± 3%	8.2	10
$5V_{IN}$ to $5V_{OUT}$	5.5	1.5 ± 3%	8.5	10

8.2.2.3 Diode Selection

A rectifier diode must always possess low-forward voltage to provide as much voltage to the converter output as possible. When used in high-frequency switching applications, such as the ISO774xTx-Q1 however, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs. A good choice for low-volt applications and ambient temperatures of up to 85°C is the low-cost Schottky rectifier MBR0520L with a typical forward voltage of 275mV at 100mA forward current. For higher output voltages such as ±10V and above use the MBR0530 which provides a higher DC blocking voltage of 30V.

Lab measurements have shown that at temperatures higher than 100°C the leakage currents of the above Schottky diodes increase significantly. These conditions can cause thermal runaway leading to the collapse of the rectifier output voltage. Therefore, for ambient temperatures higher than 85°C use low-leakage Schottky diodes, such as RB168MM-40.

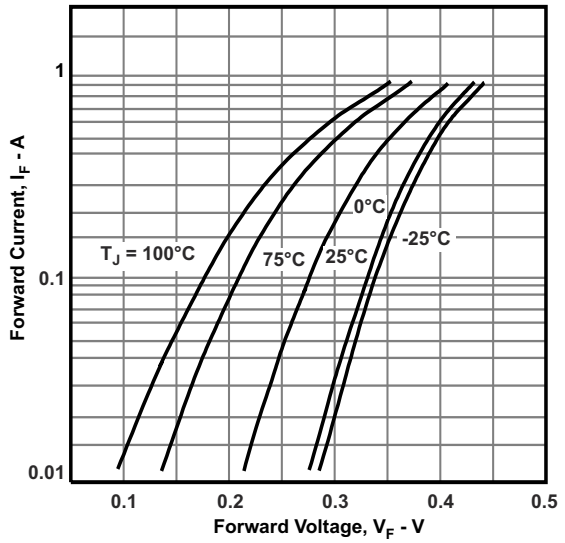


図 8-2. Diode Forward Characteristics for MBR0520L

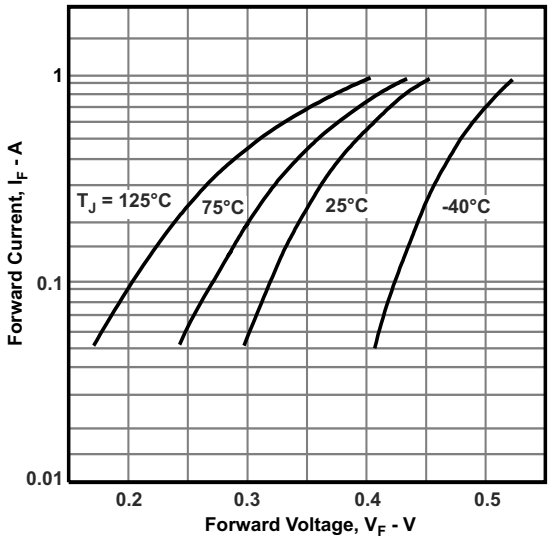


図 8-3. Diode Forward Characteristics MBR0530

8.2.2.4 Capacitor Selection

As with all high speed CMOS ICs, the device requires a bypass capacitor in the range of 10nF to 100nF.

The input bulk capacitor at the center-tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple make this capacitor 1µF to 10µF. In a 2-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layer board design with low-inductance reference planes for ground and V_{CC}, the capacitor can be placed at the supply entrance of the board. To provide low-inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smooths the output voltage. Make this capacitor 1µF to 10µF.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47nF to 100nF improves the transient response and noise rejection of the regulator.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7µF to 10µF satisfies these requirements.

8.2.2.5 Transformer Selection

8.2.2.5.1 V-t Product Calculation

To prevent a transformer from saturation, the V-t product must be greater than the maximum V-t product applied by the device. The maximum voltage delivered by the device is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the minimum V-t product for the transformer is determined through:

$$\mathrm{Vt_{min}} \geq \mathrm{V_{IN-max}} \times \frac{\mathrm{T_{max}}}{2} = \frac{\mathrm{V_{IN-max}}}{2 \times \mathrm{f_{min}}} \quad (3)$$

Taking an example of f_{min} as 138kHz for ISO774xTA-Q1 and 363kHZ for ISO774xTB-Q1 with a 5V supply, the following equations yield the minimum V-t products of:

$\mathrm{Vt_{min}} \geq \frac{5.5\mathrm{V}}{2 \times 138\mathrm{kHz}} = 20\mathrm{V\mu s}$ for ISO774xTA-Q1 applications, and

$\mathrm{Vt_{min}} \geq \frac{5.5\mathrm{V}}{2 \times 363\mathrm{kHz}} = 7.6\mathrm{V\mu s}$ for ISO774xTB-Q1 applications

Common V-t values for low-power center-tapped transformers range from 22Vµs to 150Vµs with typical footprints of 10mm x 12mm. However, transformers specifically designed for PCMCIA applications provide as little as 11Vµs and come with a significantly reduced footprint of 6mm x 6mm only.

While Vt-wise all of these transformers can be driven by the device, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

8.2.2.5.2 Turns Ratio Estimate

Assuming that the rectifier diodes and linear regulator are selected and that the transformer selected must have a V-t product of at least 11Vµs. However, before searching the manufacturer web sites for a suitable transformer, the user still needs to know the minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer typical efficiency of 97% into account:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max} \quad (4)$$

$V_{S\text{-}min}$ must be large enough to allow for a maximum voltage drop, $V_{F\text{-}max}$, across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the *LDO Selection* section, this minimum input voltage is known and by adding $V_{F\text{-}max}$ gives the minimum secondary voltage with:

$$V_{S\text{-}min} = V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max} \quad (5)$$

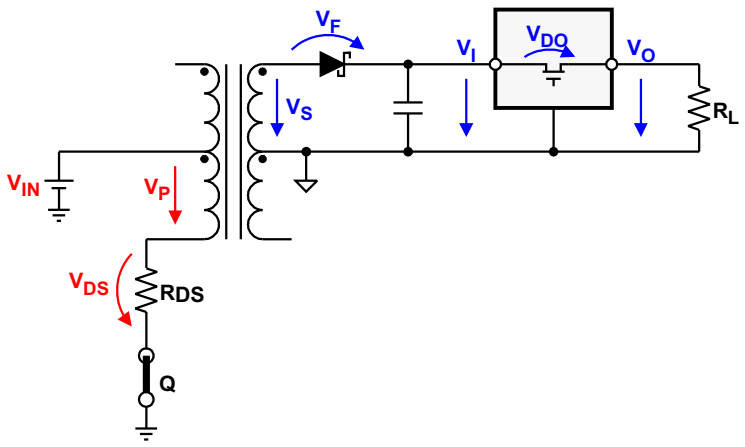


図 8-4. Establishing the Required Minimum Turns Ratio Through N_{min} = 1.031 × $V_{S\text{-}min}$ / $V_{P\text{-}min}$

Then calculating the available minimum primary voltage, $V_{P\text{-}min}$, involves subtracting the maximum possible drain-source voltage of the device, $V_{DS\text{-}max}$, from the minimum converter input voltage $V_{IN\text{-}min}$:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max} \quad (6)$$

$V_{DS\text{-}max}$ however, is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the data sheet:

$$V_{DS\text{-}max} = R_{DS\text{-}max} \times I_{Dmax} \quad (7)$$

Then inserting 式 7 into 式 6 yields:

$$V_{P\text{-}min} = V_{IN\text{-}min} - R_{DS\text{-}max} \times I_{Dmax} \quad (8)$$

and inserting 式 8 and 式 5 into 式 4 provides the minimum turns ration with:

$$n_{min} = 1.031 \times \frac{V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max}}{V_{IN\text{-}min} - R_{DS\text{-}max} \times I_{D\text{-}max}} \quad (9)$$

Example:

For a 3.3V_{IN} to 5V_{OUT} converter using the rectifier diode MBR0520L and the 5V LDO, the data sheet values taken for a load current of 600mA and a maximum temperature of 85°C are $V_{F\text{-}max}$ = 0.2V, $V_{DO\text{-}max}$ = 0.5V, and $V_{O\text{-}max}$ = 5.1V.

Then assuming that the converter input voltage is taken from a 3.3V controller supply with a maximum ±2% accuracy makes $V_{IN\text{-}min}$ = 3.234V. Finally the maximum values for drain-source resistance and drain current at 3.3V are taken from the data sheet with $R_{DS\text{-}max}$ = 0.45Ω and $I_{D\text{-}max}$ = 700mA.

Inserting the values above into 式 10 yields a minimum turns ratio of:

$$n_{min} = 1.031 \times \frac{0.2V + 0.5V + 5.1V}{3.234V - 0.45\Omega \times 700mA} \quad (10)$$

Most commercially available transformers for 3V to 5V push-pull converters offer turns ratios between 2.0 and 2.3 with a common tolerance of ±3%.

8.2.2.5.3 Recommended Transformers

Depending on the application, use the minimum configuration in 図 8-5 or standard configuration in 図 8-6.

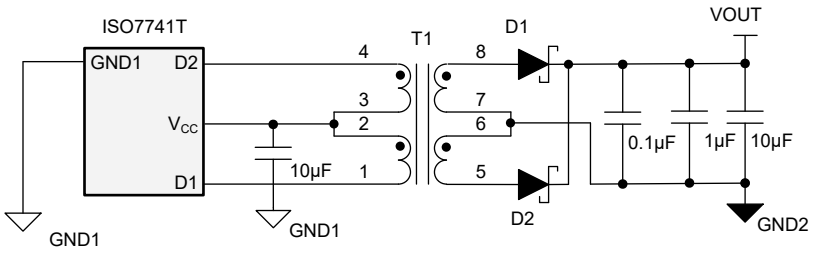


図 8-5. Unregulated Output for Low-Current Loads With Wide Supply Range

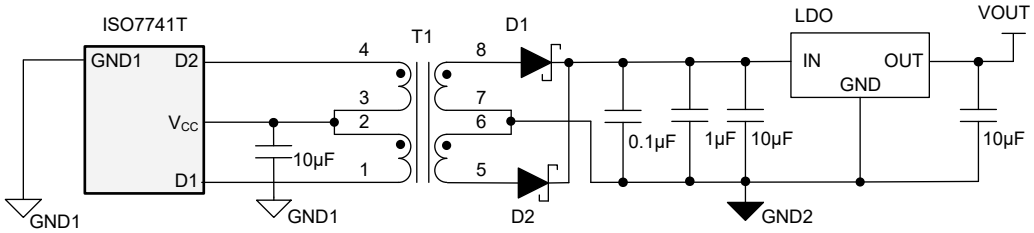


図 8-6. Regulated Output for Stable Supplies and High Current Loads

The Wurth Electronics Midcom isolation transformers in 表 8-4 are optimized designs for the device, providing high efficiency and small form factor at low-cost.

The 1:1.1 and 1:1.7 turns-ratios are designed for logic applications with wide supply rails and low load currents. These applications operate without LDO, thus achieving further cost-reduction.

表 8-4. Recommended Isolation Transformers Optimized for the Device

TURNS RATIO	V × T (Vμs)	ISOLATION (V_{RMS})	DIMENSIONS (mm)	APPLICATION	LDO(1)	ORDER NO.	MANUFACTURER
1:1.1 ±2%	7	2500	6.73 x 10.05 x 4.19	3.3V → 3.3V, 100mA, ISO774xTB-Q1	No	760390011	Wurth Electronics / Midcom
1:1.1 ±2%	11			5V → 5V, 100mA, ISO774xTB-Q1		760390012	
1:1.7 ±2%				3.3V → 5V, 100mA, ISO774xTB-Q1		760390013	
1:1.3 ±2%				3.3V → 3.3V, 100mA, ISO774xTB-Q1	Yes	760390014	
1:1.3 ±2%				5V → 5V, 100mA, ISO774xTB-Q1		760390014	
1:2.1 ±2%				3.3V → 5V, 100mA, ISO774xTB-Q1		760390015	
1.23:1 ±2%				5V → 3.3V, 100mA, ISO774xTB-Q1		750313710	
1:1.7 ±2%	8.9		8.3 x 12.6 x 4.1	3.3V → 3.3V, 1A, ISO774xTB-Q1		750316028	
1:2.1 ±2%				3.3V → 5V, 1A, ISO774xTB-Q1	No	750316029	
1.3:1 ±2%	10.8			5V → 3.3V, 1A, ISO774xTB-Q1		750316030	
1:1.1 ±2%	8.6			3.3V → 3.3V, 1A, ISO774xTB-Q1 5V → 5V, 1A, ISO774xTB-Q1		750315371	
1:1.1 ±2%	11	5000	9.14 x 12.7 x 7.37	3.3V → 3.3V, 100mA, ISO774xTB-Q1		750313734	
1:1.1 ±2%				5V → 5V, 100mA, ISO774xTB-Q1		750313734	
1:1.7 ±2%				3.3V → 5V, 100mA, ISO774xTB-Q1		750313769	
1:1.3 ±2%				3.3V → 3.3V, 100mA, ISO774xTB-Q1 5V → 5V, 100mA, ISO774xTB-Q1	Yes	750313638	
1:2.1 ±2%				3.3V → 5V, 100mA, ISO774xTB-Q1		750313626	
1.3:1 ±2%				5V → 3.3V, 100mA, ISO774xTB-Q1	No	750313638	
1:1.75 ±2%	41		12.32 x 15.41 x 11.05	3.3V → 3.3V, 1A, ISO774xTA-Q1	Yes	750316031	
1:2 ±2%				3.3V → 5V, 1A, ISO774xTA-Q1	No	750316032	
1.3:1 ±2%	42			5.0V → 3.3V, 1A, ISO774xTA-Q1		750316033	
1:1.1 ±2%	23		12.32 x 15.41 x 11.89	3.3V → 3.3V, 1A, ISO774xTA-Q1 5V → 5V, 1A, ISO774xTA-Q1		750315240	
1:3.5 ±2%	9		9.14 x 12.95 x 7.62	5V → 17.5V, 100mA,ISO774xTB-Q1		750342879	
1:3.9 ±2%			9.17 x 12.7 x 7.62	5V → 19.5V, 100mA,ISO774xTB-Q1		750343725	
1:3.75 ±2%	9.5	2500	8.3 x 12.6 x 4.1	5V → 18.75V, 100mA,ISO774xTB-Q1		78931812518	
1:4.75 ±2%				5V → 23.75V, 100mA,ISO774xTB-Q1		78931812523	
1:2.5 ±2%				5V → 12.5V, 200mA,ISO774xTB-Q1		78931812512	
1:3.13 ±2%				5V → 15.65V, 200mA,ISO774xTB-Q1		78931812515	
1:3.5 ±2%	16	6000	9.14 x 12.7 x 7.62	5V → 17.5V, 100mA,ISO774xTB-Q1		750320340	
1:1.3 ±3%	11	5000	10.4 x 12.2 x 6.1	3.3V → 3.3V, 300mA, ISO774xTB-Q1 5V → 5V, 300mA, ISO774xTB-Q1	No	HCT-SM-1.3-8-2	Bourns
1:1.5 ±3%	34.4	2500	10 x 12.07 x 5.97	3.3V → 3.3V, 1A, ISO774xTB-Q1 5V → 5V, 1A, ISO774xTA/B-Q1	Yes	DA2303-AL	Coilcraft
1:2.2 ±3%	21.5	2500	10 x 12.07 x 5.97	3.3V → 5V, 1A, ISO774xTA/B-Q1		DA2304-AL	

(1) For configurations with LDO, a higher voltage than the required output voltage is generated, to allow for LDO drop-out. Figures show the voltage and efficiency at the LDO input.

8.2.3 Application Curve

The following typical eye diagrams of the device indicates low jitter and wide open eye at the maximum data rate of 100Mbps.

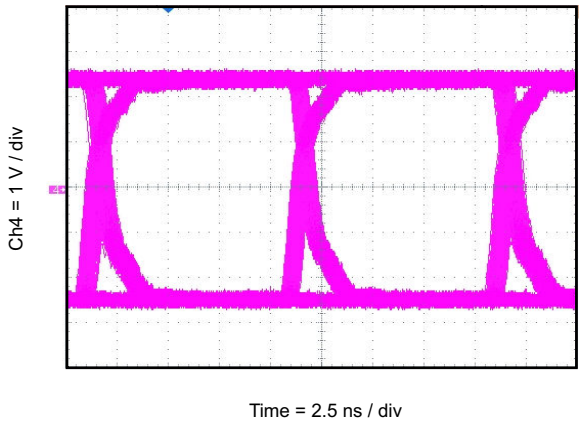


図 8-7. Eye Diagram at 100Mbps PRBS 2^{16} – 1, 5V and 25°C

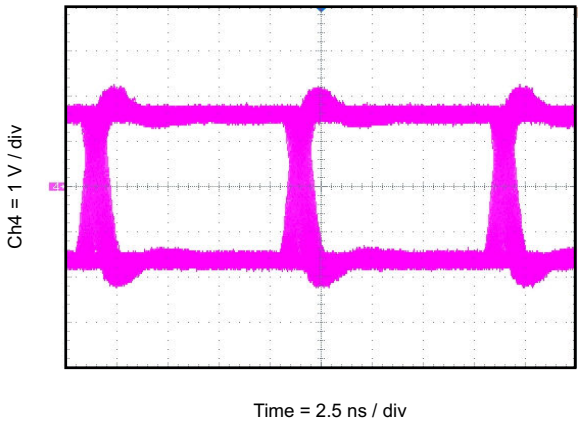


図 8-8. Eye Diagram at 100Mbps PRBS 2^{16} – 1, 3.3V and 25°C

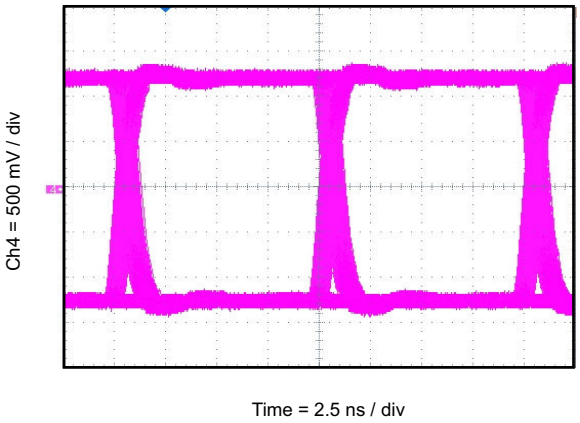


図 8-9. Eye Diagram at 100Mbps PRBS 2^{16} – 1, 2.5V and 25°C

8.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 図 8-10 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

図 8-11 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is $1500V_{RMS}$ with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, and more can further limit the working voltage of the component. The working voltage of DW-16 package is specified up to $1500V_{RMS}$. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.

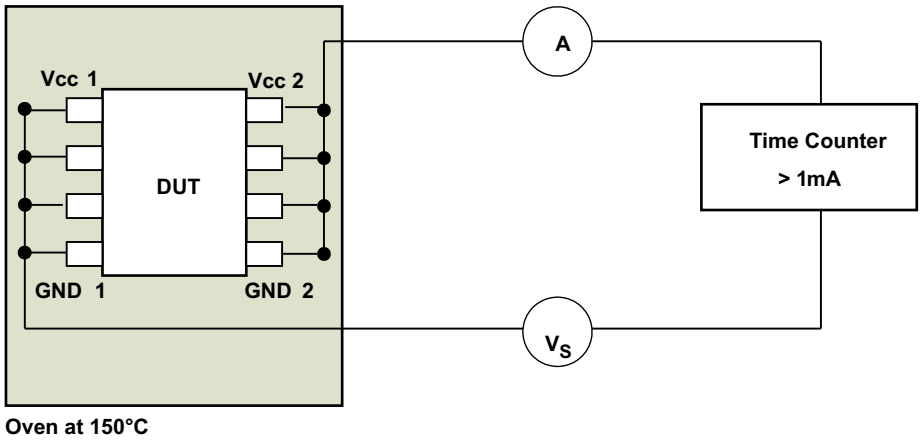


図 8-10. Test Setup for Insulation Lifetime Measurement

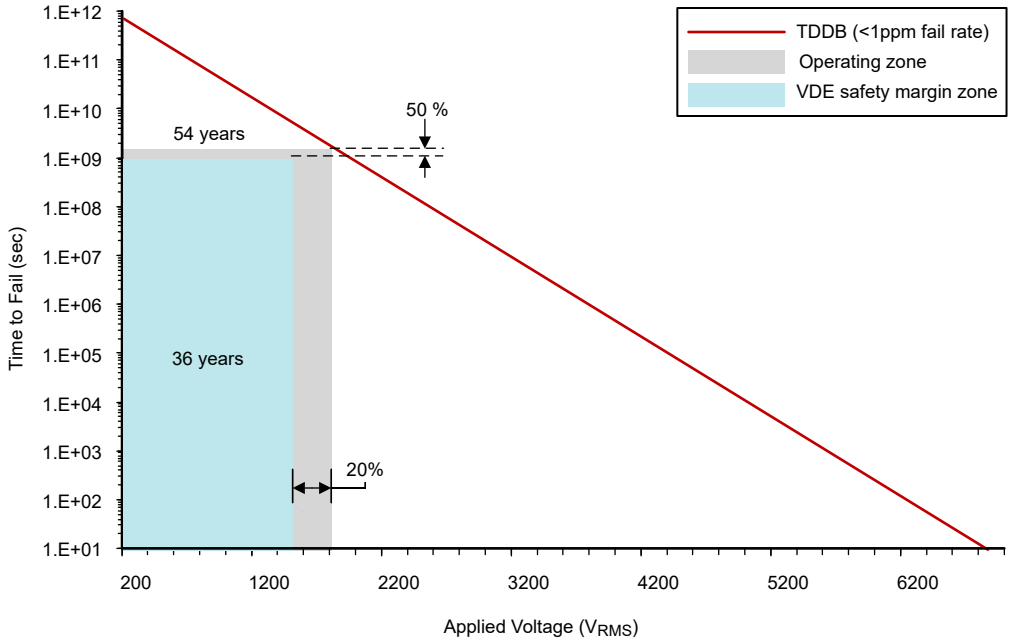


図 8-11. Insulation Lifetime Projection Data

8.2.4 System Examples

8.2.4.1 Higher Output Voltage Designs

The device can drive push-pull converters that provide high output voltages of up to 30V, or bipolar outputs of up to ±15V. Using commercially available center-tapped transformers, with relatively low turns ratios of 0.8 to 5, requires different rectifier topologies to achieve high output voltages. 図 8-12 to 図 8-14 show some of these topologies together with the respective open-circuit output voltages.

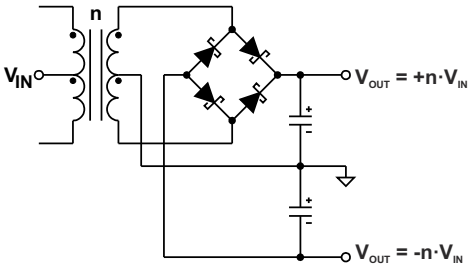


図 8-12. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs

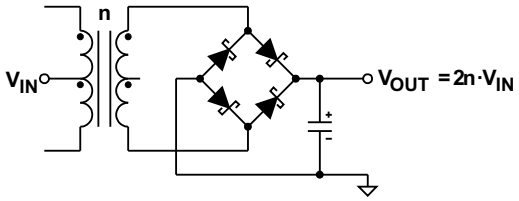


図 8-13. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Dodoubling

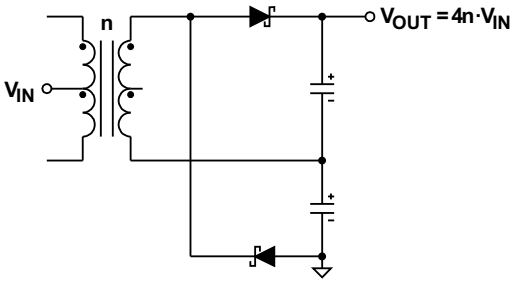


図 8-14. Half-Wave Rectifier Without Centered Ground and Center-Tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling V_{IN}

8.3 Power Supply Recommendations

The device is designed to operate in an input voltage supply range of 2.5V to 5V nominal. This input supply must be regulated within ±10%. To help provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. A 10µF capacitor must be connected close to the transformer center-tap pin for reliable power transfer. The isolated power is generated for the secondary-side with help of a transformer driver as shown in the application diagram.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 8-15). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch^2.

- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.
- A low-ESR ceramic bypass-capacitor must be connected between the V_{CC} and GND pins for both the supply. The recommended capacitor value can range from 0.1µF to 10µF. The capacitor must have a voltage rating of 10V minimum and a X5R or X7R dielectric. The optimum placement of decap is closest to the V_{CC} and GND pins.
- The connections between the device D1 and D2 pins and the transformer primary endings, and the connection of the device V_{CC1} pin and the transformer center-tap must be as close as possible for minimum trace inductance. And 10µF capacitor must be connected close to the transformer center-tap pin. Length matching of D1 and D2 traces provide the best performance in efficiency and EMI.
- The rectifier diodes must be Schottky diodes with low forward voltage in the 10mA to 100mA current range to maximize efficiency.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating below 150Mbps, (or rise and fall times higher than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to the lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

8.4.2 Layout Example

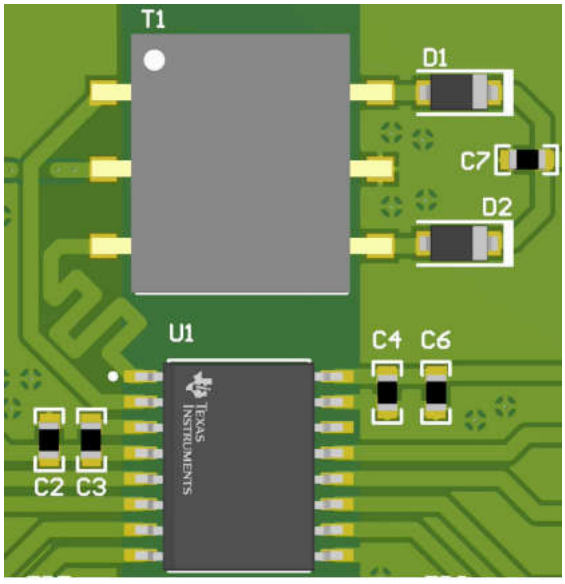


図 8-15. Example Layout

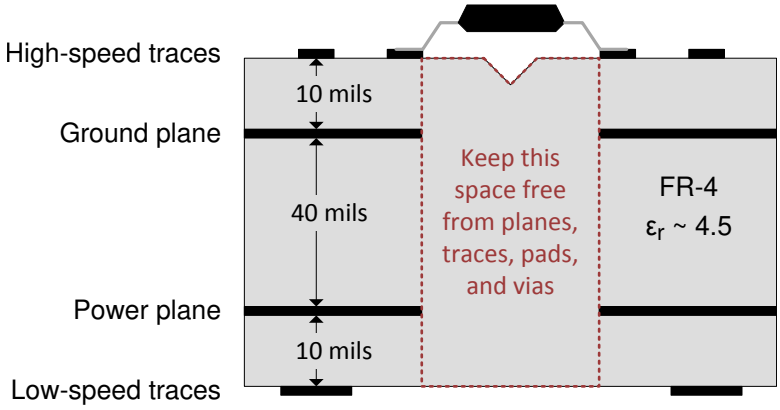


図 8-16. Example PCB Stackup

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*, application note

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (July 2024) to Revision B (January 2025) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- 新しいスピン ISO7742Tx-Q1 を追加 1
- Moved the HBM and CDM values from the *Featues* section to the *ESD Ratings* table 6
- Changed CMTI TYP value from 75kV/µs to 100 kV/µs in all Electrical Characteristics tables 12
- Added new Device ISO7742Tx 13
- Changed the t_{DO} TYP value from 6µs to 0.1µs and the MAX value from 9µs to 0.3µs in all Switching Characteristics tables 18

Changes from Revision * (April 2024) to Revision A (July 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- Changed minimum CMTI from 40 to 85 in all Electrical Characteristics tables 12

11 Mechanical, Packaging, and Orderable Information

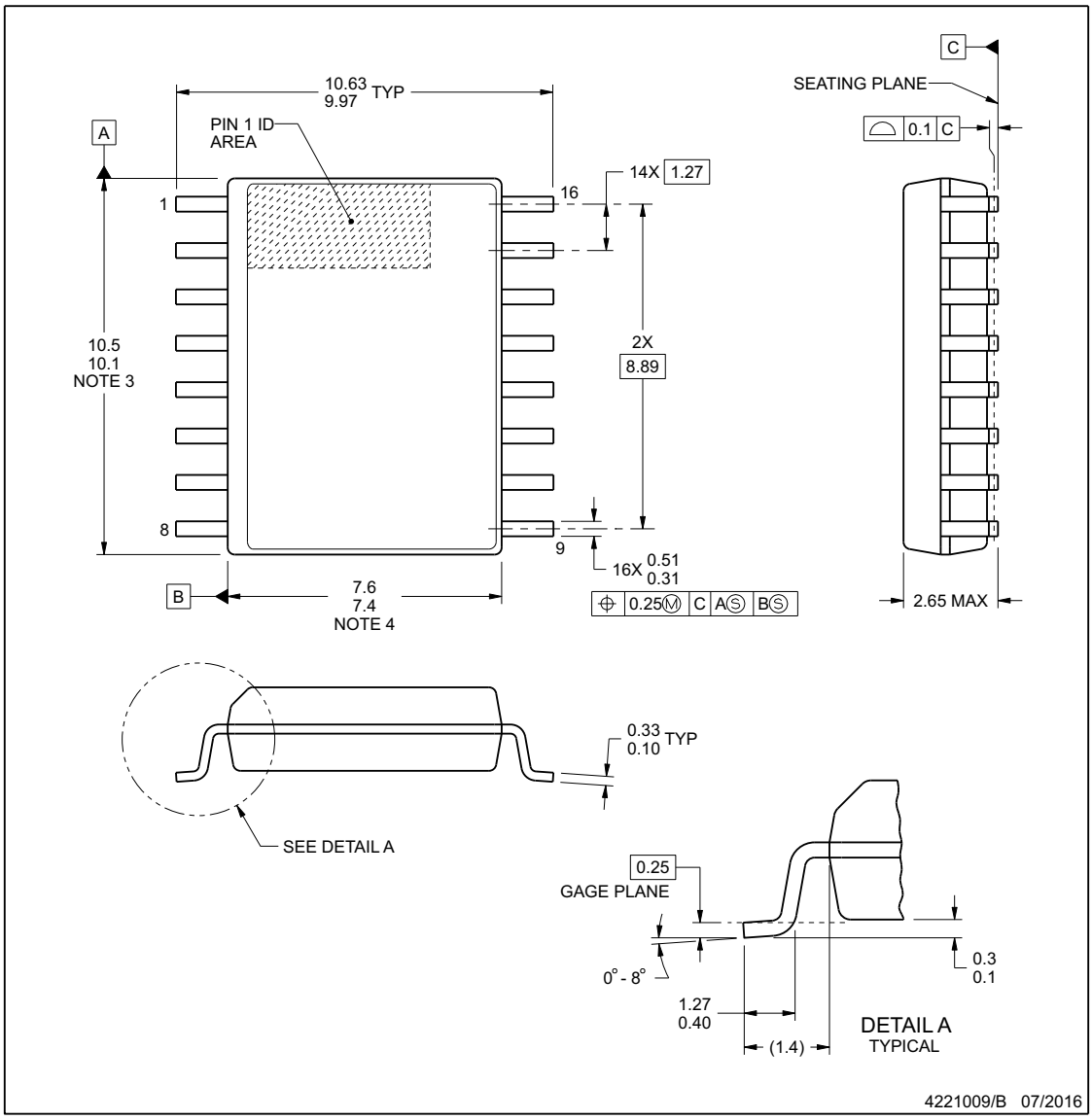
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

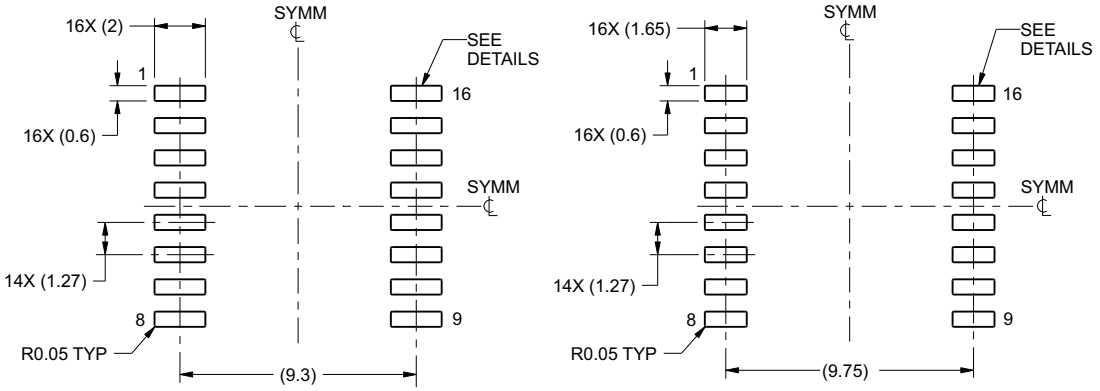
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

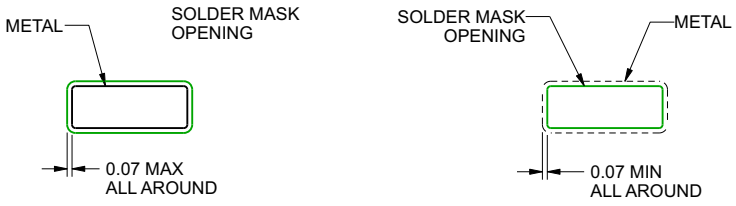
SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

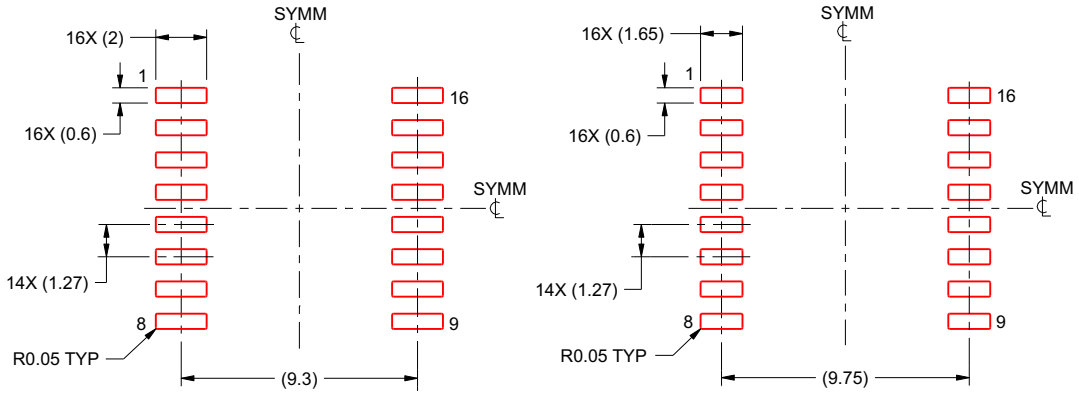
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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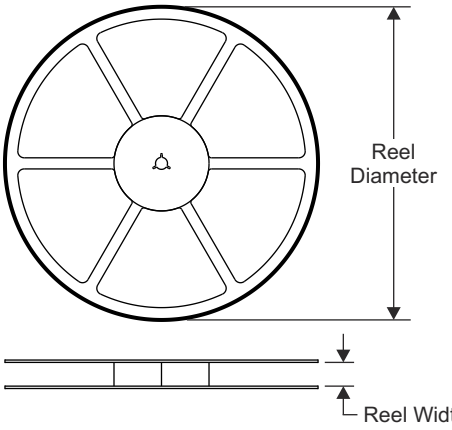
NOTES: (continued)

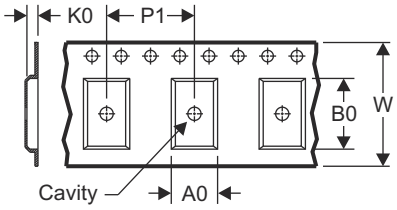
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

11.1 Tape and Reel Information

REEL DIMENSIONS

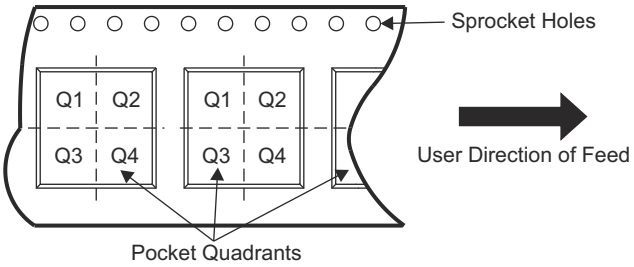


TAPE DIMENSIONS



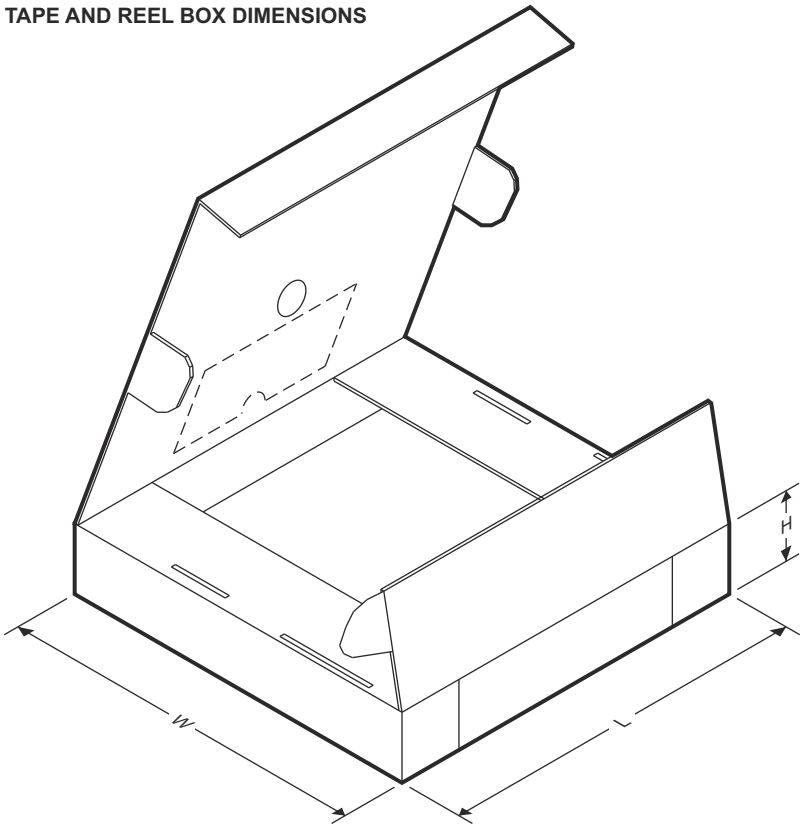
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7741FTADWRQ1	SOIC	DW	16		330	16.4	10.75	10.7	2.7	12	16	Q1
ISO7741FTBDWRQ1	SOIC	DW	16		330	16.4	10.75	10.7	2.7	12	16	Q1
ISO7741TADWRQ1	SOIC	DW	16		330	16.4	10.75	10.7	2.7	12	16	Q1
ISO7742TBDWRQ1	SOIC	DW	16		330	16.4	10.75	10.7	2.7	12	16	Q1
ISO7742FTADWRQ1	SOIC	DW	16		330	16.4	10.75	10.7	2.7	12	16	Q1
ISO7742FTBDWRQ1	SOIC	DW	16		330	16.4	10.75	10.7	2.7	12	16	Q1
ISO7742TADWRQ1	SOIC	DW	16		330	16.4	10.75	10.7	2.7	12	16	Q1
ISO7742TBDWRQ1	SOIC	DW	16		330	16.4	10.75	10.7	2.7	12	16	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7741FTADWRQ1	SOIC	DW	16		367	367	45
ISO7741FTBDWRQ1	SOIC	DW	16		367	367	45
ISO7741TADWRQ1	SOIC	DW	16		367	367	45
ISO7741TBDWRQ1	SOIC	DW	16		367	367	45
ISO7742FTADWRQ1	SOIC	DW	16		367	367	45
ISO7742FTBDWRQ1	SOIC	DW	16		367	367	45
ISO7742TADWRQ1	SOIC	DW	16		367	367	45
ISO7742TBDWRQ1	SOIC	DW	16		367	367	45

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7741FTADWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7741FTA	Samples
ISO7741FTBDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7741FTB	Samples
ISO7741TADWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7741TA	Samples
ISO7741TBDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7741TB	Samples
ISO7742FTADWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7742FTA	Samples
ISO7742FTBDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7742FTB	Samples
ISO7742TADWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7742TA	Samples
ISO7742TBDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7742TB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

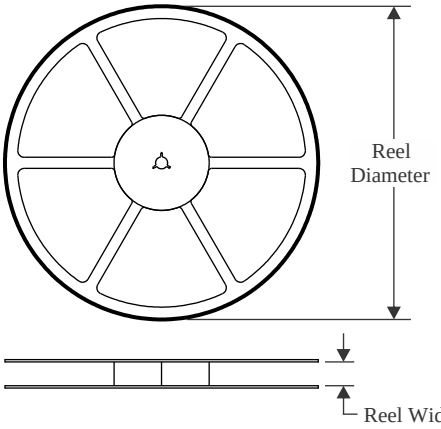
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

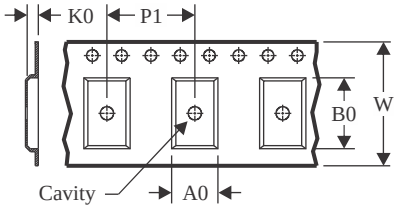
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

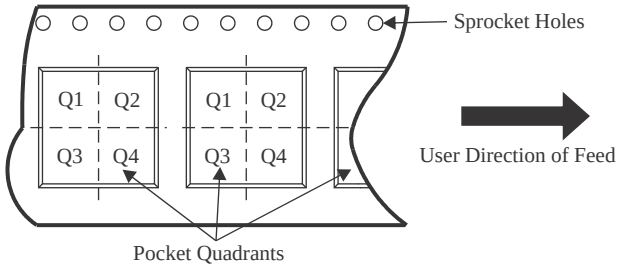


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

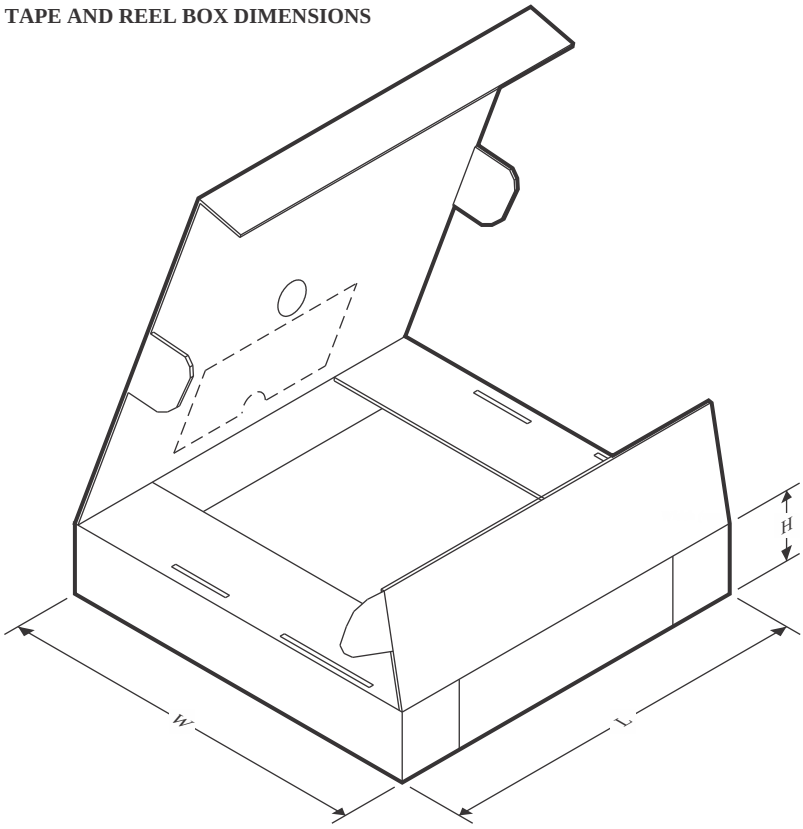
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7741FTADWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FTBDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741TADWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741TBDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742FTADWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742FTBDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742TADWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742TBDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7741FTADWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7741FTBDWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7741TADWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7741TBDWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7742FTADWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7742FTBDWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7742TADWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7742TBDWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0

GENERIC PACKAGE VIEW

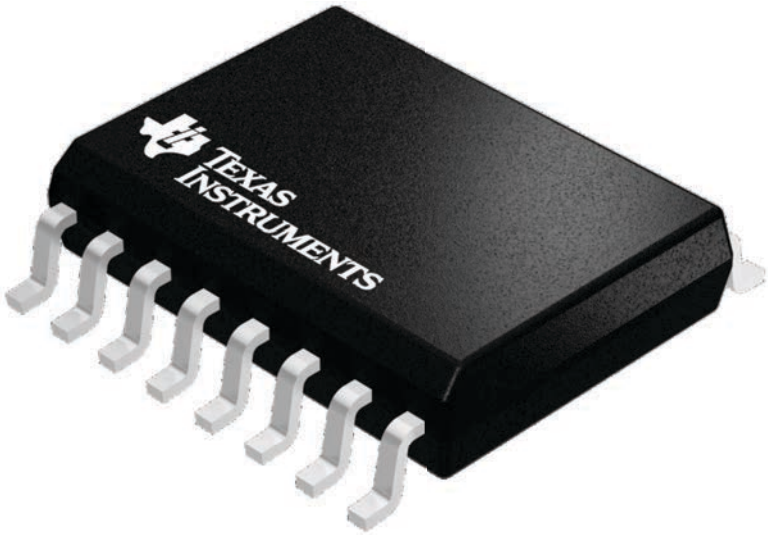
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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