INA826S 高精度、消費電流200µA、3V～36V電源、計測アンプ レール・ツー・レール出力およびシャットダウン機能搭載

1 特長

- 入力同相範囲にV-を含む
- 同相信号除去:
  - 104dB (最小値、G = 10)
  - 100dB (5kHzでの最小値、G = 10)
- 電源電圧除去: 100dB (最小値、G = 1)
- 低いオフセット電圧: 最大150µV
- ゲイン・ドリフト係数: 1 ppm/℃ (G = 1)、35 ppm/℃ (G > 1)
- ノイズ: 18 nV/√Hz、G ≥ 100
- 帯域幅: 1MHz (G = 1)、60kHz (G = 100)
- ±40Vまで入力を保護
- レール・ツー・レール出力
- 消費電流: 200µA
  - シャットダウン時電流: 2µA
- 電源電圧範囲:
  - 単一電源: 3V～36V
  - デュアル電源: ±1.5V～±18V
- 定格温度範囲:
  -40℃～+125℃
- パッケージ: 3mm×3mm VSON

2 アプリケーション

- 産業用プロセス制御
- サーキット・ブレーカ
- バッテリ・テスタ
- ECGアンプ
- パワー・オートメーション
- 医療用計測機器
- ポータブル機器

3 概要

INA826Sデバイスは、超低消費電力、シャットダウン機能付きで、幅広い単電源またはデュアル電源電圧範囲で動作する低コストの計測アンプです。単一の外付け抵抗によって、1～1000の範囲でゲインを設定できます。ゲイン・ドリフト係数が35ppm/℃ (最大値)と小さいため、G > 1の場合でも、温度変化に対して優れた安定性を示します。

INA826Sは、5kHzまでの周波数にわたり、100dB (G = 10)を超える、優れた同相信号除去比を実現するよう最適化されています。G = 1では、負の電源から正の電源の1V上までのすべての入力同相範囲について、同相信号除去比は84dBを超えます。INA826Sはレール・ツー・レール出力を使用しているため、3V単電源や、±18Vまでのデュアル電源による低電圧動作に適しています。

シャットダウン・ピンを使用すると、消費電流は2µA未満に低減します。回路を追加して、電源を超える入力に対して入力電流を8mA未満に制限することで、最高±40Vまでの過電圧に対して入力が保護されます。

INA826Sは、10ピン、3mm×3mmのVSON表面実装パッケージで供給されます。

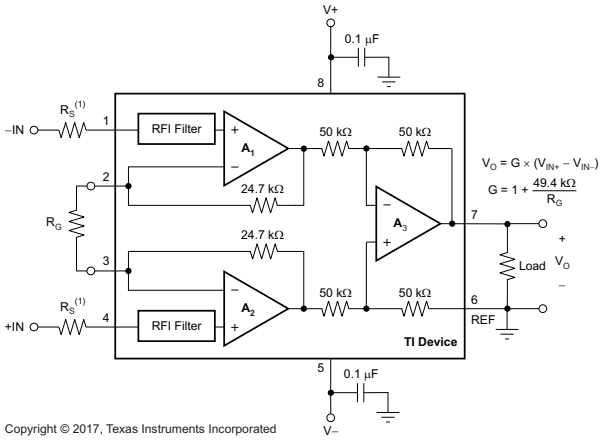
INA826Sは、-40℃～+125℃の温度範囲について動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
INA826S	VSON (10)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

INA826Sの簡略化された内部回路図



目次

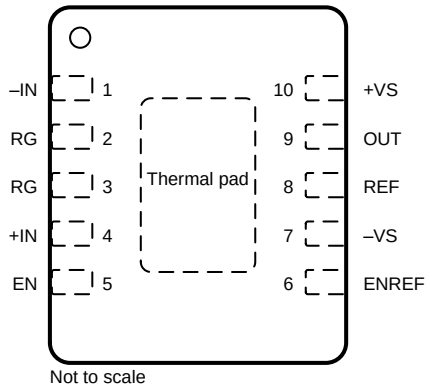
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年5月発行のものから更新	**Page**
• Changed output stage offset voltage from 700 µV to 1000 µV	5

5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Not to scale

Pin Functions

NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable pin; active low with respect to ENREF
ENREF	6	I	Enable pin reference
–IN	1	I	Negative (inverting) input
+IN	4	I	Positive (noninverting) input
OUT	9	O	Output
REF	8	I	Reference input. This pin must be driven by low impedance.
RG	2, 3	—	Gain setting pins. Place a gain resistor between pin 2 and pin 3.
–VS	7	—	Negative supply
+VS	10	—	Positive supply
Thermal pad	Pad	—	Exposed thermal die pad on underside; connect thermal die pad to V–. Soldering the thermal pad improves heat dissipation and provides specified performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage		–20	20	V
Voltage	Signal input pins	$(-V_S) - 40$	$(+V_S) + 40$	V
	REF pin	–20	+20	
	ENREF pin	$(-V_S) - 0.3$	$(+V_S) + 0.3$	
	EN pin	$(-V_S) - 0.3$	$V_{ENREF} + 0.3$	
Current	Signal input pins	–10	10	mA
	REF pin	–10	10	
	ENREF pin	–1	1	
	EN pin	–1	1	
Output short-circuit(2)		Continuous		
Temperature	Operating, T_A	–50	150	°C
	Junction, T_J		175	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	Single-supply	3		36	V
	Dual-supply	±1.5		±18	
Specified temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA826S VSON (DRC) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Input stage offset voltage(1)	RTI			40	150	µV
		vs temperature, T_A = –40°C to +125°C			0.4	2	µV/°C
V_{OSO}	Output stage offset voltage(1)	RTI			200	1000	µV
		vs temperature, T_A = –40°C to +125°C			2	5	µV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI		90	124		dB
		G = 10, RTI		100	130		
		G = 100, RTI		110	140		
		G = 1000, RTI		120	140		
z_{id}	Differential impedance				20 || 1		GΩ || pF
z_{ic}	Common-mode impedance				10 || 5		GΩ || pF
	RFI filter, –3-dB frequency				20		MHz
V_{CM}	Operating input range(2)			V–		(V+) – 1	V
		V_S = ±3 V to ±18 V, T_A = –40°C to +125°C		See 図 12 to 図 19			
	Input overvoltage range	T_A = –40°C to 125°C				±40	V
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI	G = 1, V_{CM} = (V–) to (V+) – 1 V	82	95		dB
			G = 10, V_{CM} = (V–) to (V+) – 1 V	104	115		
			G = 100, V_{CM} = (V–) to (V+) – 1 V	120	130		
			G = 1000, V_{CM} = (V–) to (V+) – 1 V	120	130		
			G = 1, V_{CM} = (V–) to (V+) – 1 V, T_A = –40°C to +125°C	80			
		At 5 kHz, RTI	G = 1, V_{CM} = (V–) to (V+) – 1 V	84			
			G = 10, V_{CM} = (V–) to (V+) – 1 V	100			
			G = 100, V_{CM} = (V–) to (V+) – 1 V	105			
			G = 1000, V_{CM} = (V–) to (V+) – 1 V	105			
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S / 2			35	65	nA
		T_A = –40°C to +125°C				95	
I_{OS}	Input offset current	V_{CM} = V_S / 2			0.7	5	nA
		T_A = –40°C to +125°C				10	
NOISE VOLTAGE							
e_{NI}	Input stage voltage noise(3)	f = 1 kHz, G = 100, R_S = 0 Ω			18		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω			0.52		$µV_{PP}$
e_{NO}	Output stage voltage noise(3)	f = 1 kHz, G = 1, R_S = 0 Ω			110		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 1, R_S = 0 Ω			3.3		$µV_{PP}$
I_n	Noise current	f = 1 kHz			100		fA/√Hz
		f_B = 0.1 Hz to 10 Hz			5		pA_{PP}

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Input voltage range of the INA826S input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage.
(3) Total RTI voltage noise is equal to: $\sqrt{(e_{NI})^2 + \left(\frac{e_{NO}}{G}\right)^2}$.

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAIN							
G	Gain equation				1 + (49.4 kΩ / R_G)		V/V
G	Range of gain			1		1000	V/V
$_{GE}$	Gain error	G = 1, V_O = ±10 V			±0.003%	±0.020%	
		G = 10, V_O = ±10 V			±0.03%	±0.15%	
		G = 100, V_O = ±10 V			±0.04%	±0.15%	
		G = 1000, V_O = ±10 V			±0.04%	±0.15%	
	Gain vs temperature(4)	G = 1, T_A = –40°C to +125°C			±0.1	±1	ppm/°C
		G > 1, T_A = –40°C to +125°C			±10	±35	
	Gain nonlinearity	G = 1 to 100, V_O = –10 V to 10 V			1	5	ppm
		G = 1000, V_O = –10 V to 10 V			5	20	
OUTPUT							
	Voltage swing	R_L = 10 kΩ		(V–) + 0.1		(V+) – 0.15	V
	Load capacitance stability				1000		pF
Z_O	Open-loop output impedance				See 図 59		
I_{SC}	Short-circuit current	Continuous to V_S / 2			±16		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 1			1		MHz
		G = 10			500		kHz
		G = 100			60		
		G = 1000			6		
SR	Slew rate	G = 1, V_{STEP} = 10 V			1		V/µs
		G = 100, V_{STEP} = 10 V			1		
t_S	Settling time	0.01%	G = 1, V_{STEP} = 10 V		12		µs
			G = 10, V_{STEP} = 10 V		12		
			G = 100, V_{STEP} = 10 V		24		
			G = 1000, V_{STEP} = 10 V		224		
		0.001%	G = 1, V_{STEP} = 10 V		14		
			G = 10, V_{STEP} = 10 V		14		
			G = 100, V_{STEP} = 10 V		31		
			G = 1000, V_{STEP} = 10 V		278		
REFERENCE INPUT							
R_{IN}	Input impedance				100		kΩ
	Voltage range			(V–)		(V+)	V
	Gain to output				1		V/V
	Reference gain error				0.01%		
ENABLE INPUT							
	Enable threshold voltage	Referenced to ENREF pin			–0.75		V
		T_A = –40°C to +125°C				–1.0	
	Disable threshold voltage	Referenced to ENREF pin			–0.7		V
		T_A = –40°C to +125°C		–0.40			
	EN pin input current	V_{ENREF} = 1.5 V, V_{EN} = 0 V			3		µA
	ENREF pin input current	V_{ENREF} = 1.5 V, V_{EN} = 0 V			–3		µA
	EN pin voltage range			V–		V_{ENREF}	V
	ENREF voltage range			(V–) + 1.5 V		V+	V
	Enable delay				100		µs

(4) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.

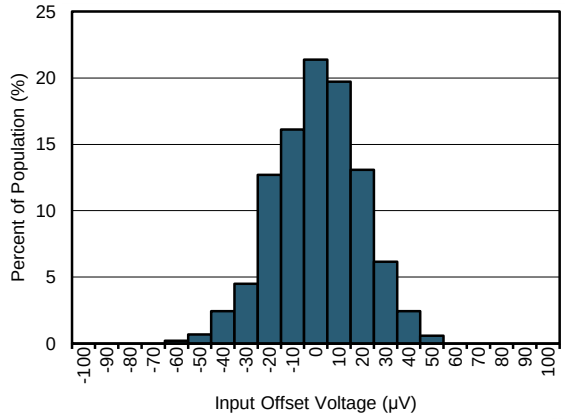
Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Power-supply voltage	Single	3		36	V
		Dual	±1.5		±18	
I_Q	Quiescent current	V_{IN} = 0 V		200	250	µA
		T_A = –40°C to +125°C			320	
I_{QSD}	Shutdown current	V_S = 3 V to 36 V, V_{IN} = 0 V		2	5	µA
		T_A = –40°C to +125°C			6	
TEMPERATURE RANGE						
	Specified		–40		125	°C
	Operating		–50		150	°C

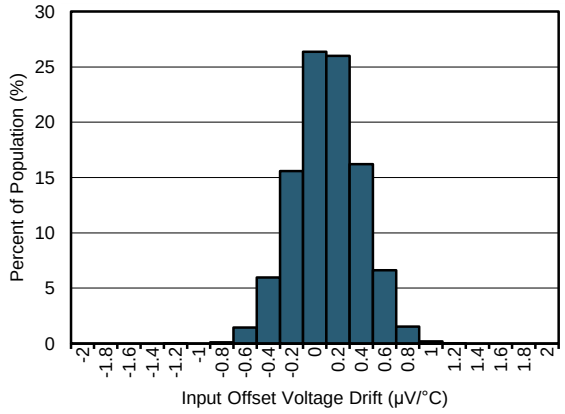
6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



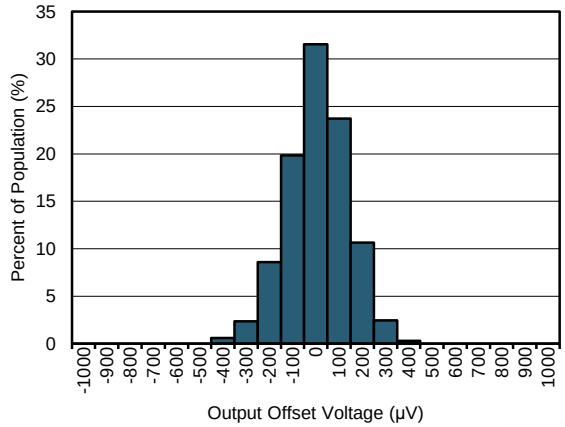
1024 units

図 1. Typical Distribution of Input Offset Voltage



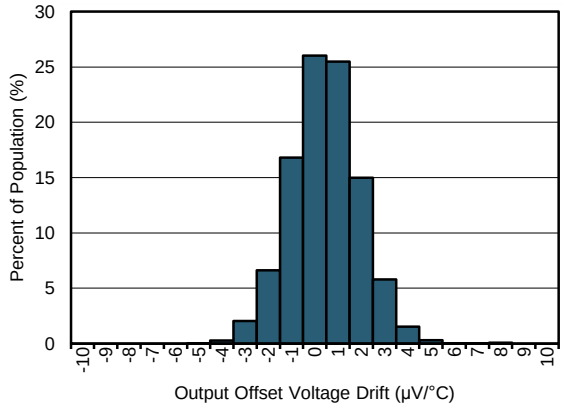
5977 units

図 2. Typical Distribution of Input Offset Voltage Drift



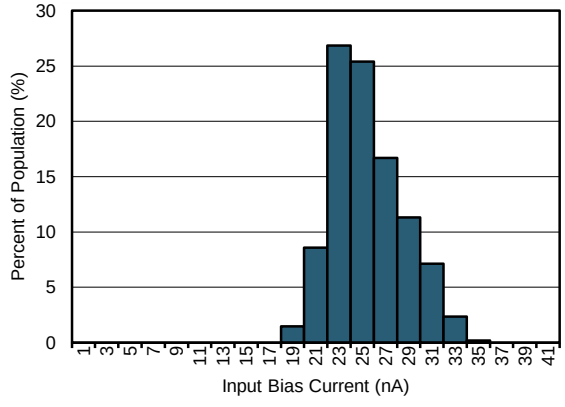
1024 units

図 3. Typical Distribution of Output Offset Voltage



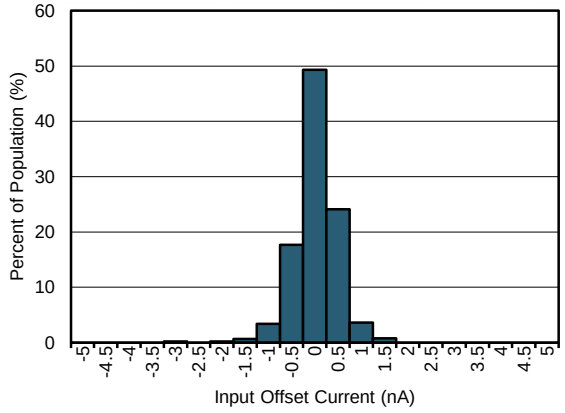
5977 units

図 4. Typical Distribution of Output Offset Voltage Drift



1024 units

図 5. Typical Distribution of Input Bias Current



1024 units

図 6. Typical Distribution of Input Offset Current

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

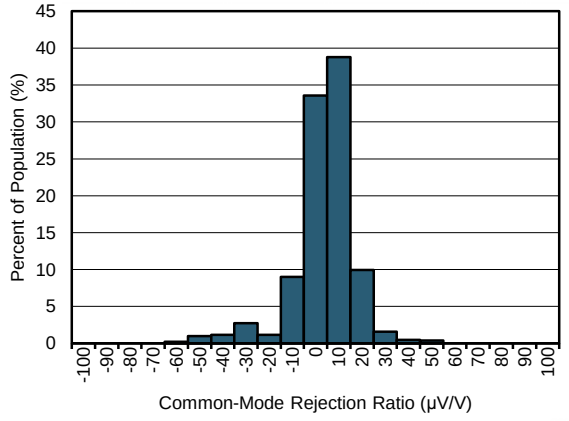


図 7. Typical Distribution of CMRR (G = 1)

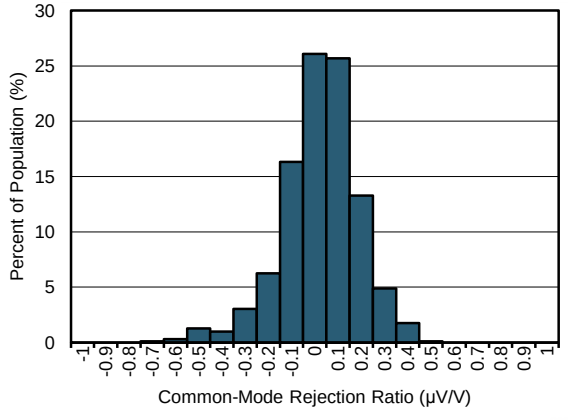


図 8. Typical Distribution of CMRR (G = 100)

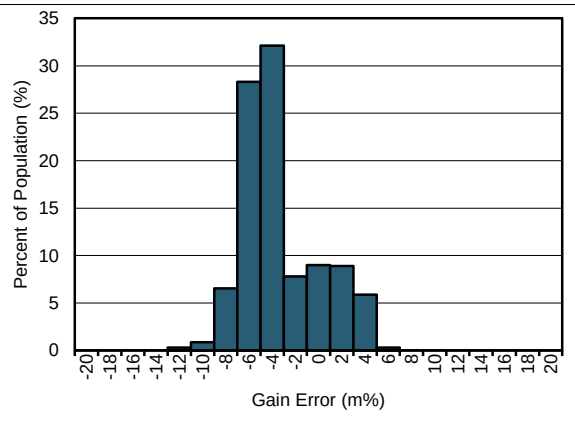


図 9. Typical Distribution of Gain Error (G = 1)

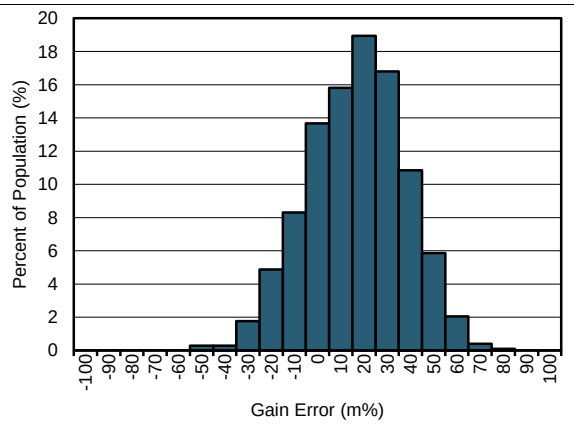


図 10. Gain Error (G = 10)

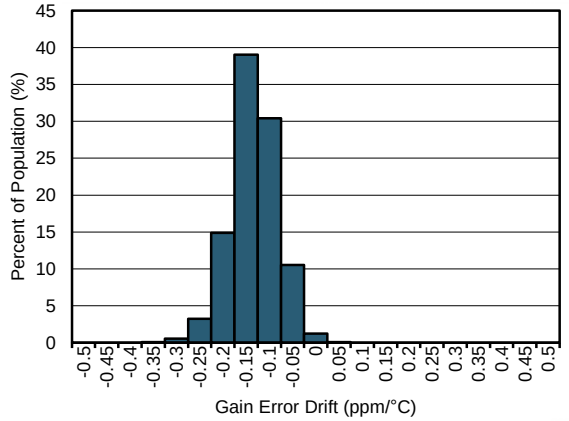


図 11. Typical Gain Error Drift Distribution (G = 1)

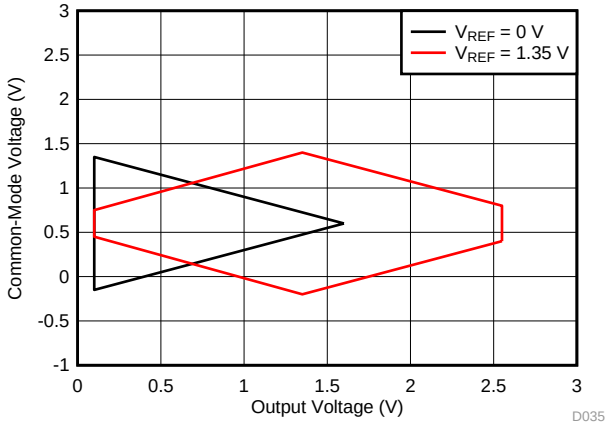
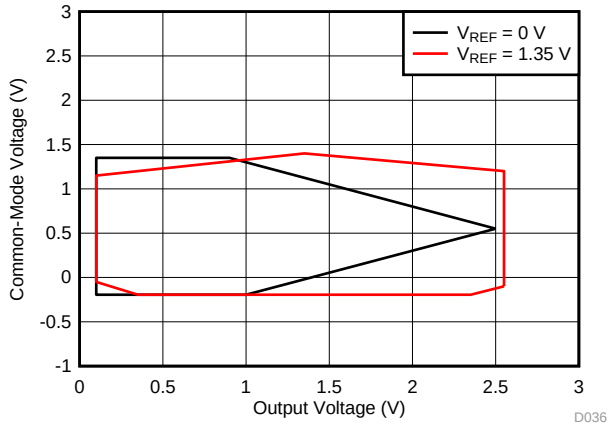


図 12. Input Common-Mode Voltage vs Output Voltage

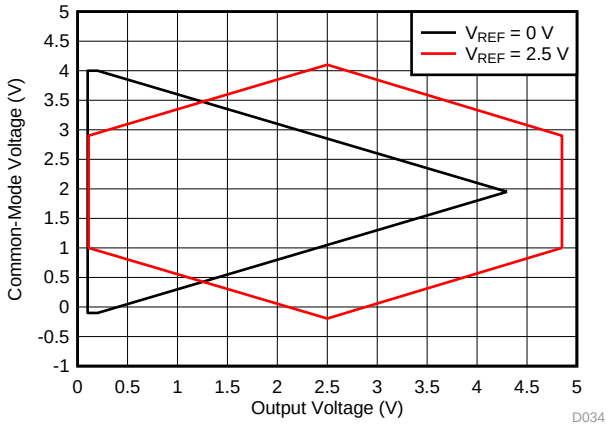
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



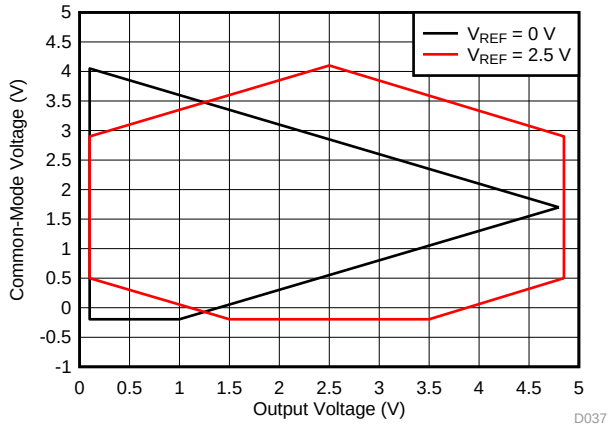
Single supply, V_S = 3 V, G = 100

図 13. Input Common-Mode Voltage vs Output Voltage



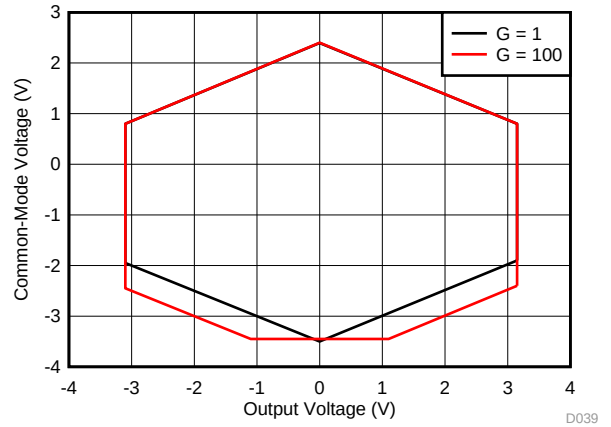
Single supply, V_S = 5 V, G = 1

図 14. Input Common-Mode Voltage vs Output Voltage



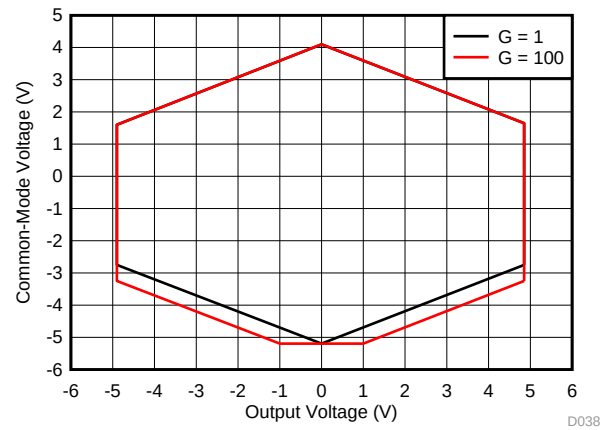
Single supply, V_S = 5 V, G = 100

図 15. Input Common-Mode Voltage vs Output Voltage



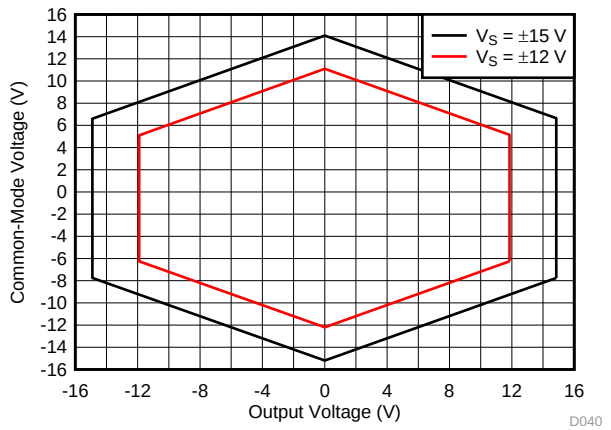
Dual supply, V_S = ±3.3 V, V_{REF} = 0 V

図 16. Input Common-Mode Voltage vs Output Voltage



Dual supply, V_S = ±5 V, V_{REF} = 0 V

図 17. Input Common-Mode Voltage vs Output Voltage

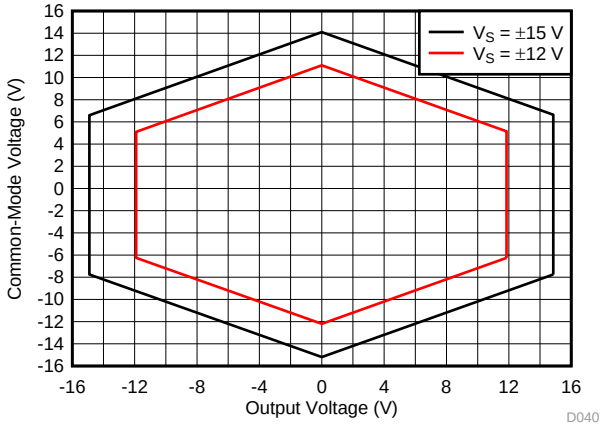


Dual supply, V_S = ±15 V and ±12 V, G = 1, V_{REF} = 0 V

図 18. Input Common-Mode Voltage vs Output Voltage

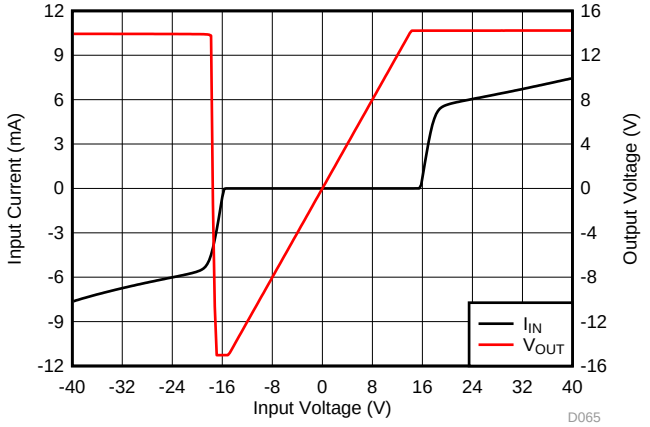
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



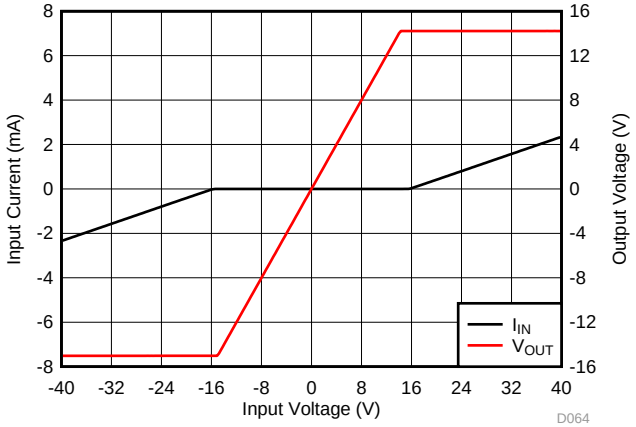
Dual supply, V_S = ±15 V and ±12 V, G = 100, V_{REF} = 0 V

図 19. Input Common-Mode Voltage vs Output Voltage



G = 1, V_S = ±15 V, R_S = 0 Ω

図 20. Input Current vs Input Voltage



G = 1, V_S = ±15 V, R_S = 10 kΩ

図 21. Input Current vs Input Voltage with 10-kΩ Resistance

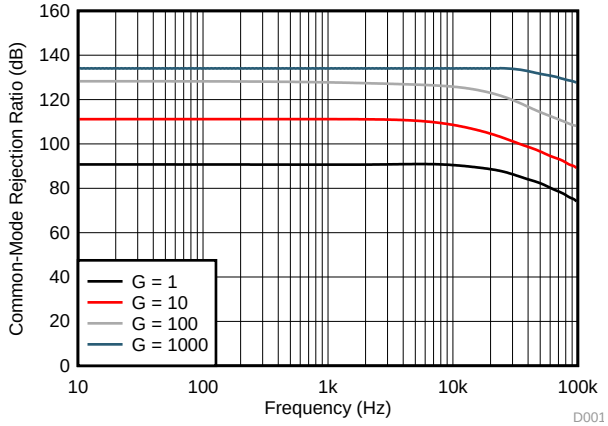


図 22. CMRR vs Frequency (RTI)

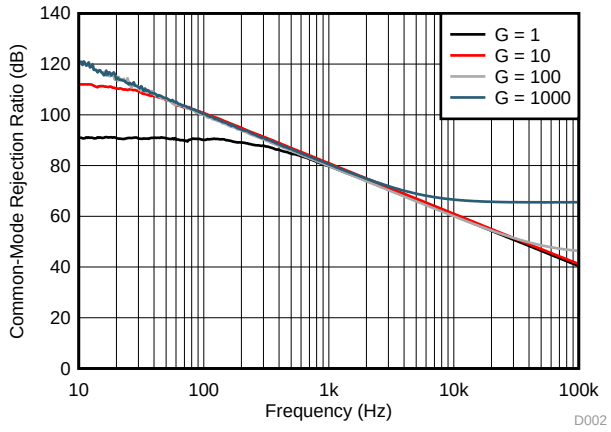


図 23. CMRR vs Frequency (RTI, 1-kΩ Source Imbalance)

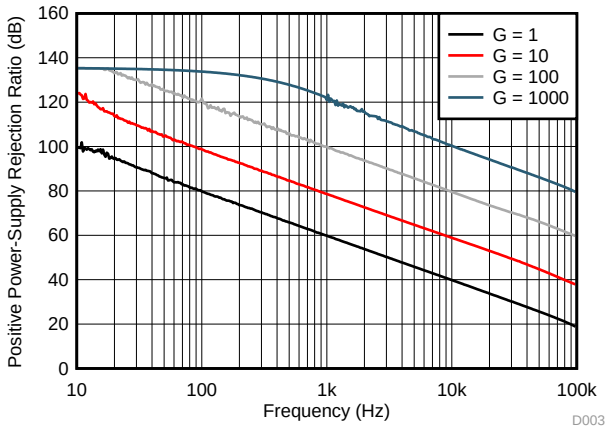


図 24. Positive PSRR vs Frequency (RTI)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

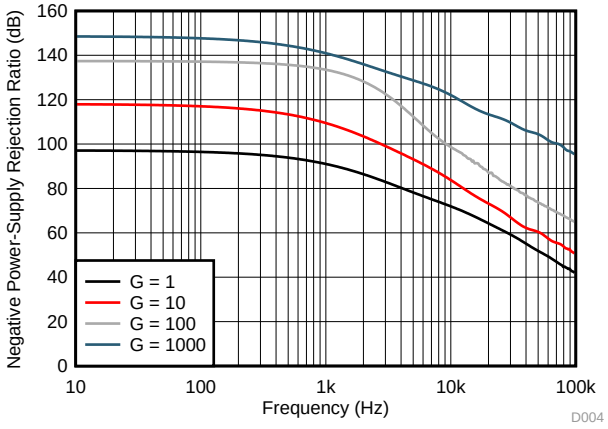


図 25. Negative PSRR vs Frequency (RTI)

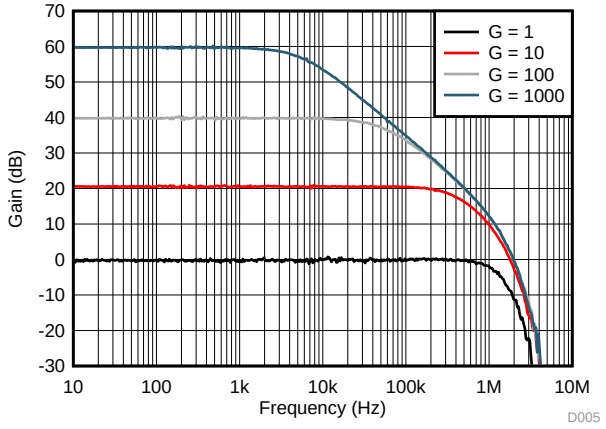


図 26. Gain vs Frequency

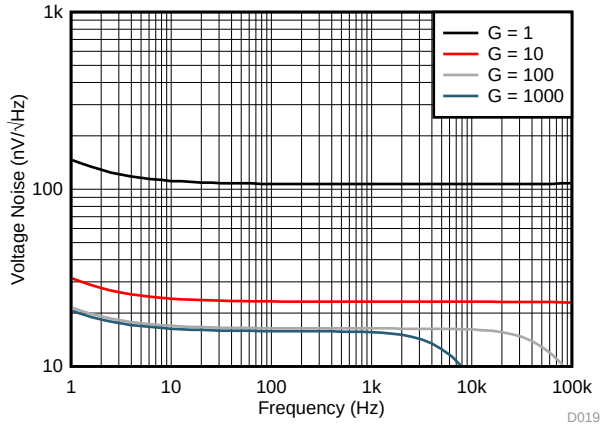


図 27. Voltage Noise Spectral Density vs Frequency (RTI)

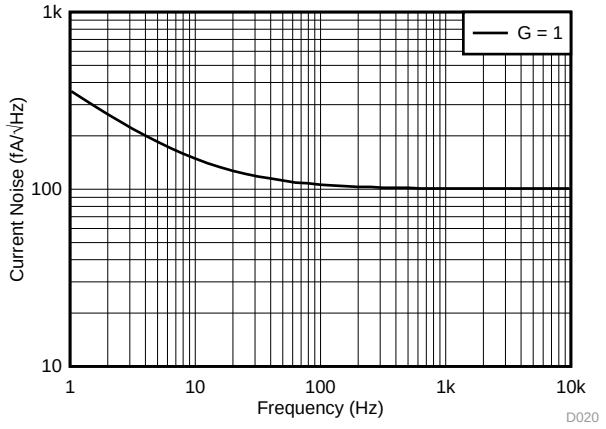


図 28. Current Noise Spectral Density vs Frequency (RTI)

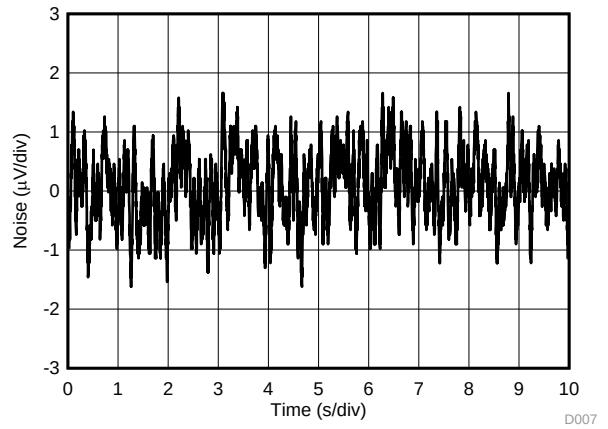


図 29. 0.1-Hz to 10-Hz RTI Voltage Noise (G = 1)

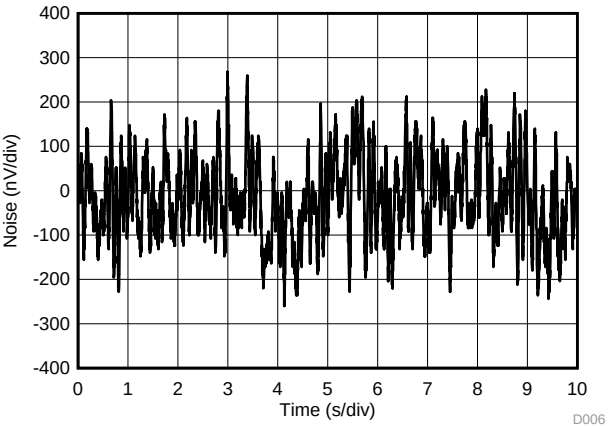


図 30. 0.1-Hz to 10-Hz RTI Voltage Noise (G = 1000)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

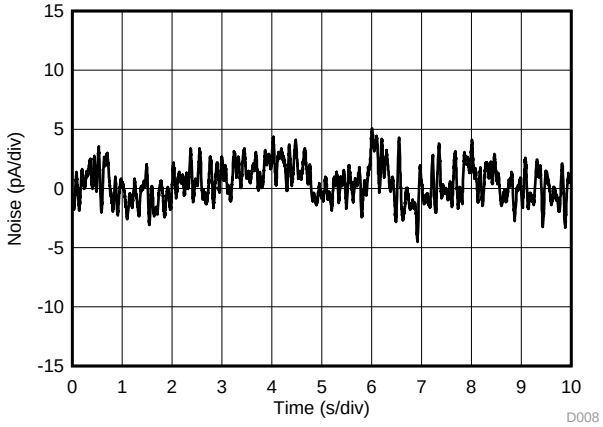
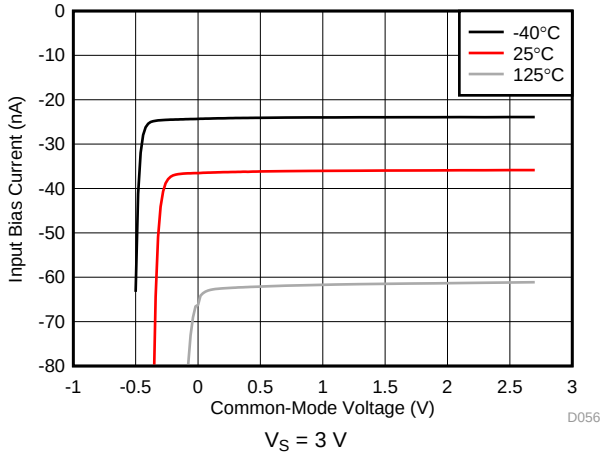
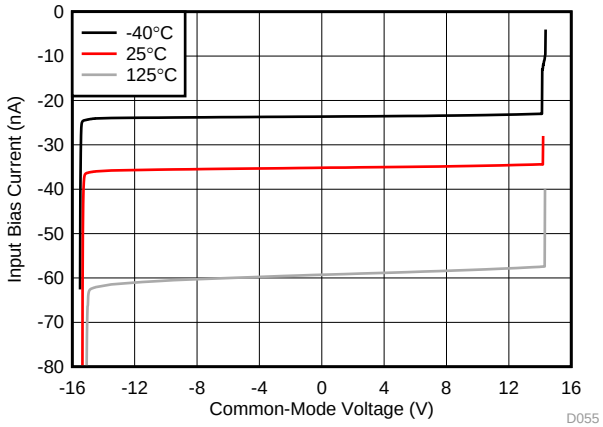


図 31. 0.1-Hz to 10-Hz RTI Current Noise



V_S = 3 V

図 32. Input Bias Current vs Common-Mode Voltage



V_S = ±15 V

図 33. Input Bias Current vs Common-Mode Voltage

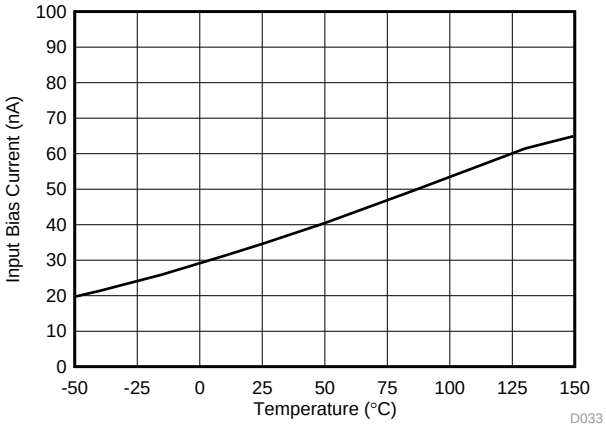


図 34. Input Bias Current vs Temperature

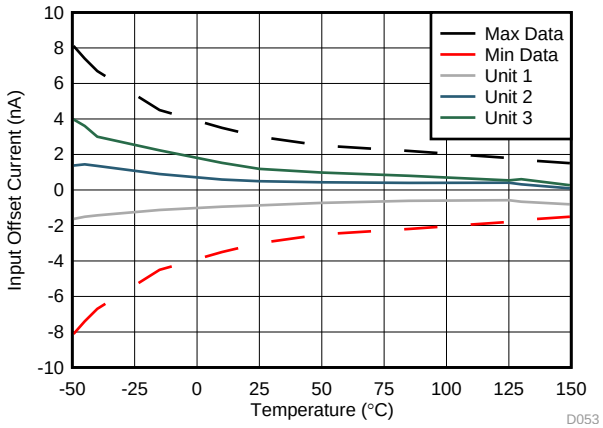


図 35. Input Offset Current vs Temperature

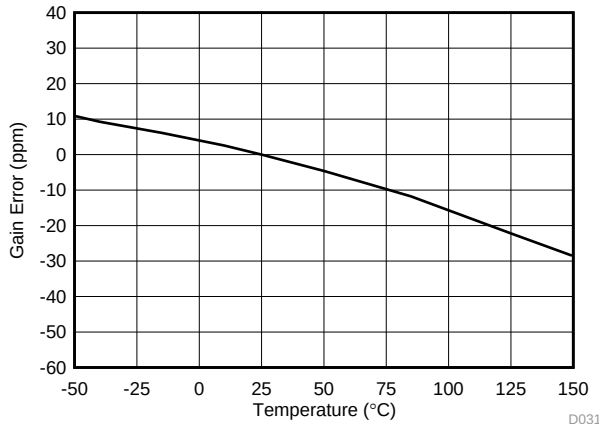


図 36. Gain Error vs Temperature (G = 1)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

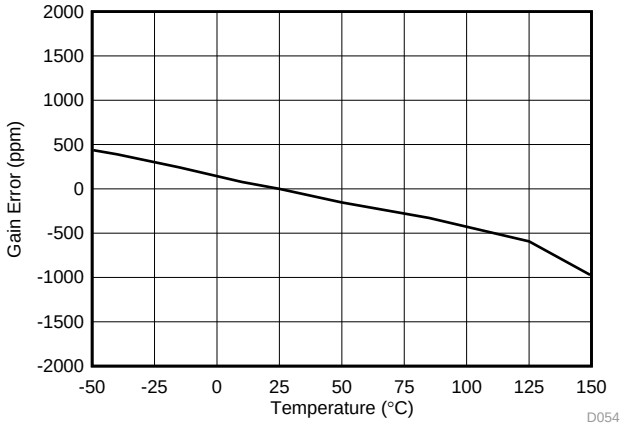


図 37. Gain Error vs Temperature (G > 1)

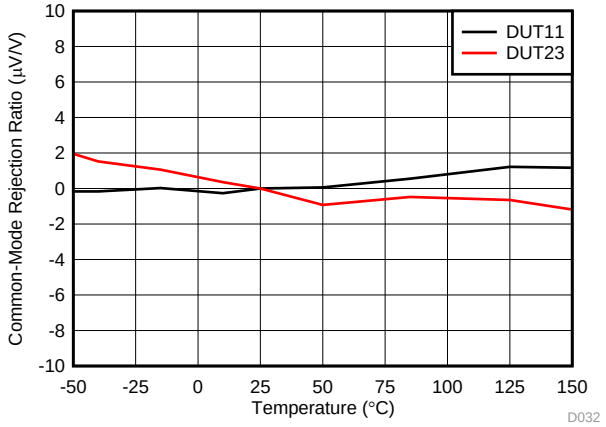


図 38. CMRR vs Temperature (G = 1)

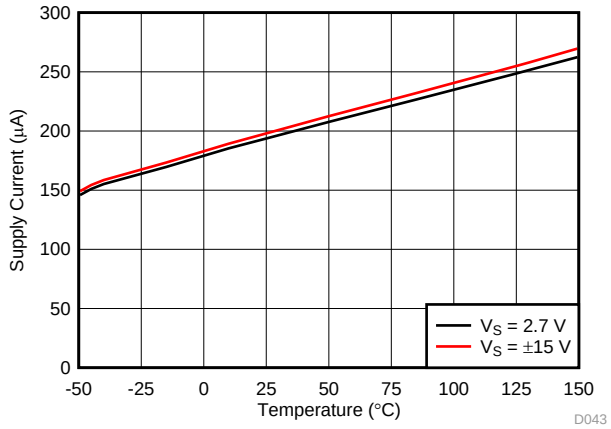


図 39. Supply Current vs Temperature

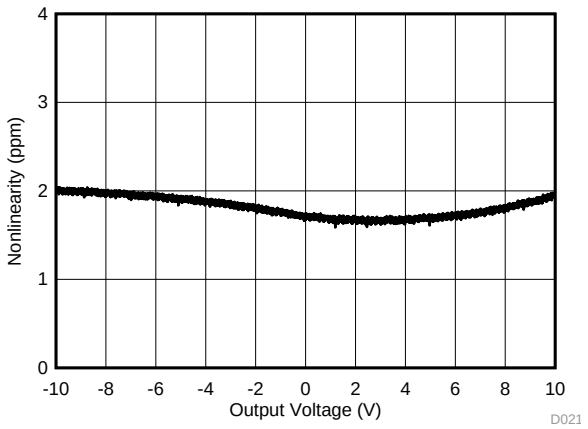


図 40. Gain Nonlinearity (G = 1)

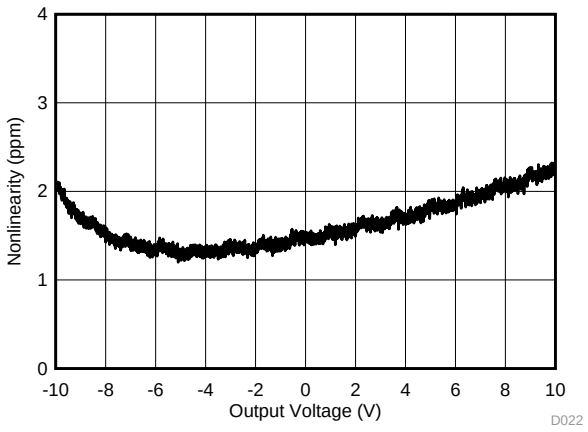


図 41. Gain Nonlinearity (G = 10)

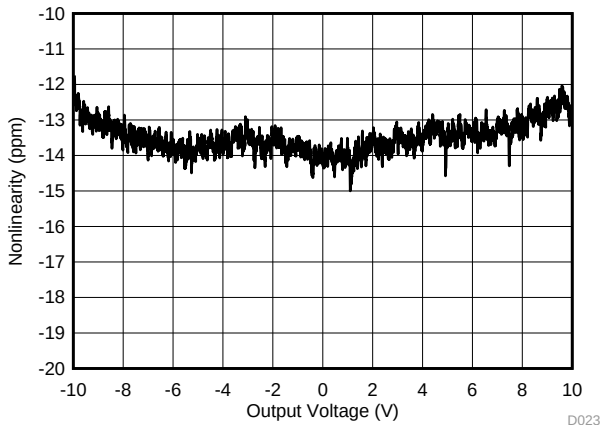


図 42. Gain Nonlinearity (G = 100)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

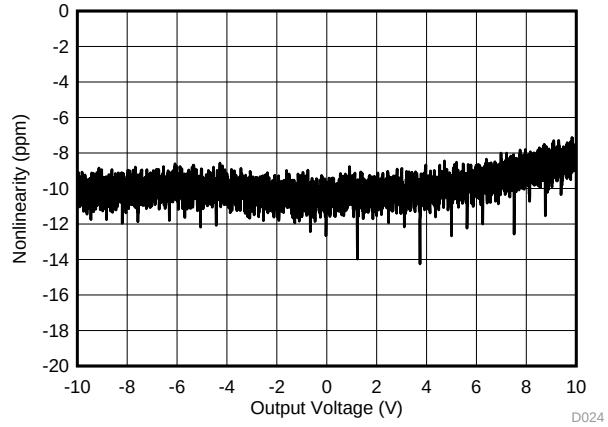
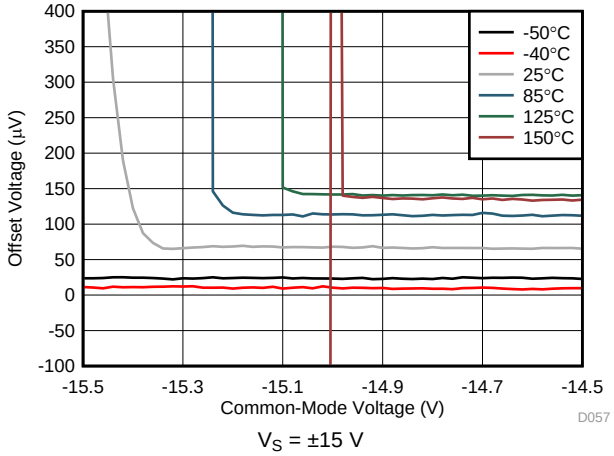
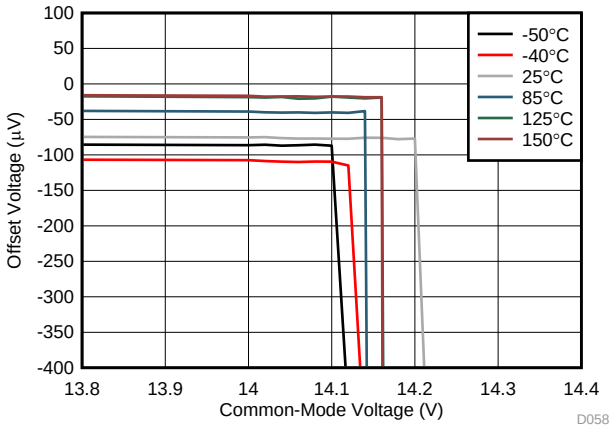


図 43. Gain Nonlinearity (G = 1000)



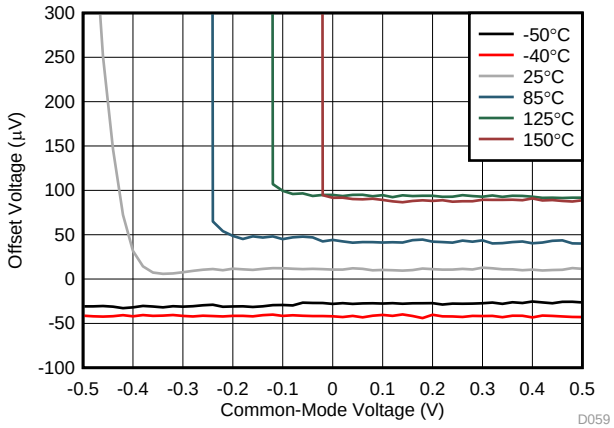
V_S = ±15 V

図 44. Offset Voltage vs Negative Common-Mode Voltage



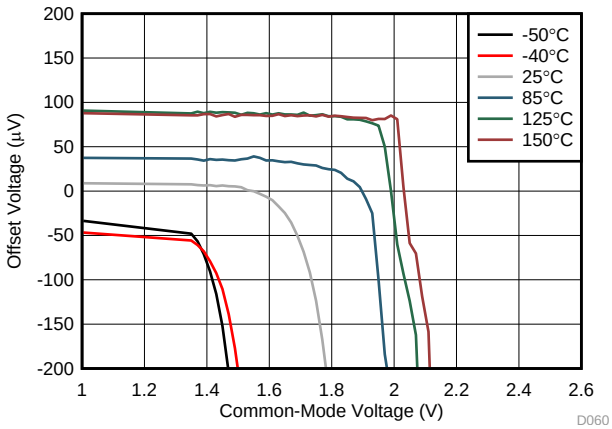
V_S = ±15 V

図 45. Offset Voltage vs Positive Common-Mode Voltage



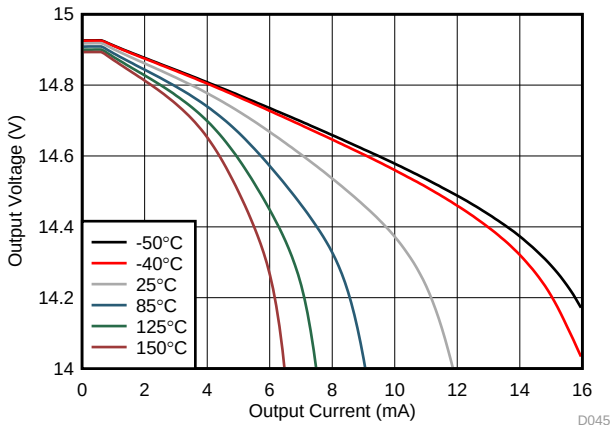
V_S = 3 V

図 46. Offset Voltage vs Negative Common-Mode Voltage



V_S = 3 V

図 47. Offset Voltage vs Positive Common-Mode Voltage

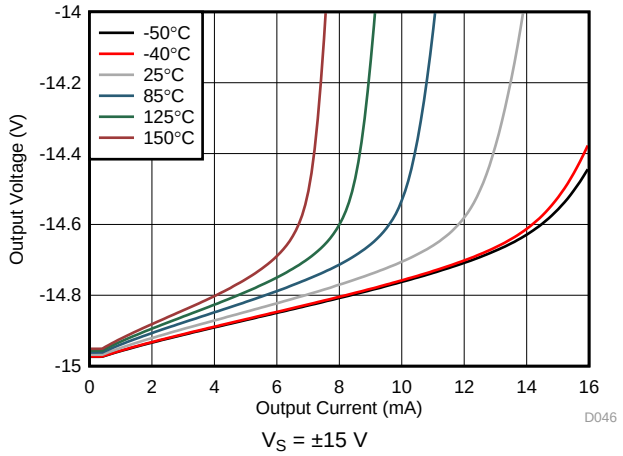


V_S = ±15 V

図 48. Positive Output Voltage Swing vs Output Current

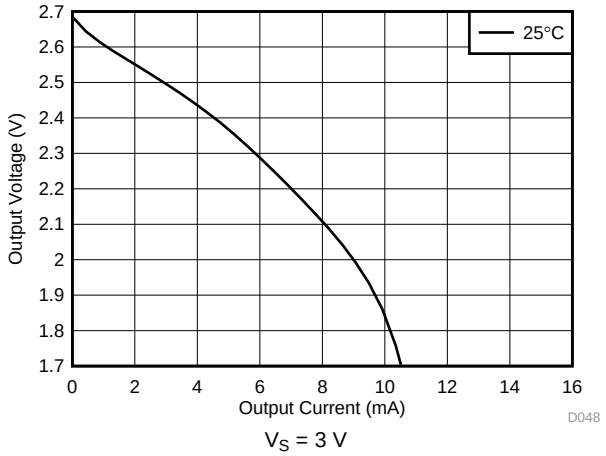
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



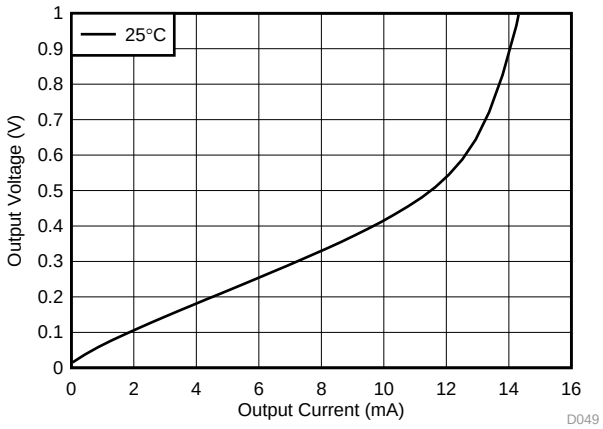
V_S = ±15 V

図 49. Negative Output Voltage Swing vs Output Current



V_S = 3 V

図 50. Positive Output Voltage Swing vs Output Current



V_S = 3 V

図 51. Negative Output Voltage Swing vs Output Current

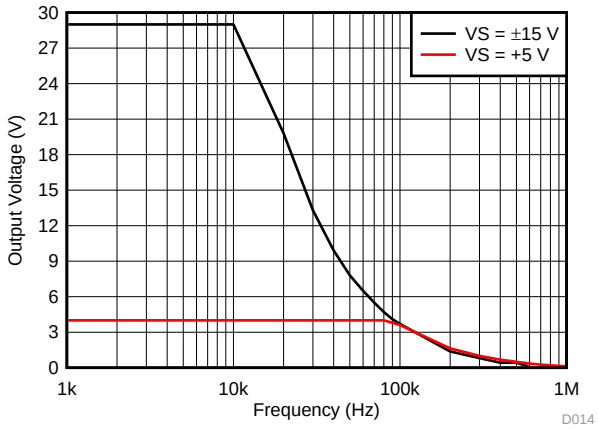


図 52. Large-Signal Frequency Response

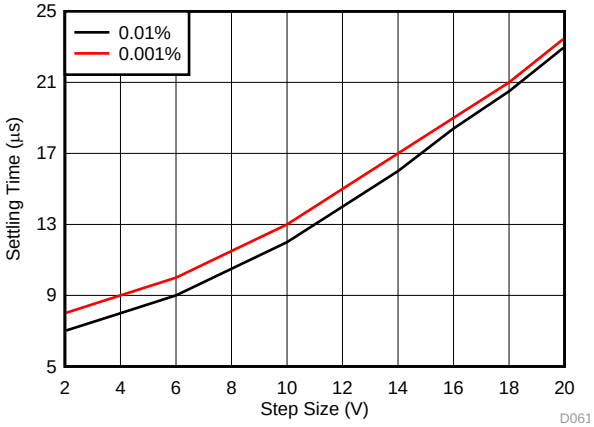


図 53. Settling Time vs Step Size (V_S = ±15 V)

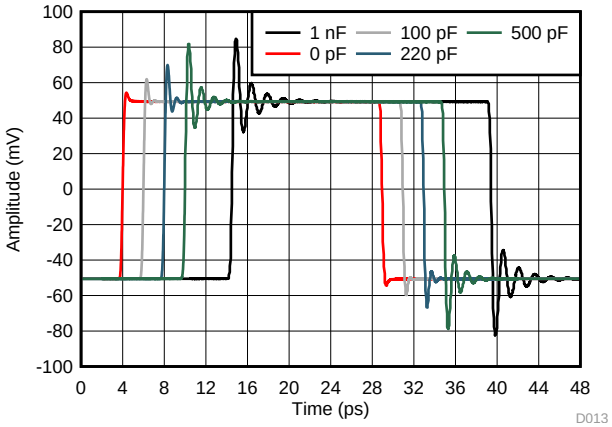
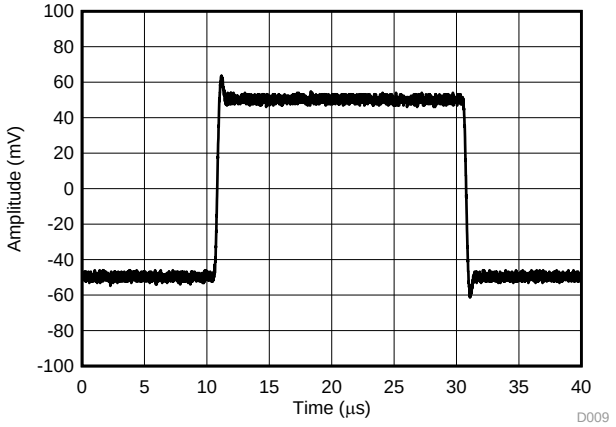


図 54. Small-Signal Response vs Capacitive Loads (G = 1)

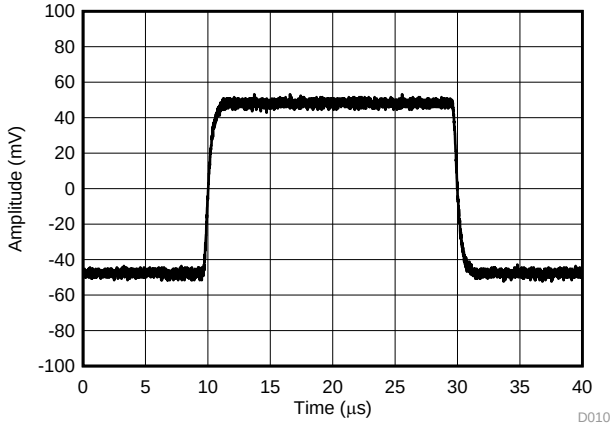
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



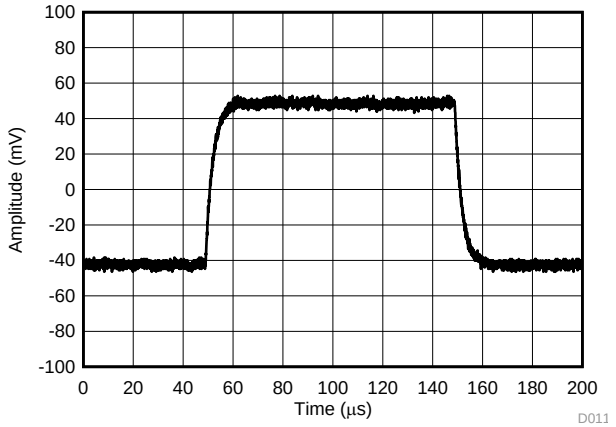
G = 1, R_L = 1 kΩ, C_L = 100 pF

図 55. Small-Signal Response



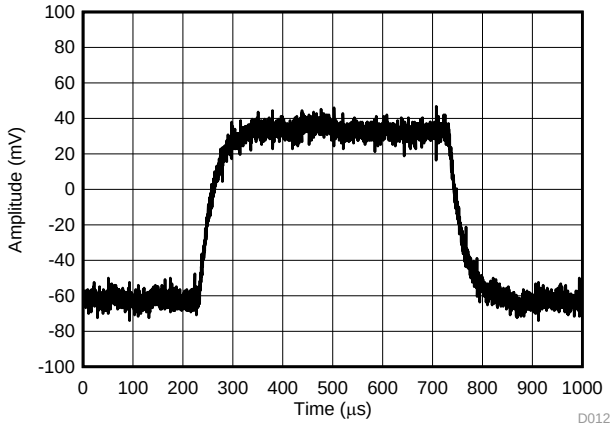
G = 10, R_L = 10 kΩ, C_L = 100 pF

図 56. Small-Signal Response



G = 100, R_L = 10 kΩ, C_L = 100 pF

図 57. Small-Signal Response



G = 1000, R_L = 10 kΩ, C_L = 100 pF

図 58. Small-Signal Response

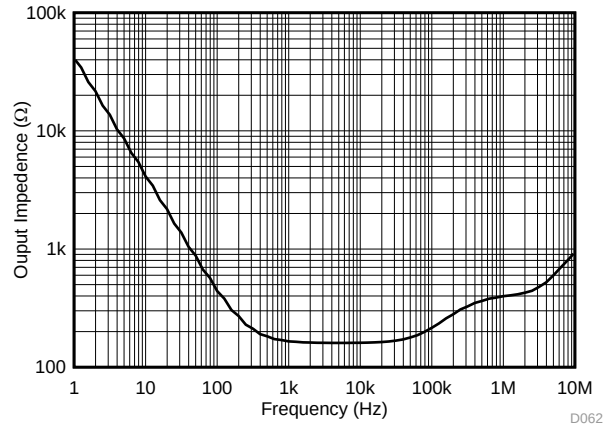


図 59. Open-Loop Output Impedance vs Frequency

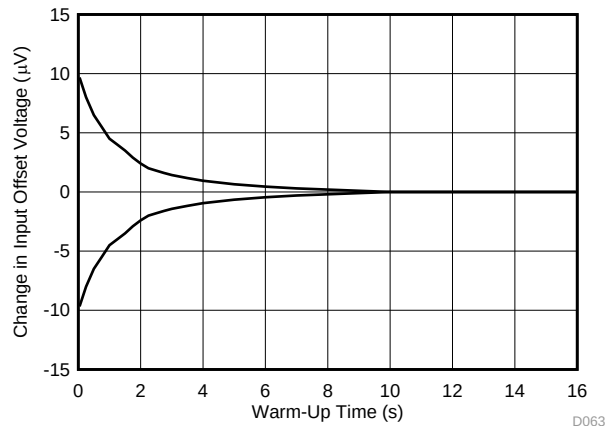
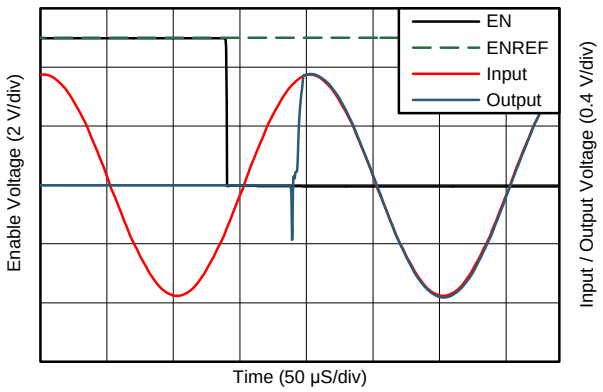


図 60. Change in Input Offset Voltage vs Warm-Up Time

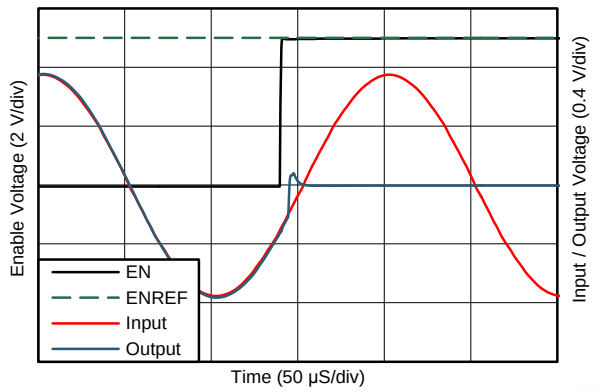
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



ENREF pin tied to 5 V

図 61. Enable Output Response



ENREF pin tied to 5 V

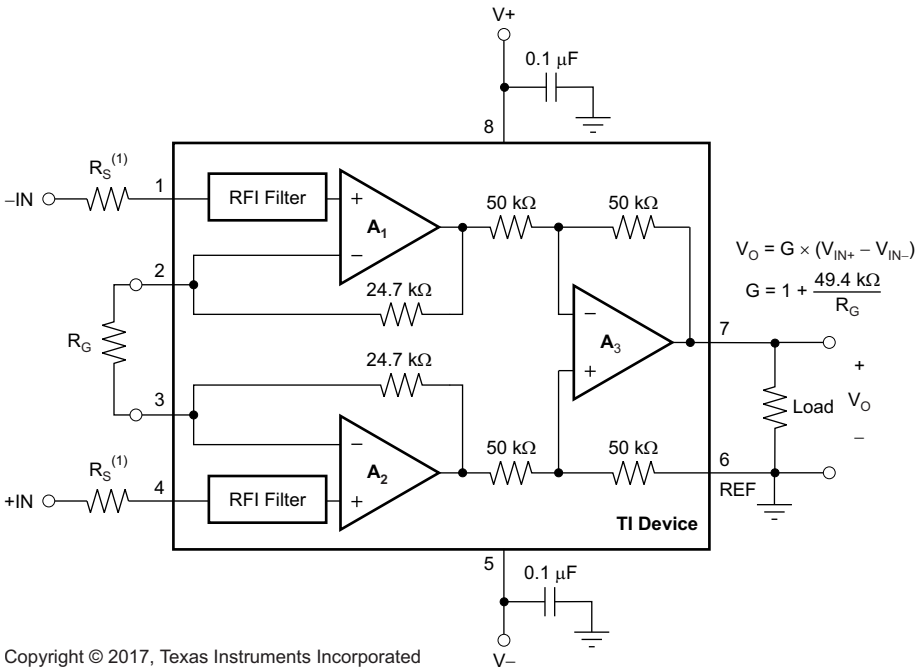
図 62. Disable Output Response

7 Detailed Description

7.1 Overview

A simplified schematic of the INA826S is shown in as well as the basic connections required for proper functionality. The INA826S consists of a 4-resistor difference amplifier, composed of amplifier A3 and 50-kΩ resistors, as well as buffer amplifiers A1 and A2. The gain of the circuit is set by a single external resistor placed across pins 2 and 3. Further information on the internal topology and setting the gain can be found in the *Feature Description* section. High-precision thin-film resistors integrated on-chip allow for excellent rejection of common-mode interference signals and high gain accuracy. The INA826S also integrates radio frequency interference (RFI) filters on the signal inputs to provide improved performance in the presence of high-frequency interference.

7.2 Functional Block Diagram



(1) This resistor is optional if the input voltage stays above [(V–) – 2 V] or the signal source current drive capability is limited to less than 3.5 mA. See the *Input Protection* section for more details.

図 63. Simplified Block Diagram

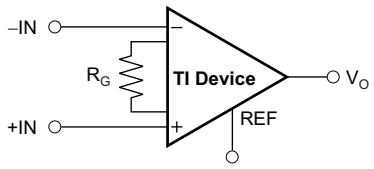


図 64. INA826S Basic Connections

7.3 Feature Description

7.3.1 Inside the INA826S

See the *Functional Block Diagram* section for a simplified representation of the INA826S. A more detailed diagram (shown in 図 65) provides additional details of the INA826S operation.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

The differential input voltage is buffered by Q_1 and Q_2 and is impressed across R_G, causing a signal current to flow through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF pin.

The equations shown in 図 65 describe the output voltages of A_1 and A_2. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V higher than the input voltages.

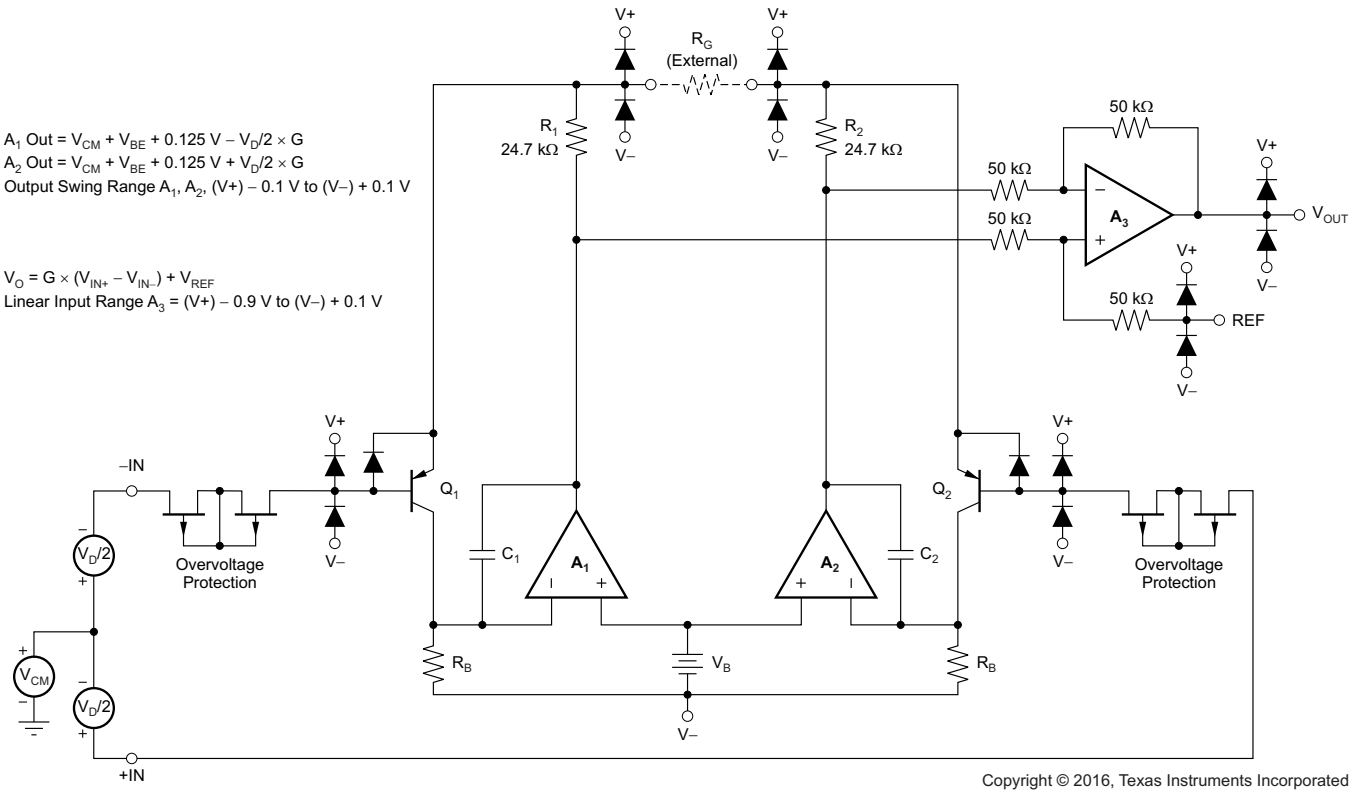


図 65. INA826S Simplified Circuit Diagram

Feature Description (continued)

7.3.2 Setting the Gain

Gain of the INA826S is set by a single external resistor, R_G, connected between pins 2 and 3. Use 式 1 to select the value of R_G:

$$G = 1 + \left(\frac{49.4\ k\Omega}{R_G} \right) \quad (1)$$

表 1 lists several commonly-used gains and resistor values. The 49.4-kΩ term in 式 1 comes from the sum of the two internal 24.7-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA826S.

表 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G (Ω)
1	—	—
2	49.4 k	49.9 k
5	12.35 k	12.4 k
10	5.489 k	5.49 k
20	2.600 k	2.61 k
50	1.008 k	1 k
100	499	499
200	248	249
500	99	100
1000	49.5	49.9

7.3.2.1 Gain Drift

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from the gain of 式 1.

The best gain drift of 1 ppm/℃ can be achieved when the INA826S uses G = 1 without R_G connected. In this case, the gain drift is limited only by the slight mismatch of the temperature coefficient of the integrated 50-kΩ resistors in the differential amplifier (A_3). At G greater than 1, the gain drift increases as a result of the individual drift of the 24.7-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of the external gain resistor R_G. Process improvements of the temperature coefficient of the feedback resistors now make possible specifying a maximum gain drift of the feedback resistors of 35 ppm/℃, thus significantly improving the overall temperature stability of applications using gains greater than 1.

Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency; see typical characteristic curves 図 22 and 図 23.

7.3.3 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF pin. 図 66 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF pin is summed at the output. The op amp buffer provides low impedance at the REF pin to preserve good common-mode rejection.

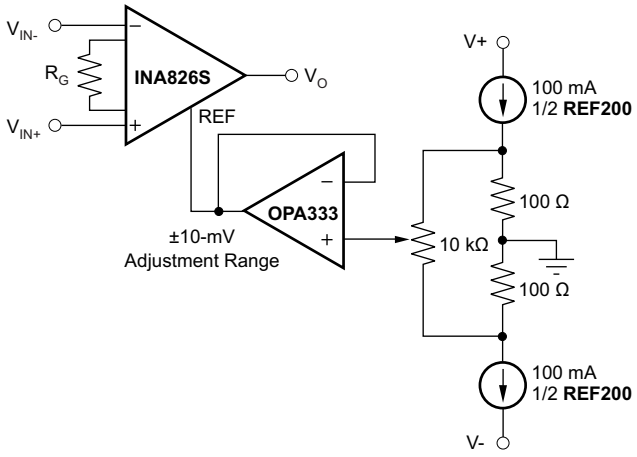


図 66. Optional Trimming of Output Offset Voltage

7.3.4 Input Common-Mode Range

The linear input voltage range of the INA826S input circuitry extends from the negative supply voltage to 1 V below the positive supply, and maintains 84-dB (minimum) common-mode rejection throughout this range. The common-mode range for most common operating conditions is described in 図 12 through 図 18 and 図 44 through 図 46. The INA826S can operate over a wide range of power supplies and V_{REF} configurations, making a comprehensive guide to common-mode range limits impractical to be provided for all possible conditions.

The most commonly overlooked overload condition occurs when a circuit exceeds the output swing of A_1 and A_2, which are internal circuit nodes that cannot be measured. Calculating the expected voltages at the output of A_1 and A_2 (see 図 65) provides a check for the most common overload conditions. The designs of A_1 and A_2 are identical and the outputs can swing to within approximately 100 mV of the power-supply rails. For example, when the A_2 output is saturated, A_1 may continue to be in linear operation, responding to changes in the noninverting input voltage. This difference can give the appearance of linear operation but the output voltage is invalid.

A single-supply instrumentation amplifier has special design considerations. To achieve a common-mode range that extends to single-supply ground, the INA826S employs a current-feedback topology with PNP input transistors; see 図 65. The matched PNP transistors Q_1 and Q_2 shift the input voltages of both inputs up by a diode drop, and through the feedback network, shift the output of A_1 and A_2 by approximately 0.8 V. With both inputs and V_{REF} at single-supply ground (negative power supply), the output of A_1 and A_2 is well within the linear range, allowing differential measurements to be made at the GND level. As a result of this input level-shifting, the voltages at pin 2 and pin 3 are not equal to the respective input pin voltages (pin 1 and pin 4). For most applications, this inequality is not important because only the gain-setting resistor connects to these pins.

7.3.5 Input Protection

The inputs of the INA826S are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and 40 V on the other input does not cause damage. However, if the input voltage exceeds (V–) – 2 V and the signal source current drive capability exceeds 3.5 mA, the output voltage switches to the opposite polarity; see 図 20. This polarity reversal can easily be avoided by adding resistance of 10 kΩ in series with both inputs.

Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 8 mA. 図 20 and 図 21 illustrate this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

7.3.6 Input Bias Current Return Path

The input impedance of the INA826S is extremely high—approximately 20 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 35 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 図 67 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA826S, and the input amplifiers saturate. If the differential source resistance is low, as shown in the thermocouple example in 図 67, the bias current return path can be connected to one input. With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

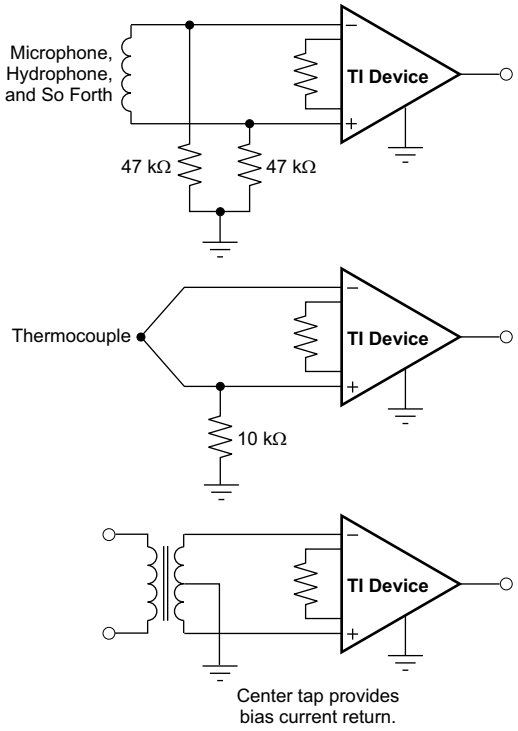


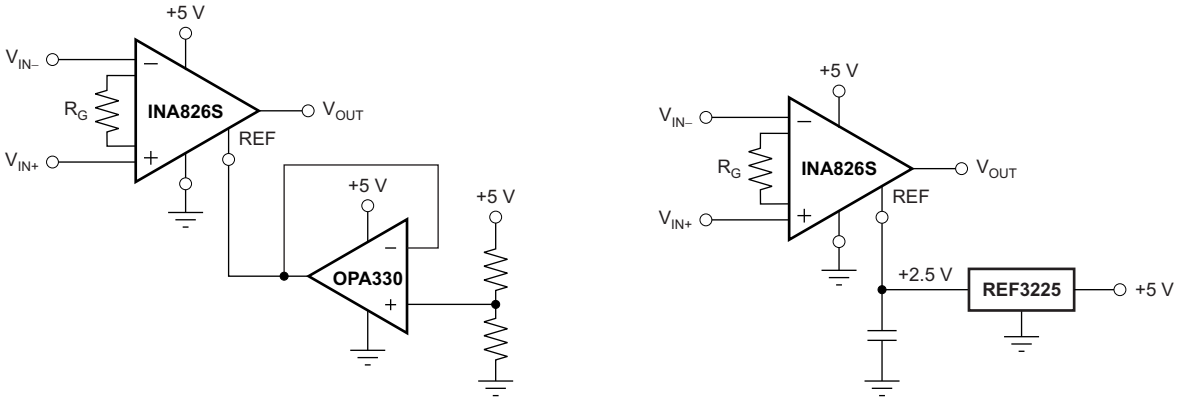
図 67. Providing an Input Common-Mode Current Path

7.3.7 Reference Pin (REF)

The output voltage of the INA826S is developed with respect to the voltage on the reference terminal. Often, in dual-supply operation, the reference pin (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise mid-supply level can be useful (for example, 2.5 V in a 5-V supply environment). To accomplish this offset, a voltage source can be tied to the REF pin to level-shift the output so that the INA826S can drive a single-supply ADC, for example.

For the best performance, keep the source impedance to the REF pin below 5 Ω. As shown in , the reference resistor is at one end of a 50-kΩ resistor. Additional impedance at the REF pin adds to this 50-kΩ resistor. The imbalance in the resistor ratios results in degraded common-mode rejection ratio (CMRR).

図 68 shows two different methods of driving the reference pin with low impedance. The OPA330 is a low-power, chopper-stabilized amplifier, and therefore offers excellent stability over temperature. The OPA330 is available in the space-saving SC70 and even smaller chip-scale package. The REF3225 is a precision reference in the small SOT23-6 package.



a) Level shifting using the OPA330 as a low-impedance buffer

b) Level shifting using the low-impedance output of the REF3225

図 68. Options for Low-Impedance Level Shifting

7.3.8 Shutdown (EN and ENREF) Pins

The INA826S provides two pins to shut the device down: EN (enable) and ENREF (enable reference). 図 69 shows a basic schematic of the shutdown logic circuitry of the INA826S. A PNP transistor forms the basis of the internal shutdown circuitry. The ENREF pin is connected to the emitter of the PNP transistor and is meant to be connected to a voltage reference point for the enable logic. The EN pin is connected the base of the PNP transistor. Applying a voltage to the EN pin that is 0.8 V or more below the enable reference voltage (at the ENREF pin) causes a small current to flow in the internal PNP transistor that powers the INA826S internal bias circuitry and powers-up the instrumentation amplifier. The shutdown circuitry functions properly with ENREF connected to a voltage between (V–) + 1.5 V up to V+. The voltage on the EN pin can be as low as the negative supply voltage (VS–) but cannot go above the voltage applied to the ENREF pin.

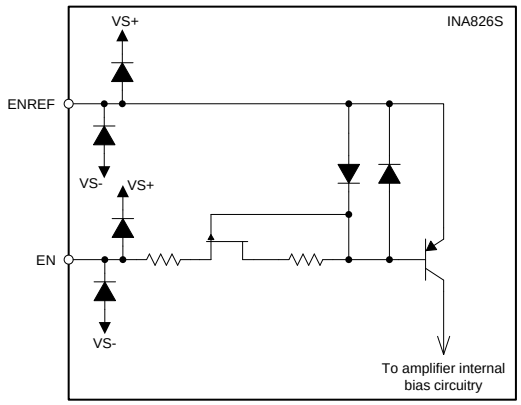


図 69. Shutdown Pin Simplified Schematic

To better understand the functionality of these pins, consider the low-voltage, single-supply application shown in 図 70 with V+ = 3.3 V. ENREF is connected to the 3.3-V power supply of the microcontroller (labeled µC) and the EN pin is toggled by a general-purpose input/output (GPIO) pin of the microcontroller. When the GPIO pin is asserted low, such that the voltage at the GPIO pin output is at or near 0 V, the INA826S is enabled. Conversely, if the GPIO pin is asserted high, with an output voltage at or near 3.3 V, the INA826S is disabled.

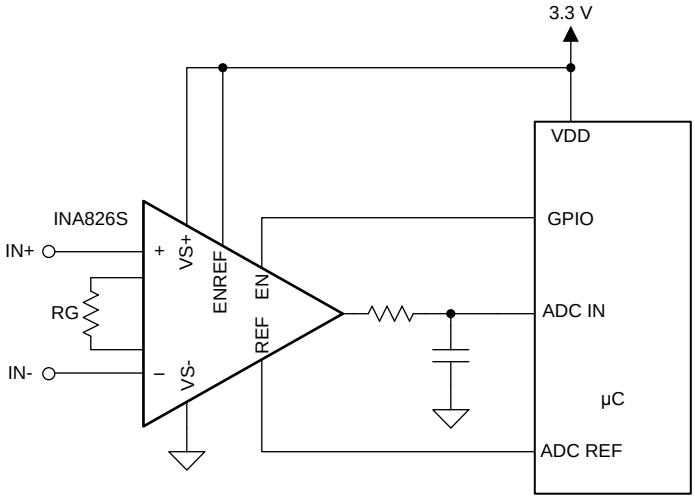


図 70. Example Configuration in a Single-Supply System (Pulling EN low enables the INA826S.)

図 71 shows an alternate configuration of the enable logic pins. By grounding the enable pin, and toggling the ENREF pin with the GPIO of the microcontroller, the enable logic is reversed. Now asserting high at the GPIO output enables the INA826S, and pulling the GPIO pin low disables the INA826S.

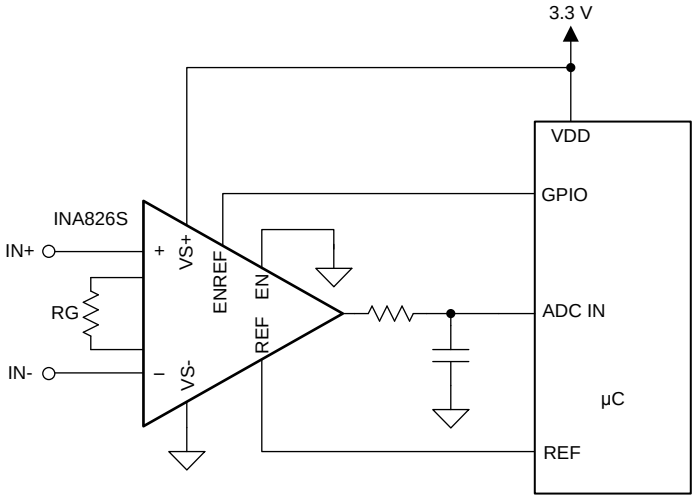


図 71. Alternate Configuration for the Enable Logic Pins (Pulling ENREF high enables the INA826S.)

The majority of INA826S applications benefit greatly from the reduction of quiescent current from the typical 200 µA to values at or below 6 µA. Achieving the lowest possible system-level current in a system requires attention to other system voltages applied to the INA826S. When shutdown, voltages applied to the reference or input pins of the INA826S can find paths for currents to flow up into the several microamps region. In many systems these voltages are shut down when the INA826S is shutdown, simplifying the problem. Otherwise, additional switching may be added to reduce currents to a minimum.

7.4 Device Functional Modes

The INA826S features a shutdown mode that reduces the typical power-supply current consumption from 200 µA to less than 6 µA. Disabling the INA826S turns off the bias circuitry that powers the internal amplifiers of the INA826S. 図 72 and 図 73 show the output behavior of the INA826S when the shutdown state is toggled. For these plots, the ENREF pin was connected to a 5-V potential and the EN pin was pulled low to enable the INA826S. 図 72 shows how quickly the INA826S output responds when transitioning from a shutdown state to an enabled state. When the EN pin is pulled low, the INA826S output begins to track the input signal approximately 60 µs later. When transitioning from enabled to shutdown, as shown in 図 73, the output of the INA826S stops tracking the input waveform in approximately 10 µs.

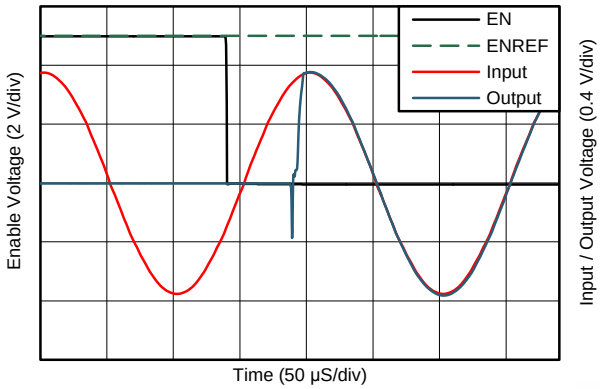


図 72. Enable Output Response

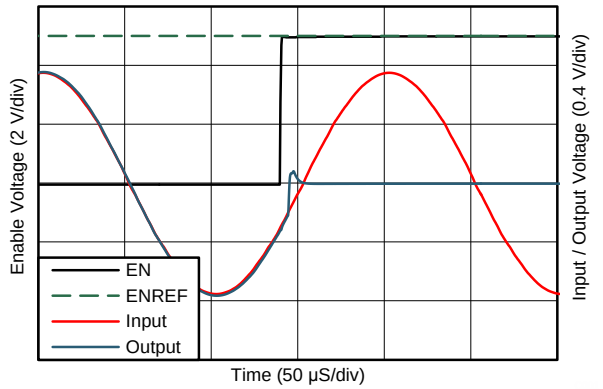


図 73. Disable Output Response

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The low power consumption and high performance of the INA826S make the device an excellent instrumentation amplifier for many applications. The INA826S can be used in many low-power, portable applications because the device has a low quiescent current (200 µA, typical) and comes in a small 10-pin VSON package. The input protection circuitry, low maximum gain drift, low offset voltage, and 36-V maximum supply voltage also make the INA826S an ideal choice for industrial applications as well.

8.2 Typical Application

図 74 shows a three-terminal, programmable-logic controller (PLC) design for the INA826S. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ± 2.3 V (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.

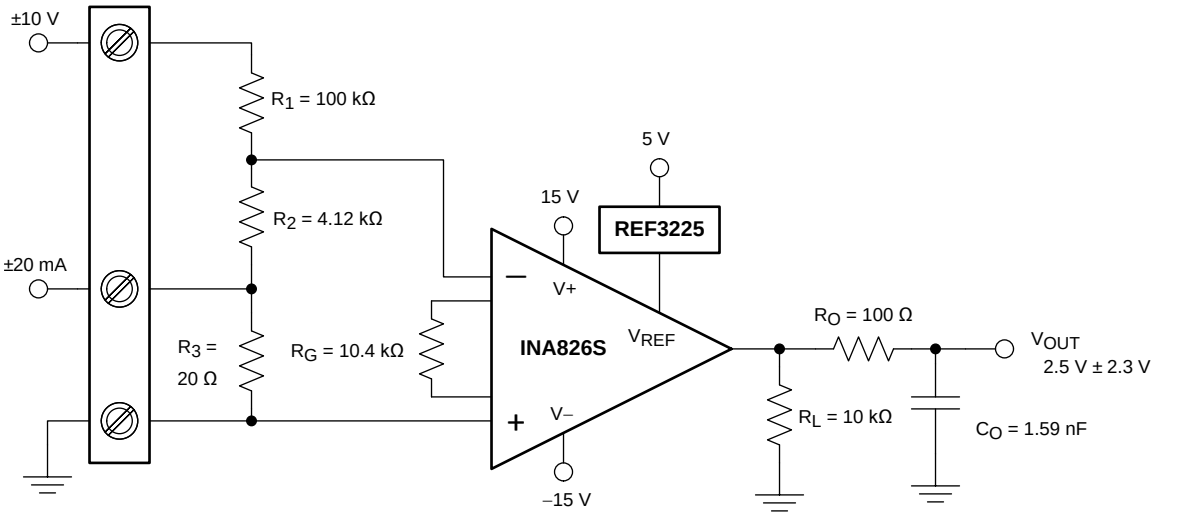


図 74. Three-Terminal Analog Input for PLCs

8.2.1 Design Requirements

This design has the following requirements:

- Supply voltage: ±15 V, 5 V
- Inputs: ±10 V, ±20 mA
- Output: 2.5 V, ±2.3 V

8.2.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in 図 74: current input and voltage input. This design requires R_1 >> R_2 >> R_3. Given this relationship, 式 2 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF}$$

where

- G represents the gain of the instrumentation amplifier (2)

式 3 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF} \quad (3)$$

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. 100 kΩ is selected for R_1 because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2. 20 Ω for R_3 is selected because that resistance value is much smaller than R_1 and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

式 4 can be used to calculate R_2 given V_D = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ k\Omega \quad (4)$$

Typical Application (continued)

The value obtained from 式 4 is not a standard 0.1% value, so 4.12 kΩ is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

Use 式 5 to calculate the ideal gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ V - 2.5\ V}{400\ mV} = 5.75\ \frac{V}{V} \quad (5)$$

式 6 calculates the gain-setting resistor value using the INA826S gain equation, 式 1.

$$G_{INA826} = 1 + \frac{49.4\ k\Omega}{R_G} \rightarrow R_G = \frac{49.4\ k\Omega}{G_{INA826} - 1} = \frac{49.4\ k\Omega}{5.75 - 1} = 10.4\ k\Omega \quad (6)$$

10.4 kΩ is a standard 0.1% resistor value that can be used in this design. Finally, the output RC filter components are selected to have a –3-dB cutoff frequency of 1 MHz.

8.2.3 Application Curves

図 75 and 図 76 show typical characteristic curves for 図 74.

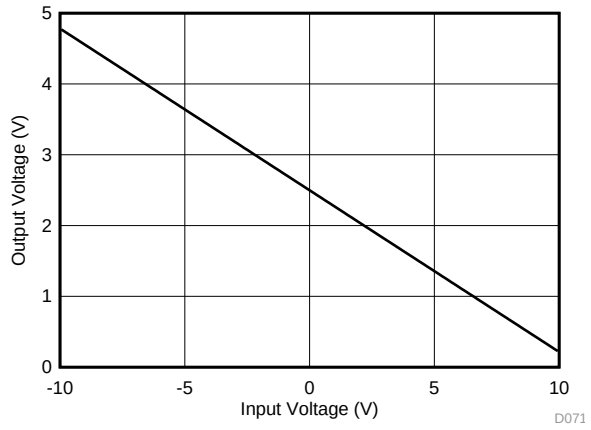


図 75. PLC Output Voltage vs Input Voltage

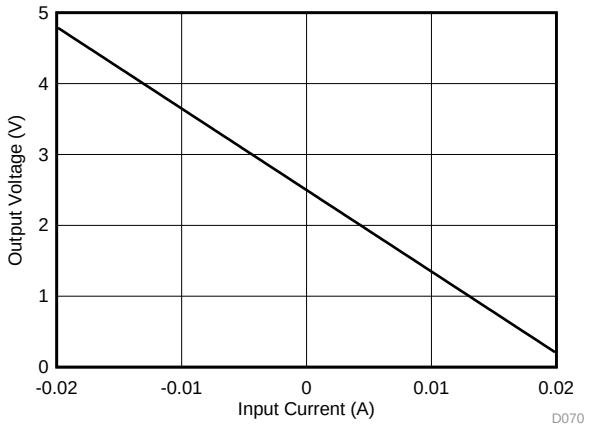


図 76. PLC Output Voltage vs Input Current

9 Power Supply Recommendations

The INA826S operates over a power-supply range of 3 V to 36 V (±3 V to ±18 V). Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are illustrated in the *Typical Characteristics* section.

9.1 Low-Voltage Operation

The INA826S can operate on power supplies as low as 3 V. Most parameters vary only slightly throughout this supply voltage range; see the *Typical Characteristics* section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The typical characteristic curves 図 12 through 図 18 and 図 44 through 図 46 describe the range of linear operation for various supply voltages, reference connections, and gains.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications. The bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry, because noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp specifically.
- Connect the device reference pin to a low-impedance, low-noise, system reference point, such as an analog ground. If a potential other than ground is used as a reference, a low output impedance (such as a voltage divider with an op amp buffer) must be included.
- Minimize the parasitic capacitance and inductance present at the gain resistor connections. Place the gain resistor as close to the device as possible, and remove the ground plane around the gain resistor to minimize parasitic capacitances at these nodes.
- For best performance, route the input traces adjacent to each other as a differential pair.
- For proper amplifier function, connect the package thermal pad to the most negative supply voltage (VEE).

10.2 Layout Example

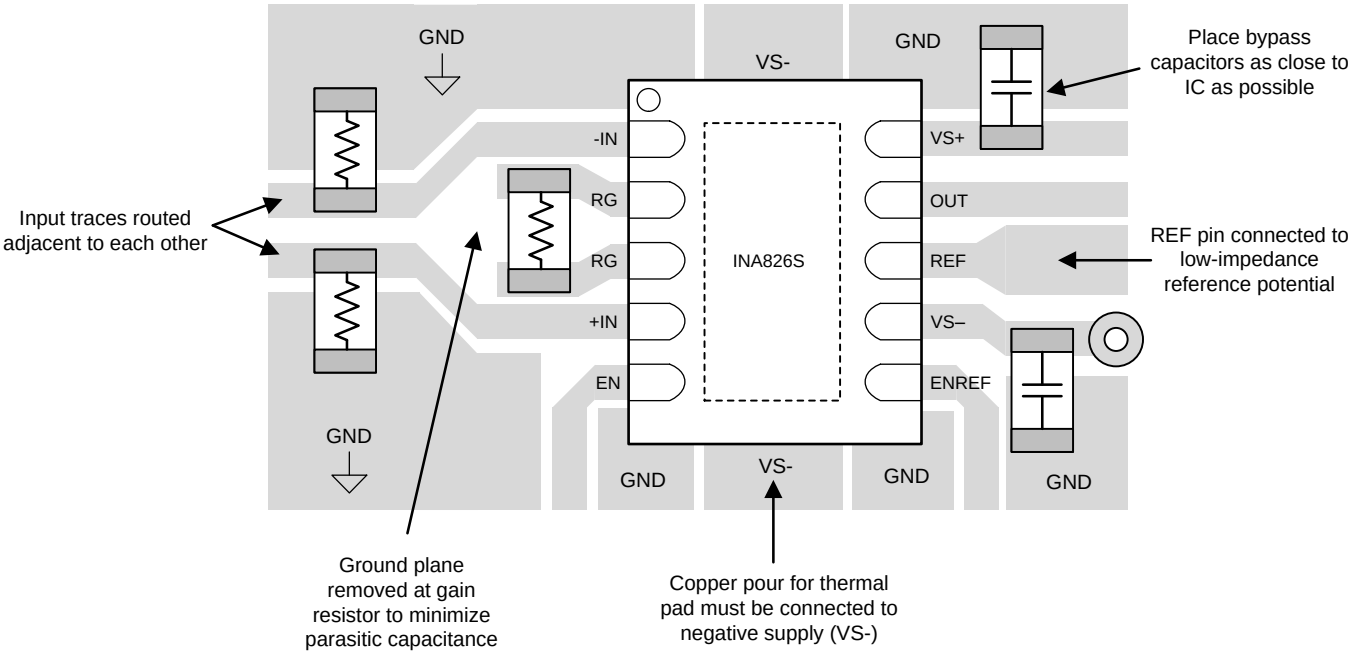


図 77. INA826S PCB Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください：

- *『OPAx330 50μV VOS、0.25μV/℃、35μA CMOSオペアンプ、ゼロ・ドリフト・シリーズ』*
- *『REF32xx 4ppm/℃、100μA、SOT23-6シリーズ基準電圧』*
- *『REF50xx 低ノイズ、超低ドリフト係数、高精度基準電圧』*
- *『SPICEベースのアナログ・シミュレーション・プログラム』*

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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11.5 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA826SIDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IN826S	Samples
INA826SIDRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IN826S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

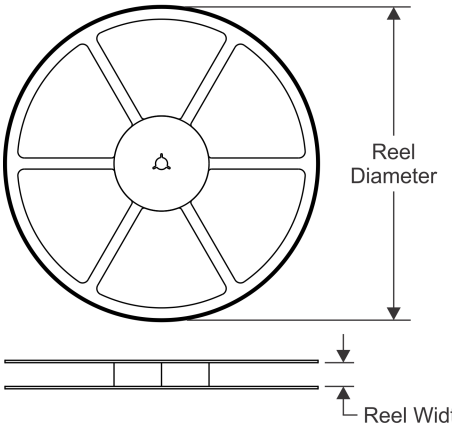
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

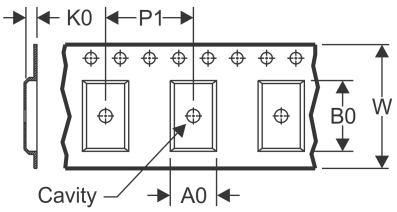
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

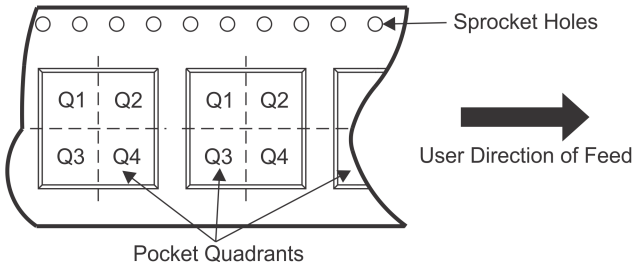


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

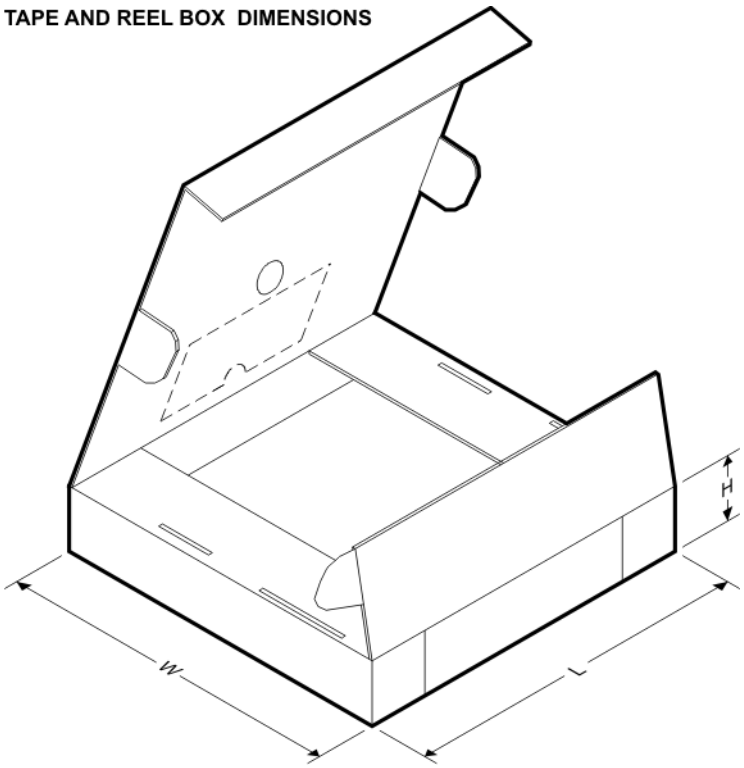
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA826SIDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA826SIDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA826SIDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
INA826SIDRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

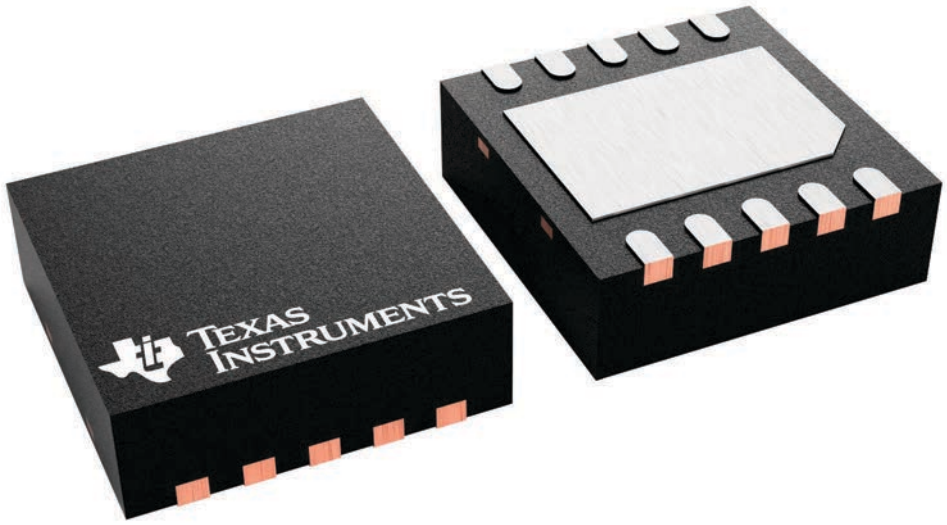
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



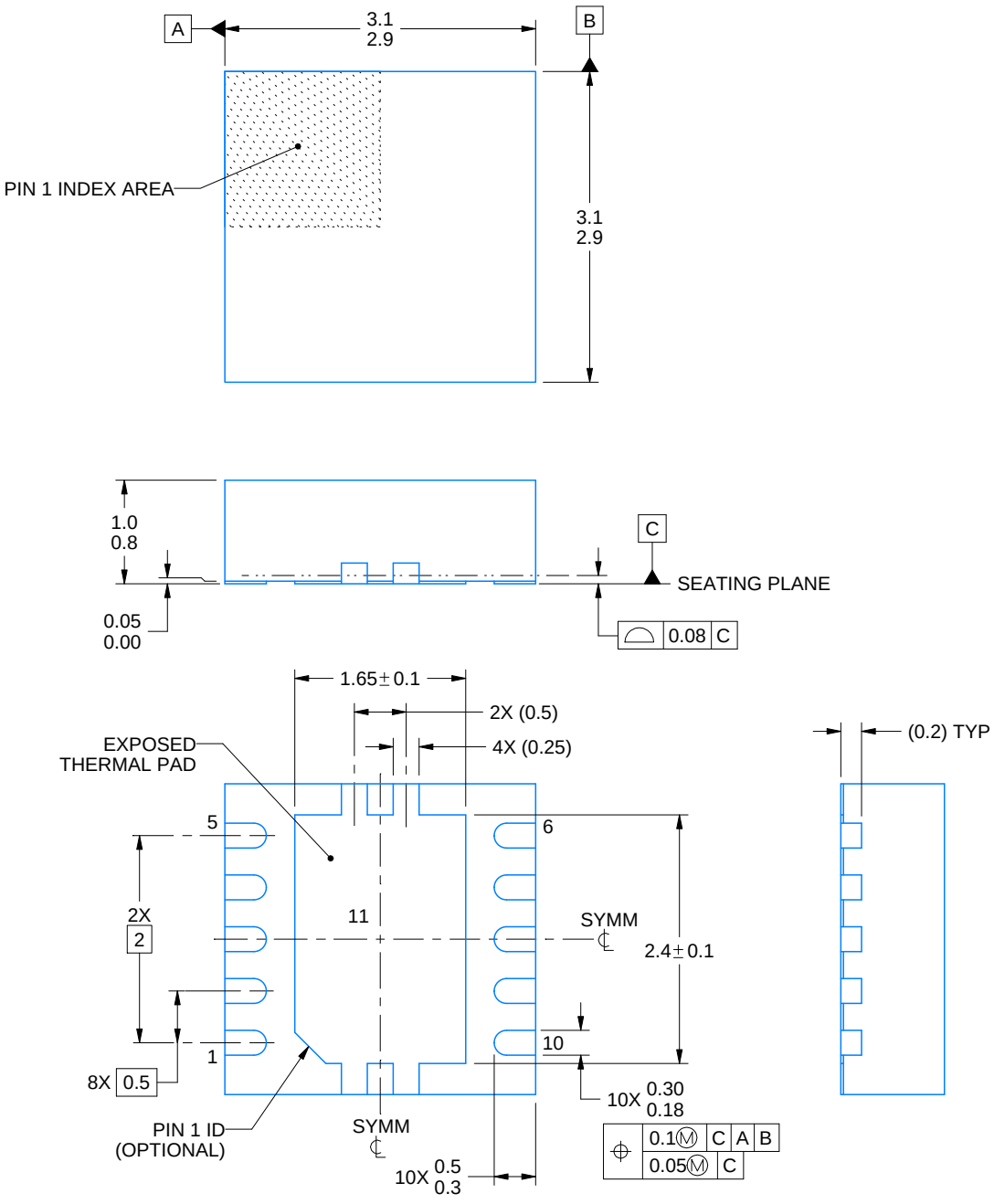
4226193/A

DRC0010J

PACKAGE OUTLINE

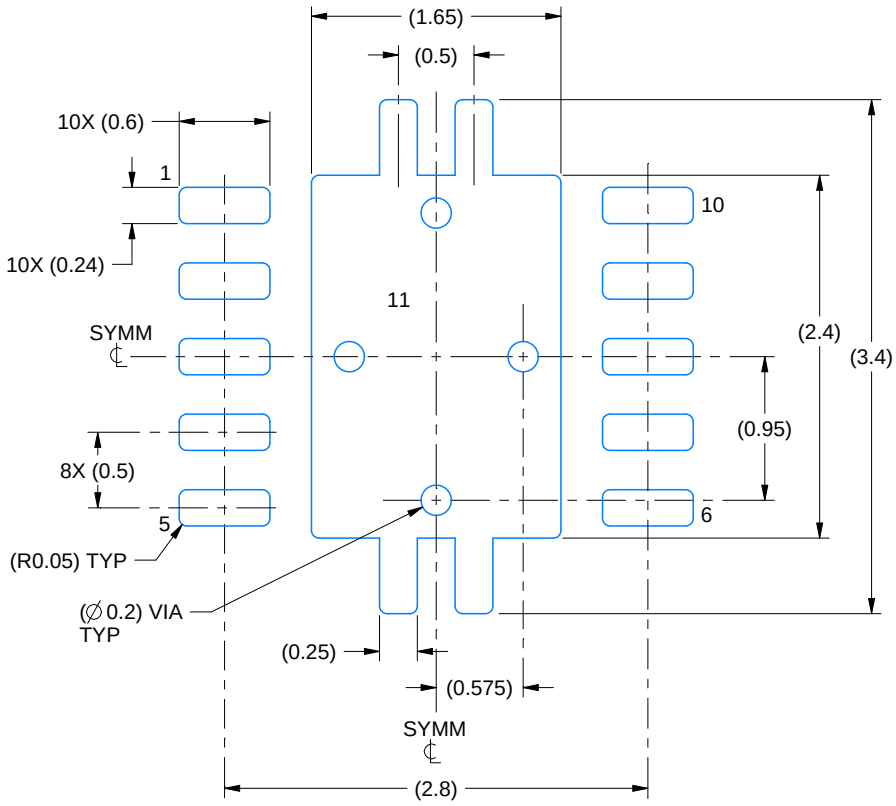
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

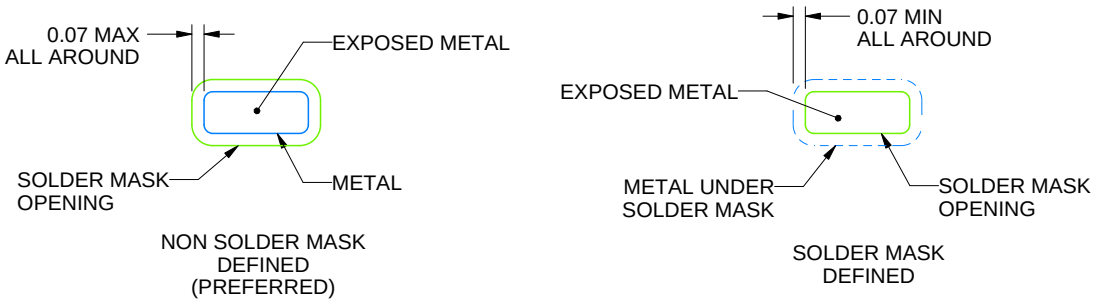


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

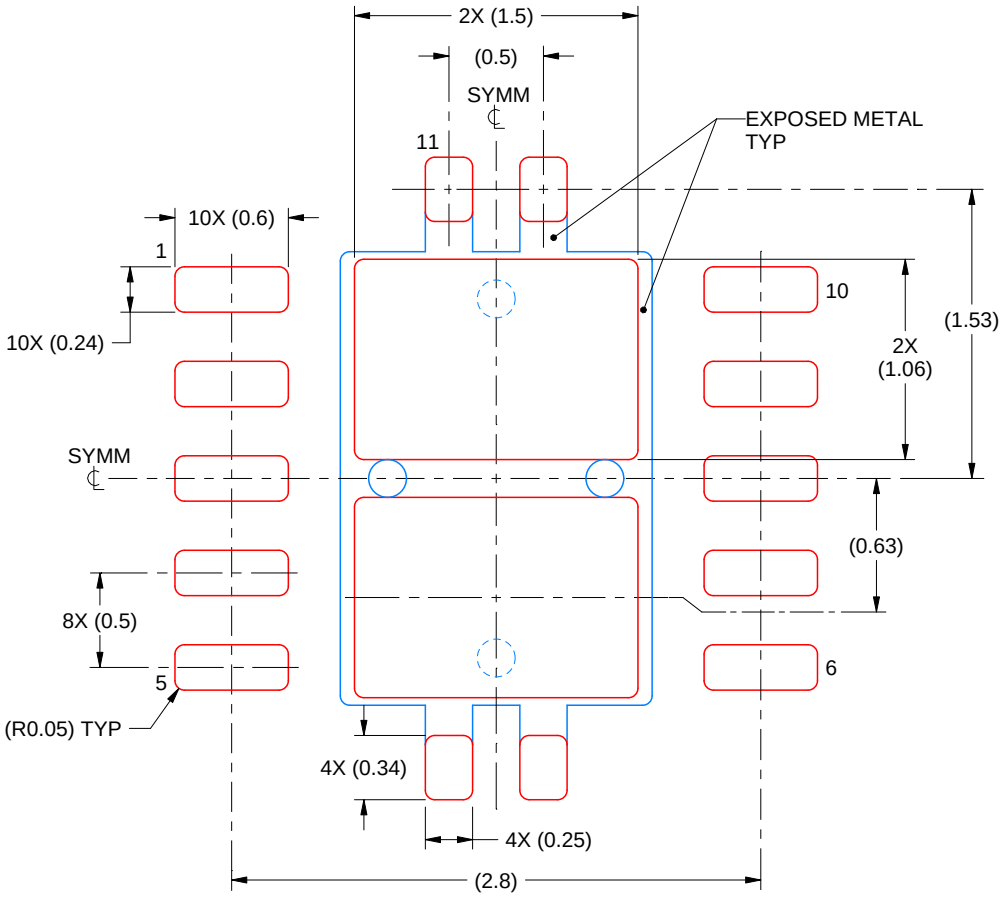
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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