TEXAS INSTRUMENTS
INA138-Q1, INA168-Q1
JAJSCM9J – SEPTEMBER 2003 – REVISED AUGUST 2018

INA1x8-Q1 車載用グレード、ハイサイド、電流出力、電流シャント・モニタ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード 1: 動作時周囲温度範囲 –40℃～125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC6
- 完全なユニポーラのハイサイド電流測定回路
- 広い電源および同相電圧範囲:
  - INA138-Q1: 2.7V～36V
  - INA168-Q1: 2.7V～60V
- 独立した電源電圧と同相入力電圧
- 1つの抵抗器でゲインを設定可能
- 低い静止電流（標準値25μA）
- 広い温度範囲: －40℃～＋125℃
- パッケージ: TSSOP-8、SOT-23-5 (INA168-Q1)

2 アプリケーション

- 電動パワー・ステアリング(EPS)システム
- 車体制御モジュール
- ブレーキ・システム
- 横滑り防止装置(ESC)システム

3 概要

INA138-Q1およびINA168-Q1 (INA1x8-Q1)はハイサイド、単方向の電流センシング・アンプです。同相入力電圧範囲が広く、静止電流が小さく、TSSOPおよびSOT-23パッケージに格納されているため、さまざまな用途に使用できます。

入力同相電圧と電源電圧はそれぞれ独立しており、INA138-Q1では2.7V～36V、INA168-Q1では2.7V～60Vです。静止電流はわずか25μAで、電流測定シャントのいずれの側にも電源を接続でき、誤差を最小限に抑えることができます。

本デバイスは差動入力電圧を電流出力に変換します。1～100以上の範囲で任意のゲインを設定できる外付けの負荷抵抗器を使用してこの電流が逆に変換され、電圧値が得られます。本回路は電流シャント測定向けに設計されていますが、測定やレベルシフトなど、さまざまなアプリケーションにご使用ください。

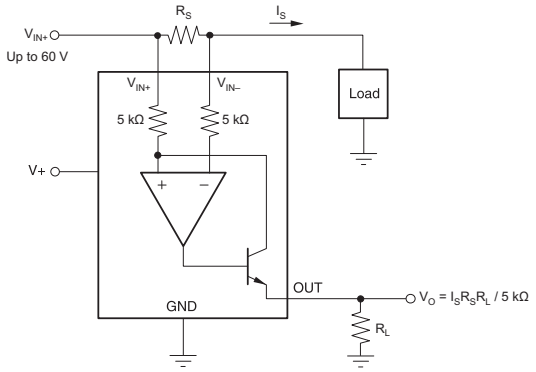
どちらのデバイスも、TSSOP-8パッケージで供給されます。INA168-Q1は、SOT-23-5パッケージでも供給されます。どちらのデバイスも、-40℃～+125℃の温度範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
INA138-Q1	TSSOP (8)	4.40mm×3.00mm
INA168-Q1		
INA168-Q1	SOT-23 (5)	2.90mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション回路



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision I (January 2018) から **Revision J** に変更 **Page**

- Added "V_{SENSE} =" to differential analog input voltage label in *Absolute Maximum Ratings* table ... 5
- Changed maximum differential analog input voltage from 2 V to 40 V in *Absolute Maximum Ratings* table ... 5
- Added new note 2 to *Absolute Maximum Ratings* table ... 5
- Added output current row with upper limit of 400 µA to *Absolute Maximum Ratings* table ... 5

Revision H (May 2016) から **Revision I** に変更 **Page**

- Changed *Thermal Information* data for INA168-Q1 DBV device ... 6

Revision G (January 2014) から **Revision H** に変更 **Page**

- 「*アプリケーション*」の箇条書きを変更 ... 1
- 「*製品情報*」セクション、「*ESD定格*」表、「*推奨動作条件*」セクション、「*熱に関する情報*」セクション、「*機能説明*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- 特長の箇条書きに車載用認定の項目を追加、古い項目を削除 ... 1
- すべての図にピン名を追加し、ピン番号をすべて削除 ... 1
- Deleted Ordering Information table; information available in the Package Option Addendum at the end of this data sheet 4
- Added missing minus sign to V_{IN-} pin in pin configuration figures ... 4
- Deleted thermal resistance from *Absolute Maximum Ratings* table; see new *Thermal Information* table ... 5
- Changed $R_{\theta JA}$ value for both packages ... 6
- Changed V_S to V+ throughout data sheet for consistency ... 6
- Changed R_{OUT} in *Electrical Characteristics* table to R_L for consistency ... 6
- Changed V_{IN} to V_{SENSE} in Figure 4 ... 7
- Deleted V_S symbol from text regarding voltage drop in *Operation* section ... 10
- Changed 10 µA to 100 µA in *Operation* section (typo) ... 10
- Changed Figure 9; removed incorrect pin numbers, and moved embedded table to outside of figure ... 11

- Changed Figure 10 12
- Changed Figure 15 16

Revision F (November 2013) から Revision G に変更 **Page**

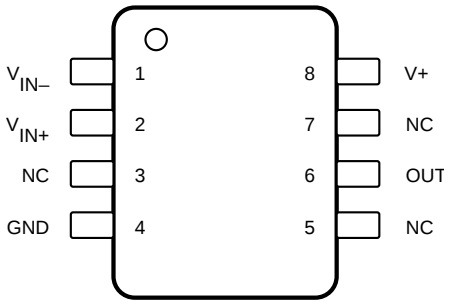
- ドキュメント全体を通して複数の場所で部品番号をIN168-Q1からINA168-Q1に変更 1

Revision E (September 2012) から Revision F に変更 **Page**

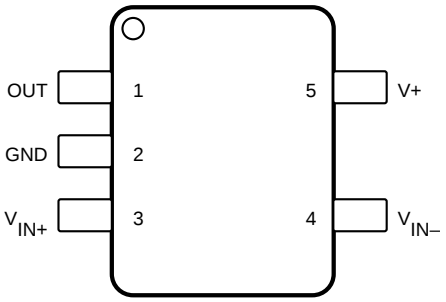
- Corrected Y-axis label of QUIESCENT CURRENT versus POWER-SUPPLY VOLTAGE graph 7

5 Pin Configuration and Functions

PW Package
8-Pin TSSOP
Top View



DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	INA138-Q1, INA168-Q1	INA168-Q1		
	TSSOP−8	SOT-23−5		
GND	4	2	—	Ground
NC	3, 5, 7	—	—	No internal connection
OUT	6	1	O	Output current
V+	8	5	I	Power-supply voltage
V_{IN-}	1	4	I	Negative input voltage
V_{IN+}	2	3	I	Positive input voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
Voltage	Supply, V+		INA138-Q1	–0.3	60	V
			INA168-Q1	–0.3	75	
	Analog inputs, V_{IN+}, V_{IN-}	Common-mode	INA138-Q1	–0.3	60	
			INA168-Q1	–0.3	75	
		Differential, $V_{SENSE} = (V_{IN+} - V_{IN-})$(2)		–40	40	
	Analog output, OUT			–0.3	40	
Current	Output current, I_{OUT}(2)				400	µA
Temperature	Operating, T_A			–55	150	°C
	Junction, T_J				150	
	Storage, T_{stg}			–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Use the following equation to make sure that the maximum value of I_{OUT} in a given application is less than 400 µA:

$$I_{OUT,MAX} = MIN\left(\frac{V_{SENSE,MAX}}{5\ k\Omega}, \frac{V_{IN+,MAX}}{10\ k\Omega + R_{LOAD}}, \frac{V+_{MAX}}{5\ k\Omega + R_{LOAD}}\right)$$

where:

- $I_{OUT,MAX}$ is the estimated maximum value of I_{OUT}
- $V_{SENSE,MAX}$ is the maximum possible value of the differential input voltage in the application
- $V_{IN+,MAX}$ is the maximum possible value of V_{IN+} in the application
- $V+_{MAX}$ is the maximum possible value of V+ in the application
- R_{LOAD} is the value of the load resistor in kΩ

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V+	INA138-Q1	2.7	5	36	V
	INA168-Q1	2.7	5	60	
Common-mode voltage	INA138-Q1	2.7	12	36	V
	INA168-Q1	2.7	12	60	
Operating temperature, T_A		–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		INA138-Q1, INA168-Q1	INA168-Q1	UNIT
		PW (TSSOP)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179.1	168.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.6	73.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	107.7	28.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.0	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.0	27.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = −40°C to +125°C, V+ = 5 V, V_{IN+} = 12 V, and R_L = 125 kΩ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	INA138-Q1			INA168-Q1			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Full-scale sense voltage	$V_{SENSE} = V_{IN+} - V_{IN-}$		100	500		100	500	mV
Common-mode rejection	V_{IN+} = 2.7 V to 36 V, V_{SENSE} = 50 mV	100	120					dB
	V_{IN+} = 2.7 V to 60 V, V_{SENSE} = 50 mV				100	120		
Offset voltage[1]			±0.2	±2		±0.2	±2	mV
Offset voltage vs temperature			1			1		µV/°C
Offset voltage vs power supply (V+)	V+ = 2.7 V to 36 V, V_{SENSE} = 50 mV		0.1	10				µV/V
	V+ = 2.7 V to 60 V, V_{SENSE} = 50 mV					0.1	10	
Input bias current	$V_{IN+} = V_{IN-}$ = 12 V			10			10	µA
OUTPUT								
Transconductance	V_{SENSE} = 10 mV to 150 mV	194		206	194		206	µA/V
Transconductance versus temperature	V_{SENSE} = 100 mV		10			10		nA/°C
Nonlinearity error	V_{SENSE} = 10 mV to 150 mV		±0.01%	±0.2 %		±0.01%	±0.2 %	
Total output error	V_{SENSE} = 100 mV		±0.5%	±3.2%		±0.5%	±3.2%	
Output impedance			1 || 5			1 || 5		GΩ || pF
Voltage output swing to power supply (V+)			(V+) – 0.8	(V+) – 1.2		(V+) – 0.8	(V+) – 1.2	V
Voltage output swing to common mode, V_{CM}			V_{CM} – 0.5	V_{CM} – 1.2		V_{CM} – 0.5	V_{CM} – 1.2	V
FREQUENCY RESPONSE								
Bandwidth	R_L = 5 kΩ		800			800		kHz
	R_L = 125 kΩ		32			32		
Settling time (0.1%)	5-V step, R_L = 5 kΩ		1.8			1.8		µs
	5-V step, R_L = 125 kΩ		30			30		
NOISE								
Output-current noise density	T_A = 25°C		9			9		pA/√Hz
Total output-current noise	BW = 100 kHz		3			3		nA RMS
POWER SUPPLY								
Quiescent current	V_{SENSE} = 0 V, I_O = 0 mA		25	60		25	60	µA

(1) Defined as the amount of input voltage, V_{SENSE}, to drive the output to zero.

6.6 Typical Characteristics

at T_A = 25°C, V+ = 5 V, V_{IN+} = 12 V, and R_L = 125 kΩ (unless otherwise noted)

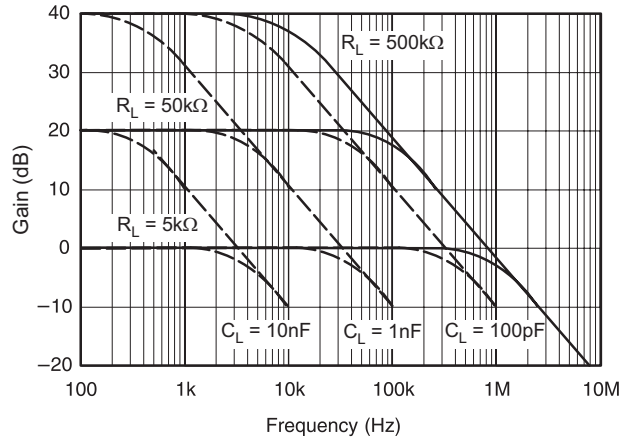


Figure 1. Gain vs Frequency

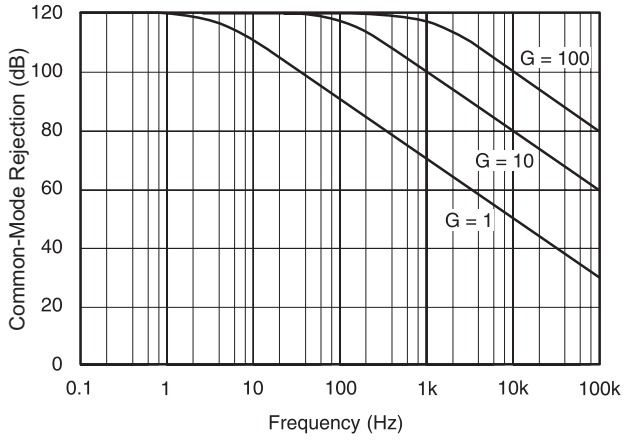


Figure 2. Common-Mode Rejection vs Frequency

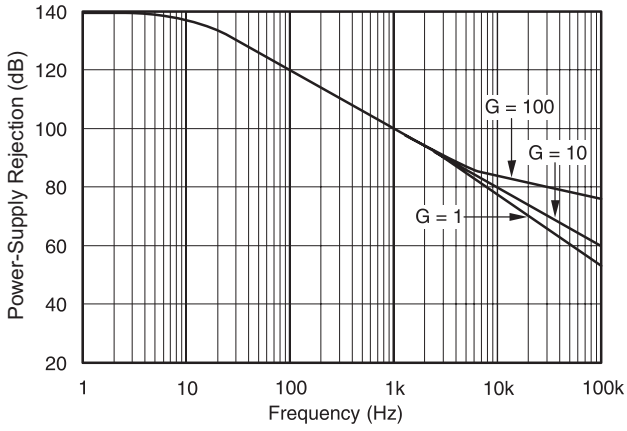


Figure 3. Power-Supply Rejection vs Frequency

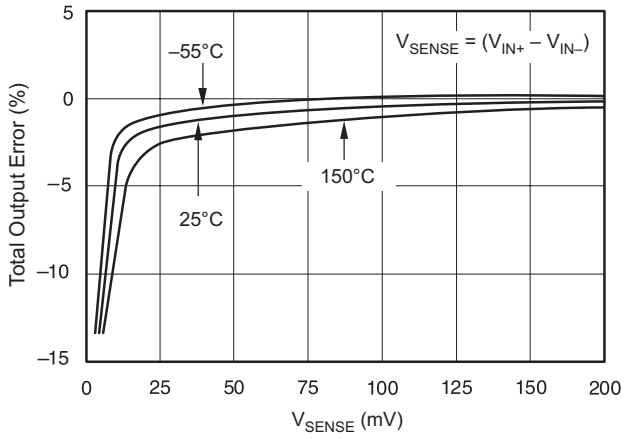


Figure 4. Total Output Error vs V_{SENSE}

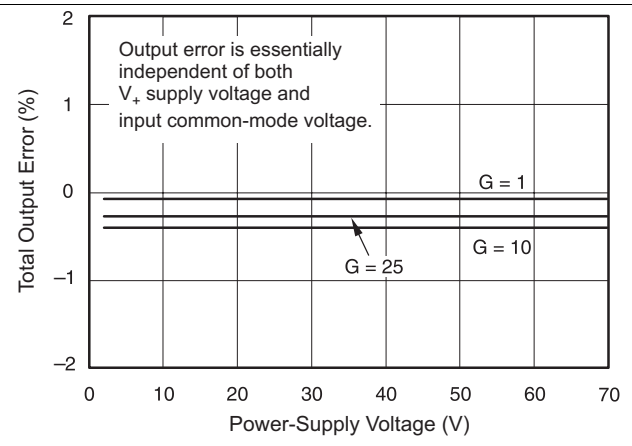


Figure 5. Total Output Error vs Power-Supply Voltage

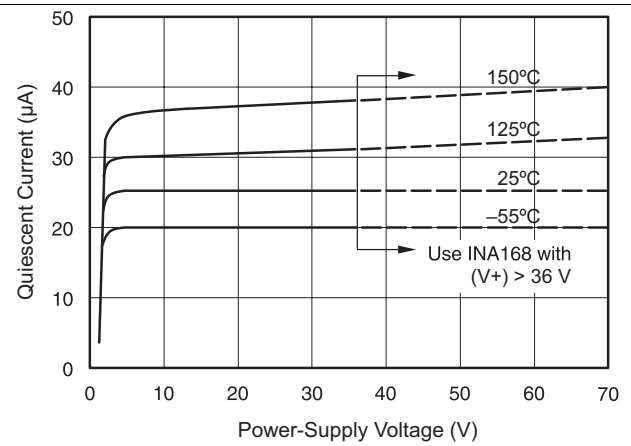


Figure 6. Quiescent Current vs Power-Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V_{IN+} = 12 V, and R_L = 125 kΩ (unless otherwise noted)

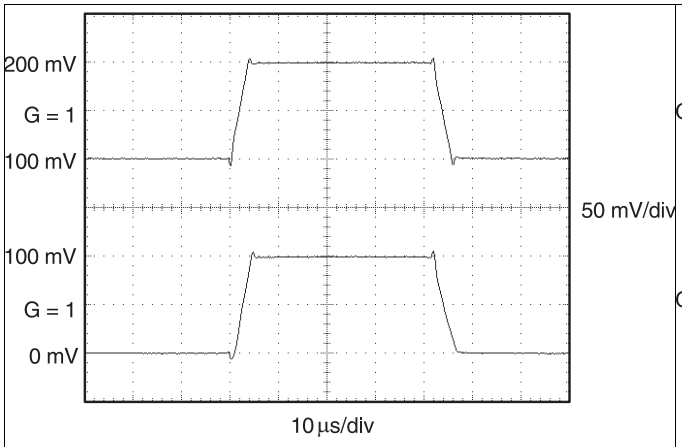


Figure 7. Step Response

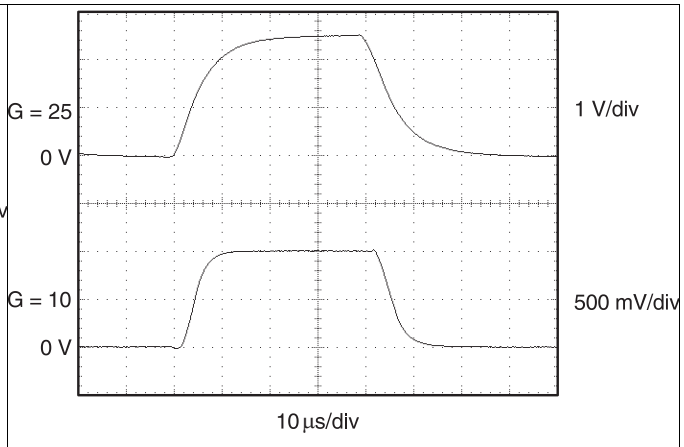


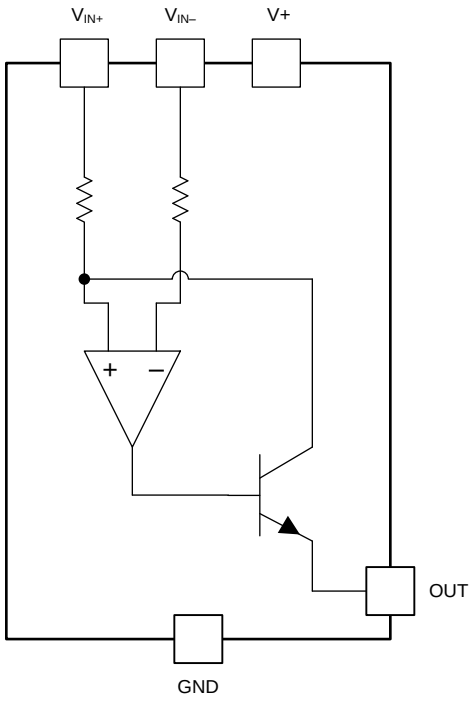
Figure 8. Step Response

7 Detailed Description

7.1 Overview

The INA138-Q1 and INA168-Q1 devices (INA1x8-Q1) are comprised of a high-voltage, precision operational amplifier, precision thin film resistors trimmed in production to an absolute tolerance, and a low-noise output transistor. The INA1x8-Q1 are powered from a single power supply, and the input voltages can exceed the power supply voltage. The INA1x8-Q1 are ideal for measuring small differential voltages, such as those generated across a shunt resistor, in the presence of large common-mode voltages. The *Functional Block Diagram* shows the functional components within both the INA138-Q1 and INA168-Q1 devices.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Voltage Range

The output of the INA1x8-Q1 is a current that is converted to a voltage by the load resistor, R_L. The output current remains accurate within the compliance voltage range of the output circuitry. The shunt voltage and the input common-mode and power-supply voltages limit the maximum possible output swing. The maximum output voltage ($V_{out\ max}$) compliance is limited by either Equation 1 or Equation 2, whichever is lower:

$$V_{out\ max} = (V+) - 0.7\ V - (V_{IN+} - V_{IN-}) \quad (1)$$

or

$$V_{out\ max} = V_{IN-} - 0.5\ V \quad (2)$$

7.3.2 Bandwidth

Measurement bandwidth is affected by the value of the load resistor, R_L. High gain produced by high values of R_L yields a narrower measurement bandwidth (see the *Typical Characteristics* section). For the widest possible bandwidth, keep the capacitive load on the output to a minimum. Reduction in bandwidth due to capacitive load is shown in the *Typical Characteristics* section.

If bandwidth limiting (filtering) is desired, add a capacitor to the output (see Figure 12). This capacitor does not cause instability.

7.4 Device Functional Modes

For proper operation, the INA1x8-Q1 must operate within the specified limits. Operating either device outside of their specified power-supply voltage range, or their specified common-mode range, results in unexpected behavior, and is not recommended. Additionally, operating the output beyond the specified limits with respect to power-supply voltage and input common-mode voltage also produces unexpected results. See the *Electrical Characteristics* section for the device specifications.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Operation

Figure 9 illustrates the basic circuit diagram for both the INA138-Q1 and INA168-Q1. Load current I_S is drawn from supply V_P through shunt resistor R_S. The voltage drop in the shunt resistor is forced across R_{G1} by the internal op amp, causing current to flow into the collector of Q1. External resistor R_L converts the output current, I_O, to a voltage, V_{OUT}, at the OUT pin. The transfer function for the INA1x8-Q1 is shown in Equation 3:

$$I_O = g_m (V_{IN+} - V_{IN-})$$

where

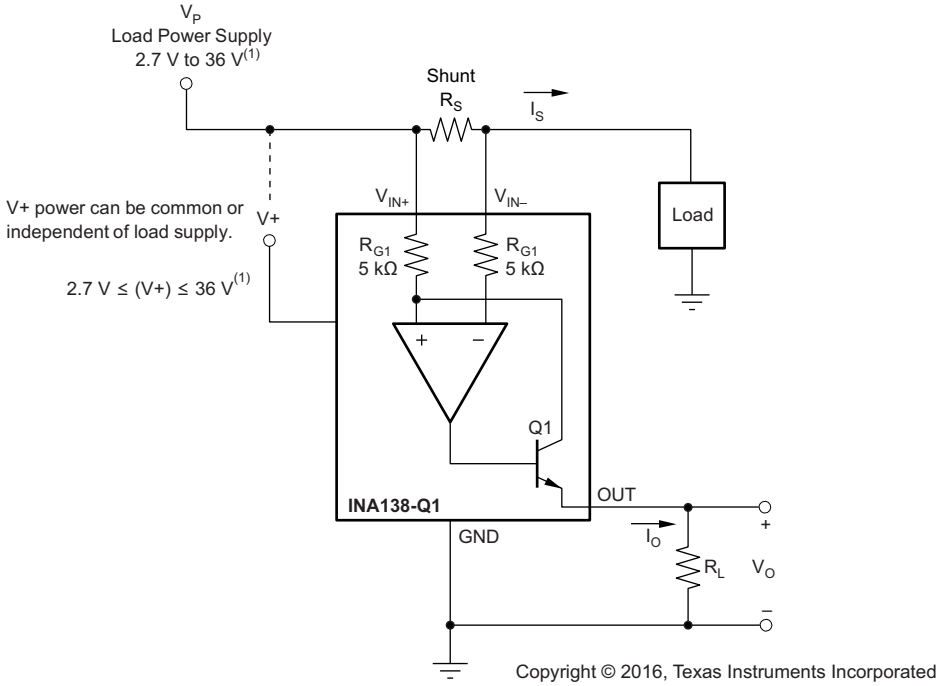
- g_m = 200 µA/V (3)

In the circuit of Figure 9, the input voltage, ($V_{IN+} - V_{IN-}$), is equal to $I_S \times R_S$. The output voltage, V_{OUT}, is equal to $I_O \times R_L$. The transconductance, g_m, of the INA1x8-Q1 is 200 µA/V. The complete transfer function for the current measurement amplifier in this application is shown in Equation 4:

$$V_{OUT} = (I_S)\ (R_S)\ (200\ \mu A/V)\ (R_L) \quad (4)$$

The maximum differential input voltage for accurate measurements is 0.5 V, producing a 100-µA output current. A differential input voltage of up to 2 V does not cause damage. Differential measurements (V_{IN+} and V_{IN-} pins) must be unipolar, with a more-positive voltage applied to the V_{IN+} pin. If a more-negative voltage is applied to the V_{IN+} pin, I_O goes to zero, but no damage occurs.

Application Information (continued)



(1) Maximum V_P and V+ voltage is 60 V with INA168-Q1.

Figure 9. Basic Circuit Connections

Table 1. Voltage Gains and Corresponding Load-Resistor Values

VOLTAGE GAIN	EXACT R_L (kΩ)	NEAREST 1% R_L (kΩ)
1	5	4.99
2	10	10
5	25	24.9
10	50	49.9
20	100	100
50	250	249
100	500	499

8.2 Typical Applications

The INA1x8-Q1 are designed for current-shunt measurement circuits (see Figure 9) but its basic function is useful in a wide range of circuitry. With a little creativity, many unforeseen uses can be found in measurement and level-shifting circuits. A few ideas are illustrated in the following subsections.

8.2.1 Buffering Output to Drive an ADC

Digitize the output of the INA138-Q1 or INA168-Q1 devices using a 1-MSPS analog-to-digital converter (ADC).

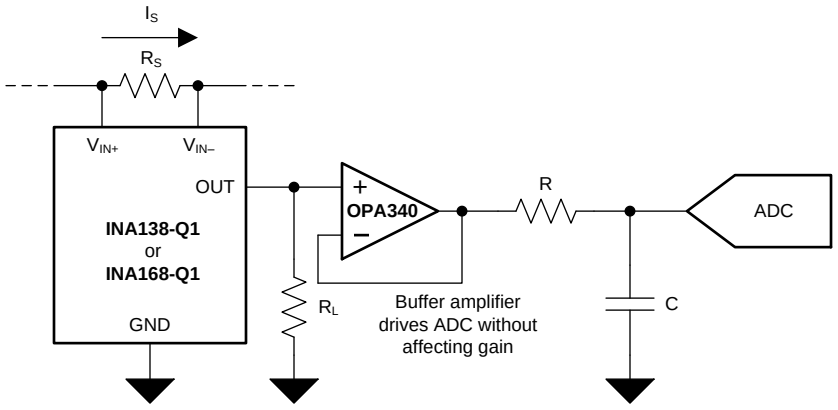


Figure 10. Buffering Output to Drive an ADC

8.2.1.1 Design Requirements

For this design example, use the input parameters shown in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, V+	5 V
Common-mode voltage, V_{CM}	INA138-Q1: 2.7 V to 36 V
	INA168-Q1: 2.7 V to 60 V
Full-scale shunt voltage, V_{SENSE}	50 mV to 100 mV
Load resistor, R_L	5 kΩ to 500 kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Selecting R_S and R_L

In Figure 10, the value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, best performance is attained with an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is 500 mV.

Choose an R_L that provides the desired full-scale output voltage. The output impedance of the INA1x8-Q1 OUT pin is very high, permitting the use of R_L values up to 500 kΩ with excellent accuracy. The input impedance of any additional circuitry at the output must be much higher than the value of R_L to avoid degrading accuracy.

Some ADCs have input impedances that significantly affects measurement gain. The input impedance of the ADC can be included as part of the effective R_L if the ADC input can be modeled as a resistor to ground. Alternatively, an op amp can be used to buffer the ADC input, as shown in Figure 10. The INA1x8-Q1 are current output devices, and as such, have an inherently large output impedance. The output currents from the amplifier are converted to an output voltage using the load resistor, R_L, connected from the amplifier output to ground. The ratio of the load resistor value to that of the internal resistor value determines the voltage gain of the system.

In many applications, digitizing the output of the INA1x8-Q1 is required. Digitizing is accomplished by connecting the output of the amplifier to an ADC. It is very common for an ADC to have a dynamic input impedance. If the INA1x8-Q1 output is connected directly to an ADC input, the input impedance of the ADC is effectively connected in parallel with gain setting resistor R_L. This parallel impedance combination affects the gain of the system and the impact on the gain is difficult to estimate accurately. A simple solution that eliminates the paralleling of impedances, and simplifies the gain of the circuit is to place a buffer amplifier, such as the OPA340, between the output of the INA1x8-Q1 and the input to the ADC.

Figure 10 illustrates this concept. Notice that a low-pass filter is placed between the OPA340 output and the input to the ADC. The filter capacitor is required to provide any instantaneous demand for current required by the input stage of the ADC. The filter resistor is required to isolate the OPA340 output from the filter capacitor in order to maintain circuit stability. The values for the filter components vary according to the operational amplifier used for the buffer and the particular ADC selected. More information regarding the design of the low-pass filter is found in the TI Precision Design, *16 bit 1MSPS Data Acquisition Reference Design for Single-Ended Multiplexed Applications*.

Figure 11 shows the expected results when driving an ADC at 1 MSPS with and without buffering the INA1x8-Q1 output. Without the buffer, the high impedance of the INA1x8-Q1 reacts with the input capacitance and sample-and-hold capacitance of the ADC, and does not allow the sampled value to reach the correct final value before the ADC is reset, and the next conversion starts. Adding the buffer amplifier significantly reduces the output impedance driving the sample-and-hold circuitry, and allows for higher conversion rates.

8.2.1.3 Application Curve

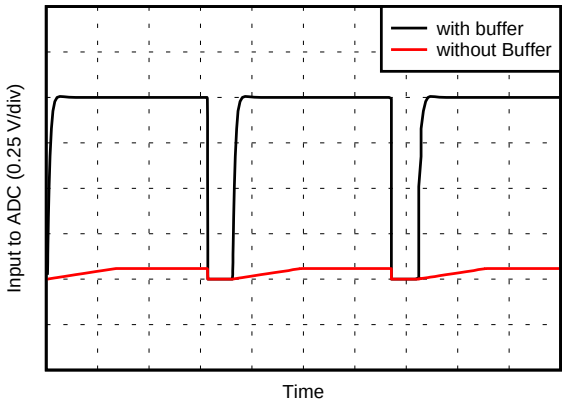


Figure 11. Driving an ADC With and Without a Buffer

8.2.2 Output Filter

Filter the output of the INA1x8-Q1 devices.

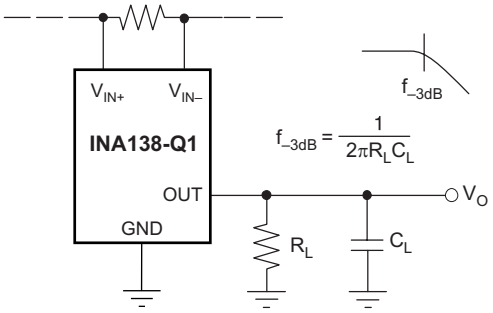


Figure 12. Output Filter

8.2.2.1 Design Requirements

For this design example, use the input parameters shown in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, V+	INA138-Q1: 2.7 V to 36 V
	INA168-Q1: 2.7 V to 60 V
Common-mode voltage, V_{CM}	INA138-Q1: 2.7 V to 36 V
	INA168-Q1: 2.7 V to 60 V
Full-scale shunt voltage, V_{SENSE}	50 mV to 100 mV
Load resistor, R_L	5 kΩ to 500 kΩ

8.2.2.2 Detailed Design Procedure

A low-pass filter can be formed at the output of the INA1x8-Q1 simply by placing a capacitor of the desired value in parallel with the load resistor. First, determine the value of the load resistor needed to achieve the desired gain by using Table 1. Next, determine the capacitor value that results in the desired cutoff frequency according to the equation shown in Figure 12. Figure 13 shows various combinations of gain settings (determined by R_L) and filter capacitors.

8.2.2.3 Application Curve

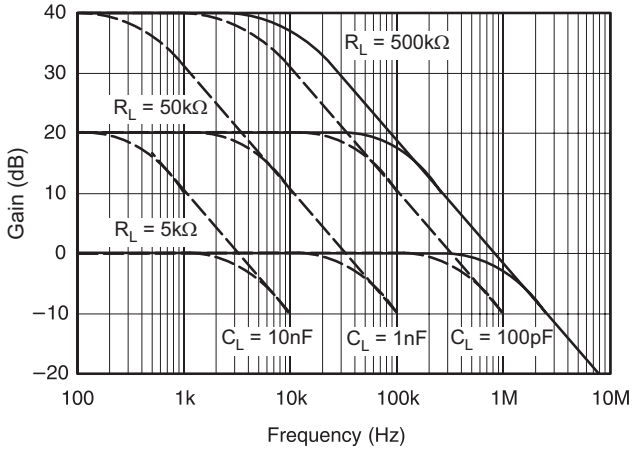


Figure 13. Gain vs Frequency

8.2.3 Offsetting the Output Voltage

For many applications using only a single power supply, the output voltage may have to be level shifted away from ground when there is no load current flowing in the shunt resistor. Level shifting the output of the INA1x8-Q1 is easily accomplished by one of two simple methods shown in Figure 14. Method (a) on the left-hand side of Figure 14 shows a simple voltage-divider method. This method is useful for applications that require the output of the INA1x8-Q1 to remain centered with respect to the power supply at zero load current through the shunt resistor. Using this method, the gain is determined by the parallel combination of R_1 and R_2, while the output offset is determined by the voltage divider ratio of R_1 and R_2, as shown in Figure 14(a). For applications that require a fixed value of output offset independent of the power-supply voltage, use current-source method (b) shown on the right-hand side of Figure 14. With this method, a REF200 constant current source is used to generate a constant output offset. Using this method, the gain is determined by R_L, and the offset is determined by the product of the value of the current source and R_L.

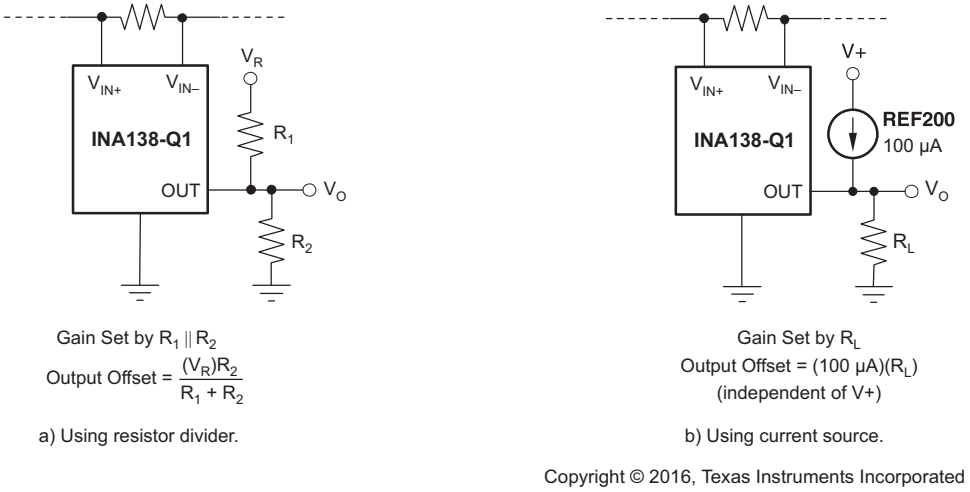


Figure 14. Offsetting the Output Voltage

8.2.4 Bipolar Current Measurement

Configure the INA1x8-Q1 as illustrated in Figure 15 for applications where bidirectional current measurement is required. Two INA1x8-Q1 devices are required; connect the inputs across the shunt resistor; see Figure 15. A comparator, such as the TLV3201, is used to detect the polarity of the load current. The magnitude of the load current is monitored across the resistor connected between ground and the connection labeled *Output*. In this example, the 100-kΩ resistor results in a gain of 20 V/V. The 10-kΩ resistors connected in series with the INA1x8-Q1 output current are used to develop a voltage across the comparator inputs. Two diodes are required to prevent current flow into the INA1x8-Q1 output because only one device at a time provides current to the *Output* connection of the circuit. The circuit functionality is illustrated in Figure 16.

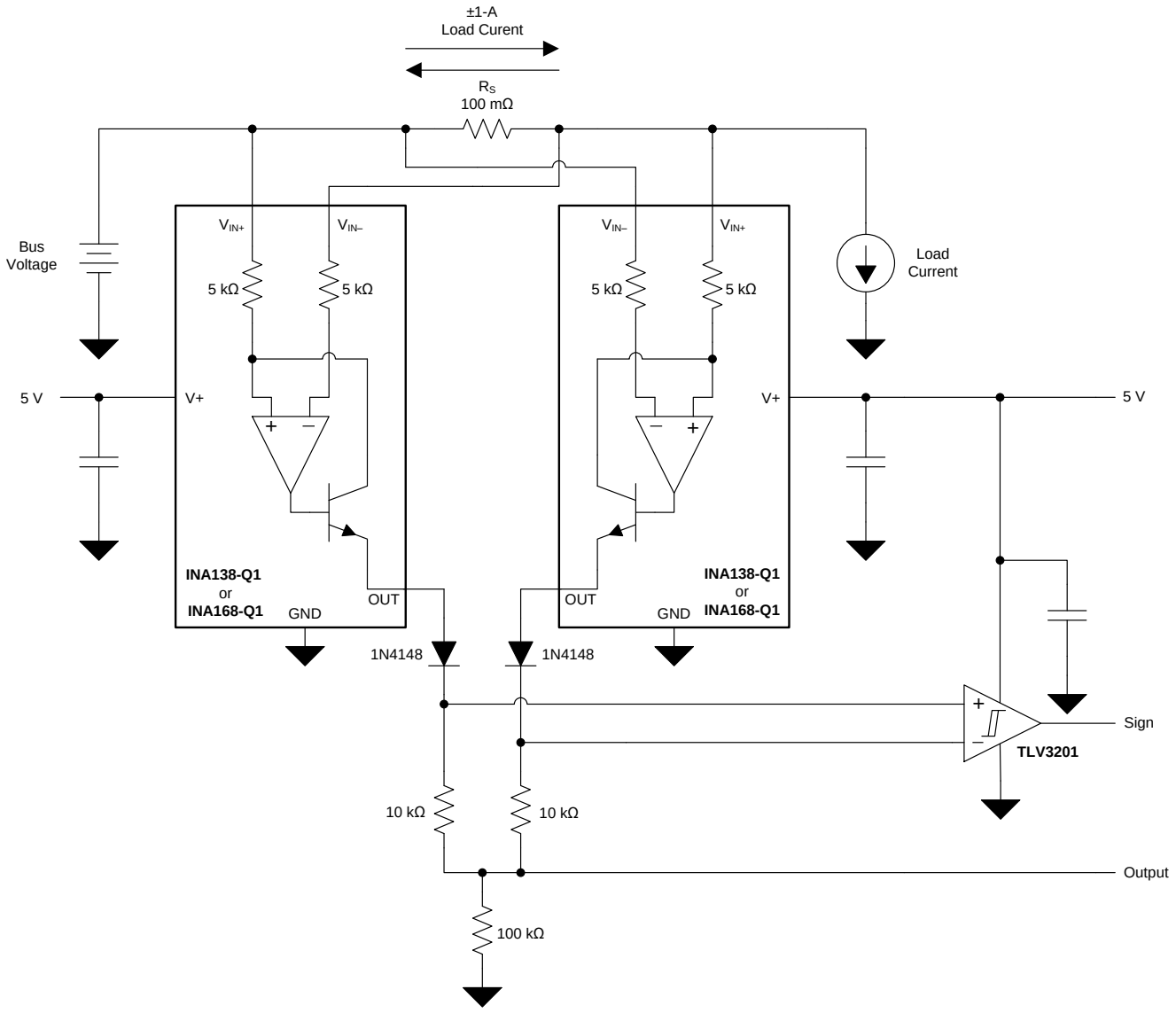


Figure 15. Bipolar Current Measurement

8.2.4.1 Application Curve

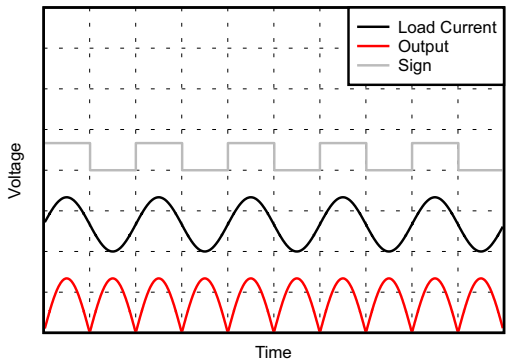
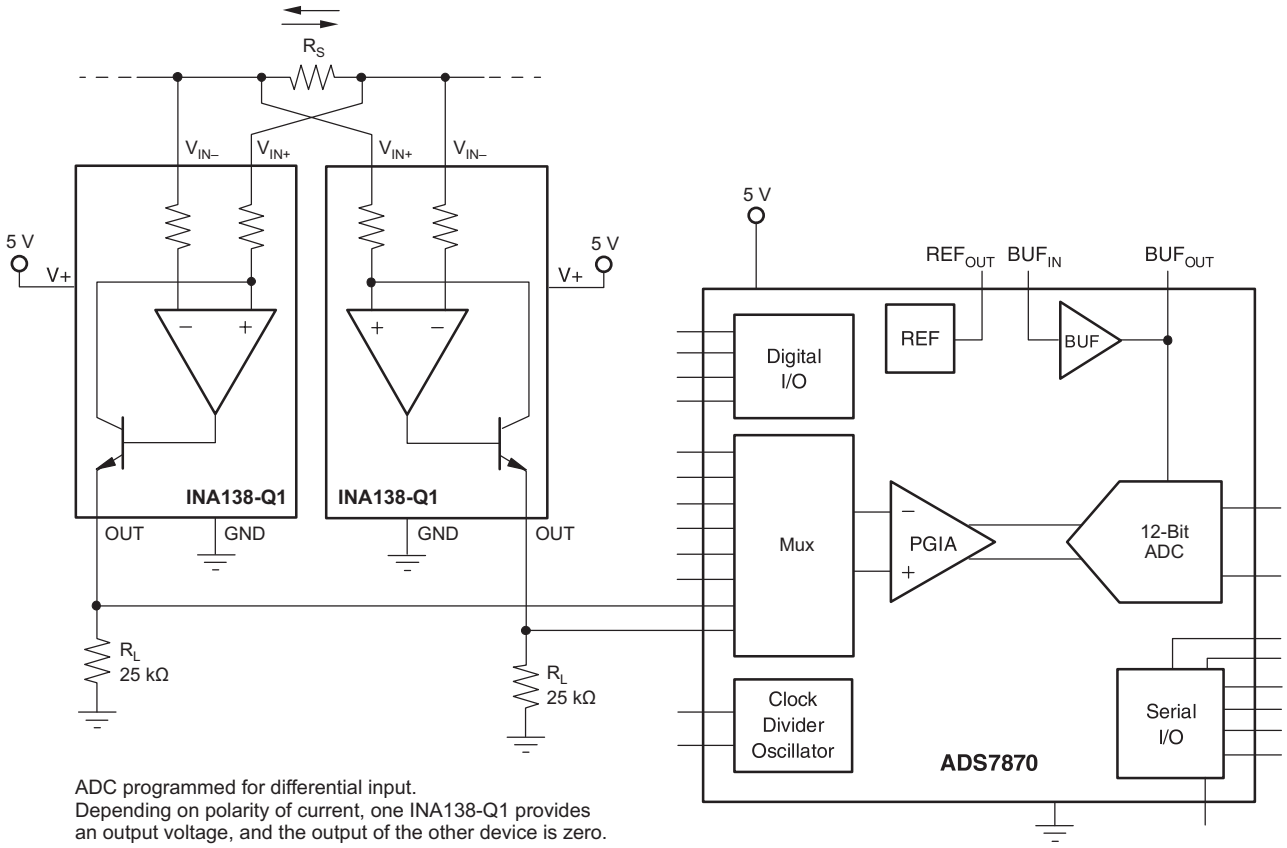


Figure 16. Bipolar Current Measurements Results (Arbitrary Scale)

8.2.5 Bipolar Current Measurement Using Differential Input of an ADC

Use the INA1x8-Q1 with an ADC such as the ADS7870 programmed for differential-mode operation; Figure 17 shows this configuration. In this configuration, the use of two INA138-Q1s or INA168-Q1s allows for bidirectional current measurement. Depending on the polarity of the current, one of the INA devices provides an output voltage, while the other INA device output is zero. In this way, the ADC reads the polarity of current directly, without the need for additional circuitry.



ADC programmed for differential input.
Depending on polarity of current, one INA138-Q1 provides an output voltage, and the output of the other device is zero.

Figure 17. Bipolar Current Measurement Using Differential Input of the ADC

8.2.6 Multiplexed Measurement Using Logic Signal for Power

Measure multiple loads as shown in Figure 18. In this configuration, each INA138-Q1 or INA168-Q1 device is powered by the digital I/O from the ADS7870. Multiplexing is achieved by switching on or off each desired I/O.

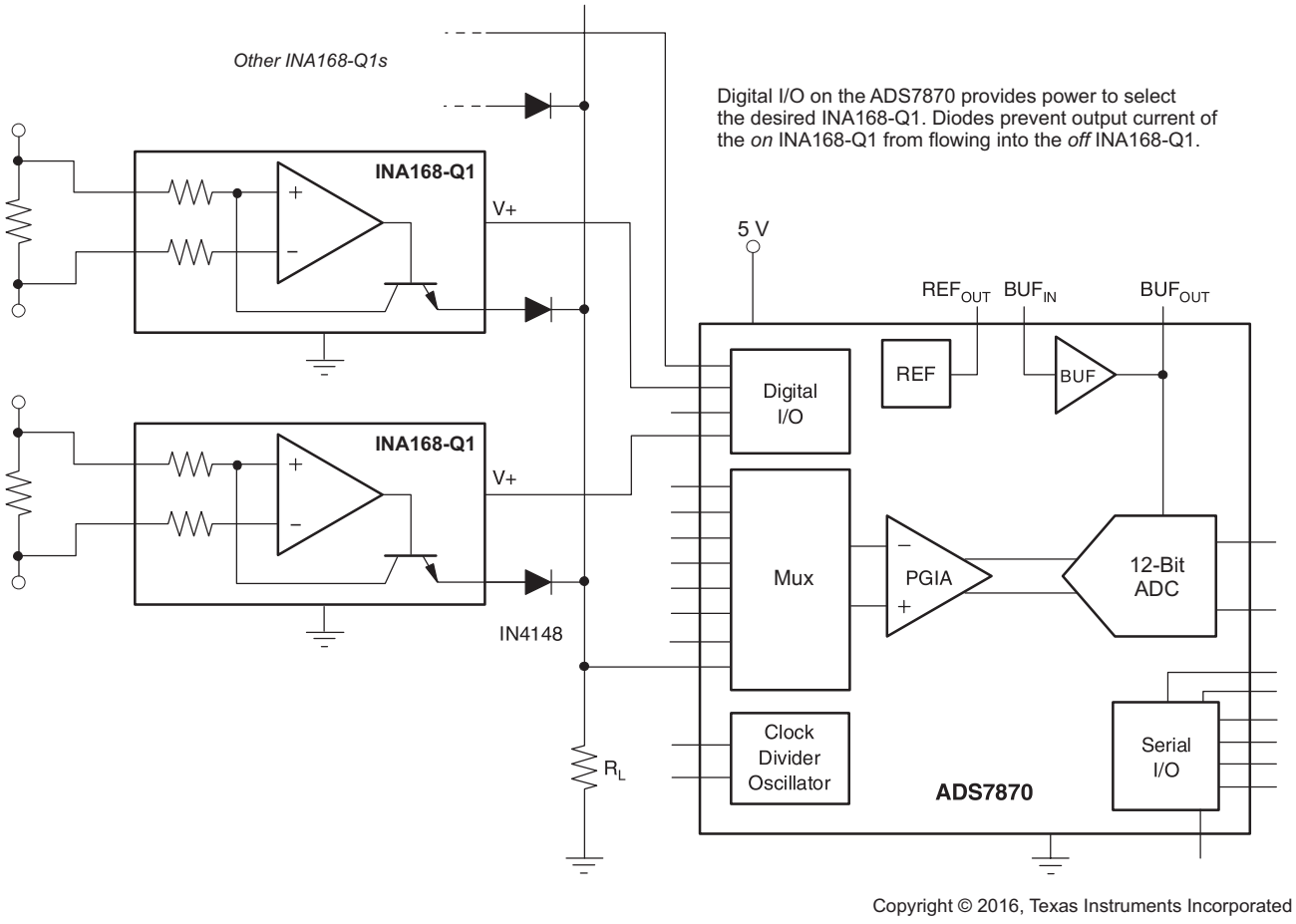


Figure 18. Multiplexed Measurement Using Logic Signal for Power

9 Power Supply Recommendations

The input circuitry of the INA1x8-Q1 can accurately measure beyond the power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage goes up to 36 V with the INA138-Q1, or 60 V with the INA168-Q1. However, the output voltage range of the OUT pin is limited by the lesser of the two voltages (see the *Output Voltage Range* section). Place a 0.1-µF capacitor near the power-supply pin on the INA1x8-Q1. Additional capacitance may be required for applications with noisy power-supply voltages.

10 Layout

10.1 Layout Guidelines

Figure 19 shows the basic connection of the INA1x8-Q1 in the TSSOP-8 package. Connect input pins V_{IN+} and V_{IN-} as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance. Output resistor R_L is shown connected between the OUT pin and ground. Best accuracy is achieved with the output voltage measured directly across R_L. Measuring directly across R_L is especially important in high-current systems where load current could flow in the ground connections and affect measurement accuracy.

No power-supply bypass capacitors are required for stability of the INA1x8-Q1. However, applications with noisy or high-impedance power supplies may require decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

10.2 Layout Example

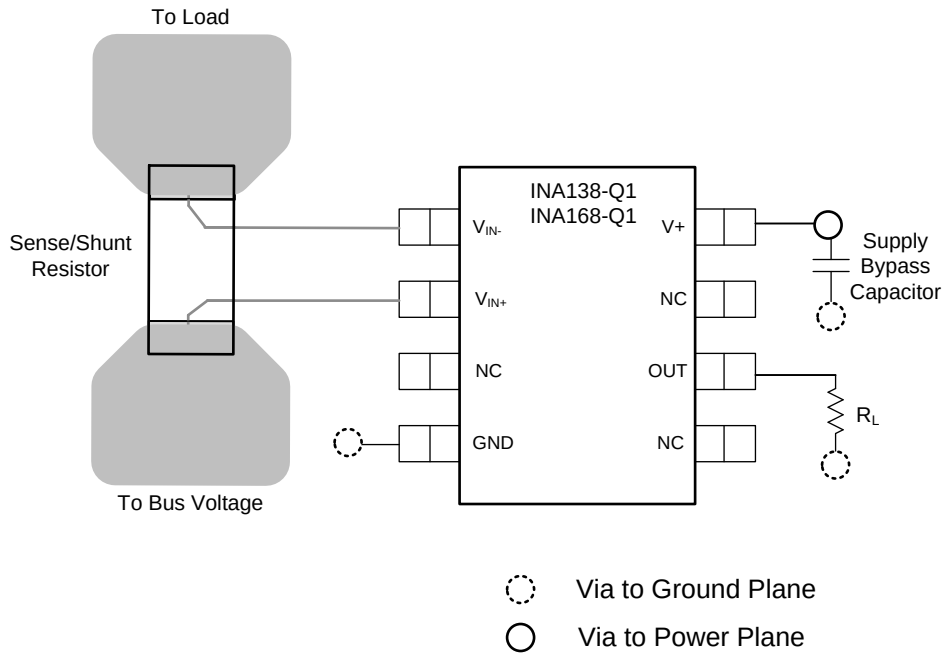


Figure 19. Typical Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

『シングルエンド・マルチプレクス・アプリケーション用の16ビット、1MSPSのデータ収集のリファレンス・デザイン』

11.2 関連リンク

表 4 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
INA138-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
INA168-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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11.6 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA138QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA138	Samples
INA168QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LUIQ	Samples
INA168QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA168	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

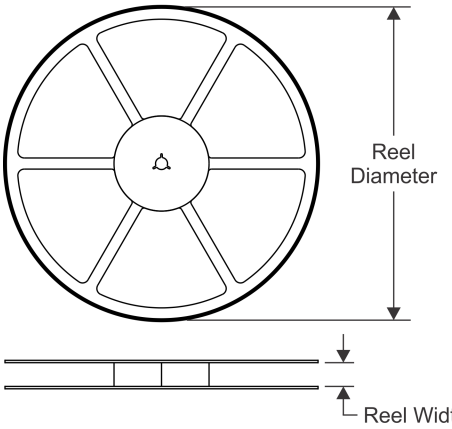
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

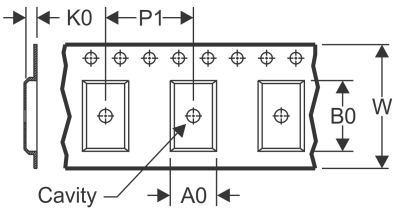
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

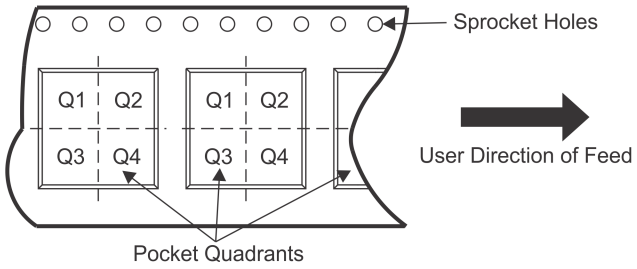


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

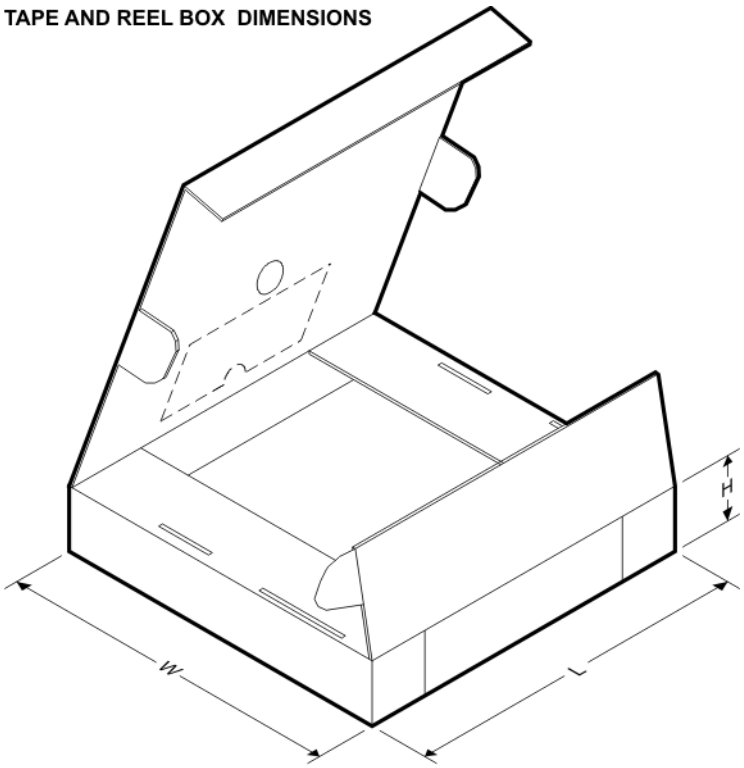
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA138QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA168QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
INA168QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

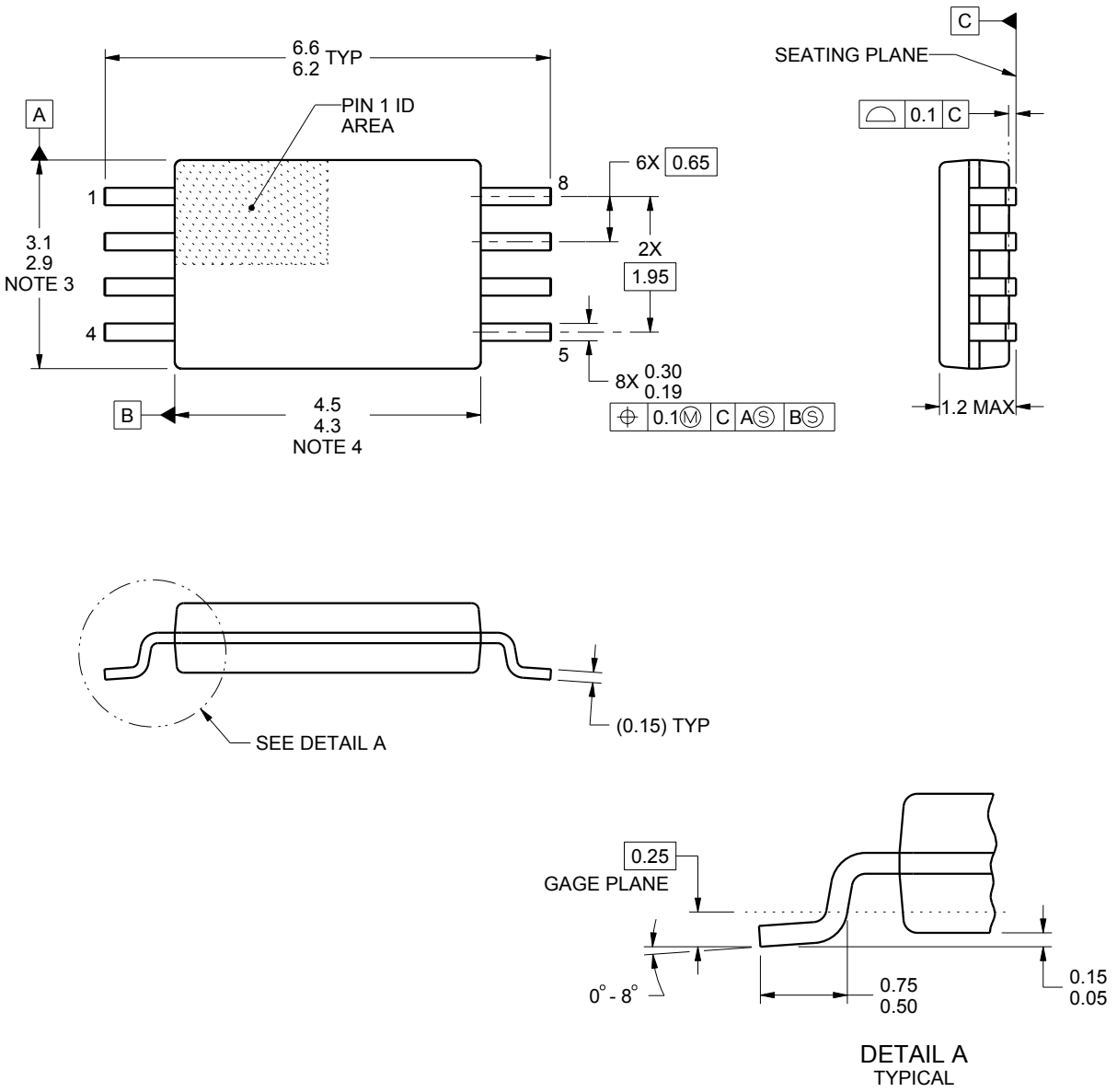
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA138QPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0
INA168QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA168QPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0008A

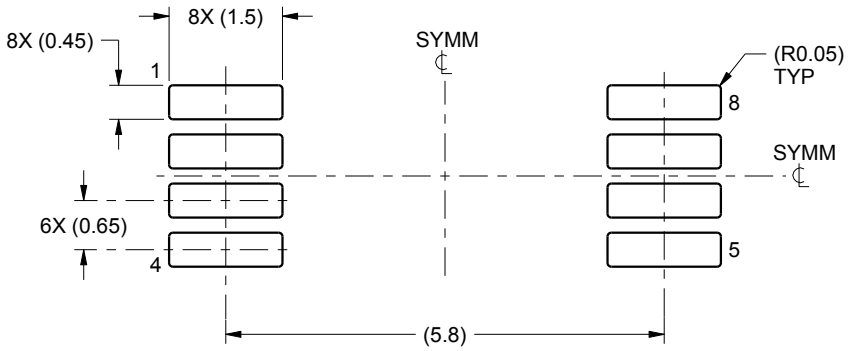
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

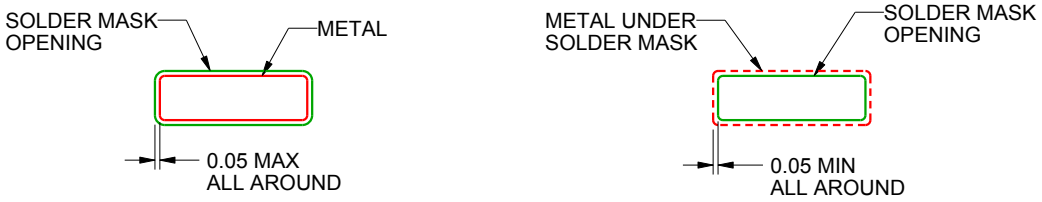


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

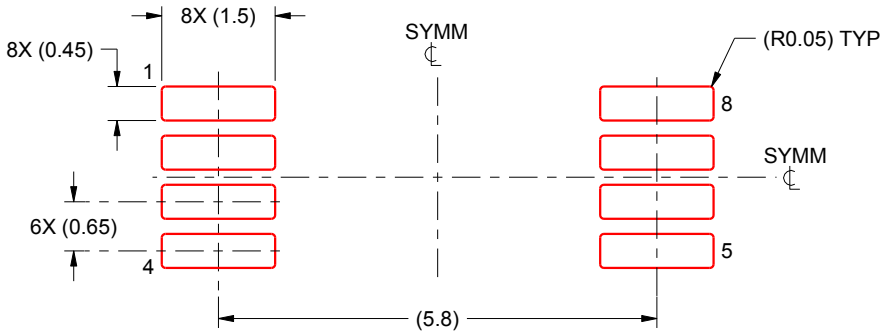


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

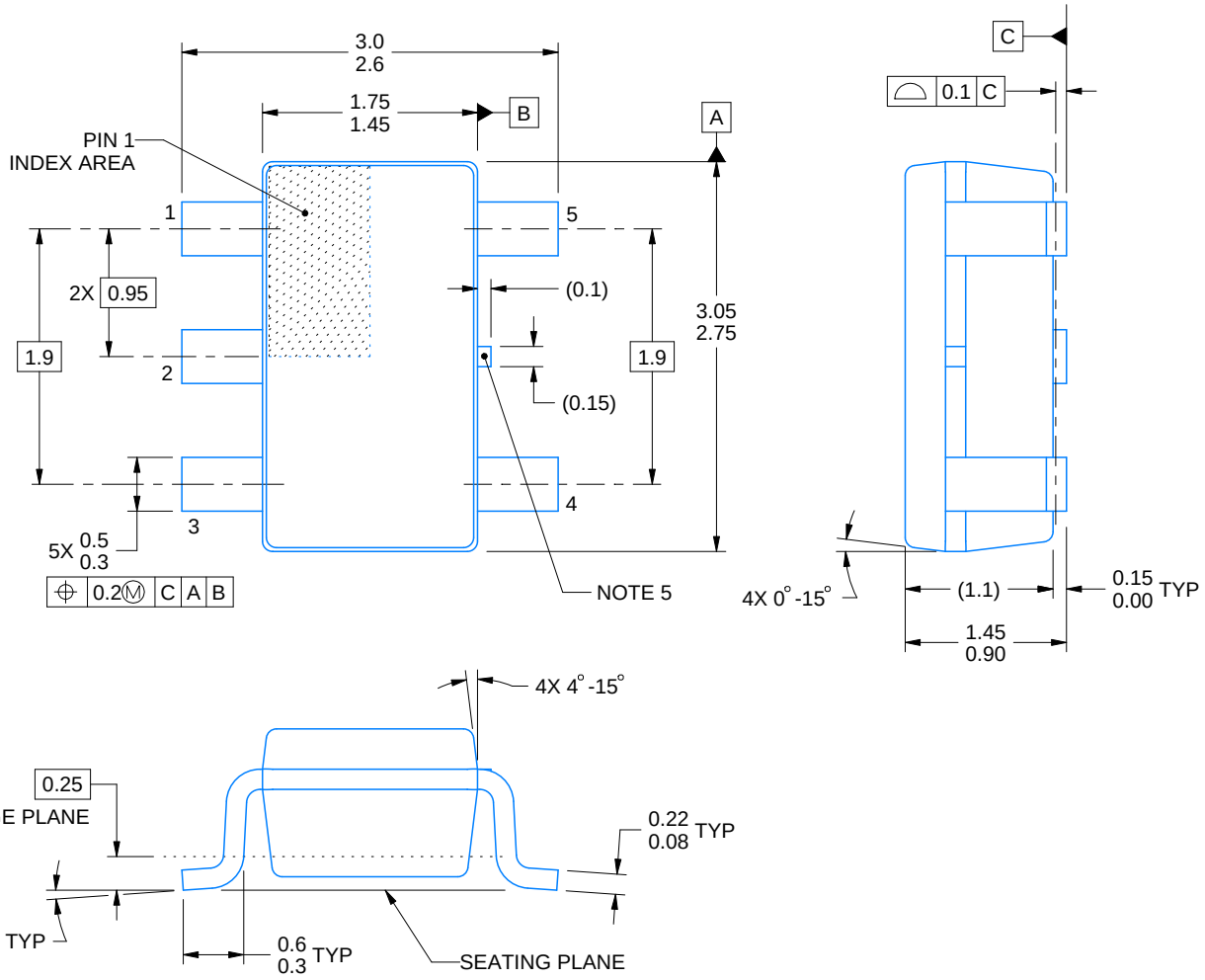
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

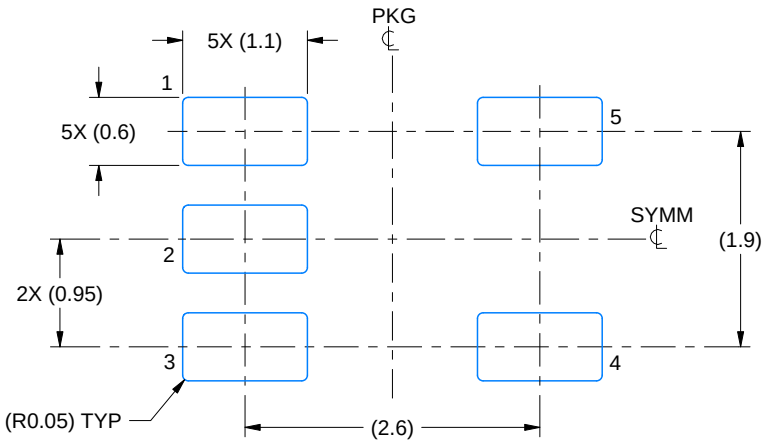
SMALL OUTLINE TRANSISTOR



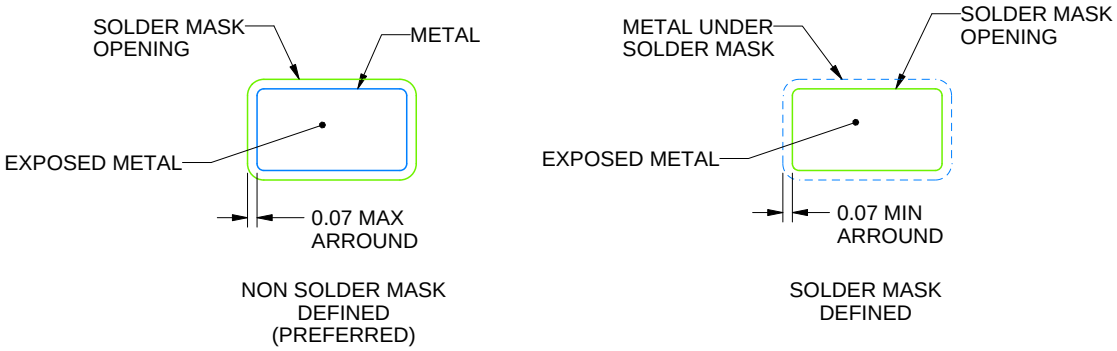
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

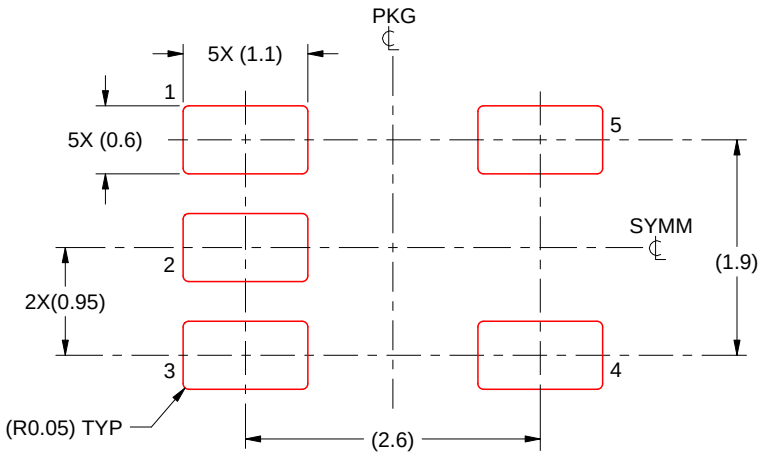


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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