



INA115

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** 50µV max
- **LOW DRIFT:** 0.25µV/°C max
- **LOW INPUT BIAS CURRENT:** 2nA max
- **HIGH COMMON-MODE REJECTION:** 115dB min
- **INPUT OVER-VOLTAGE PROTECTION:** ±40V
- **WIDE SUPPLY RANGE:** ±2.25 TO ±18V
- **LOW QUIESCENT CURRENT:** 3mA max
- **SOL-16 SURFACE-MOUNT PACKAGE**

APPLICATIONS

- SWITCHED-GAIN AMPLIFIER
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

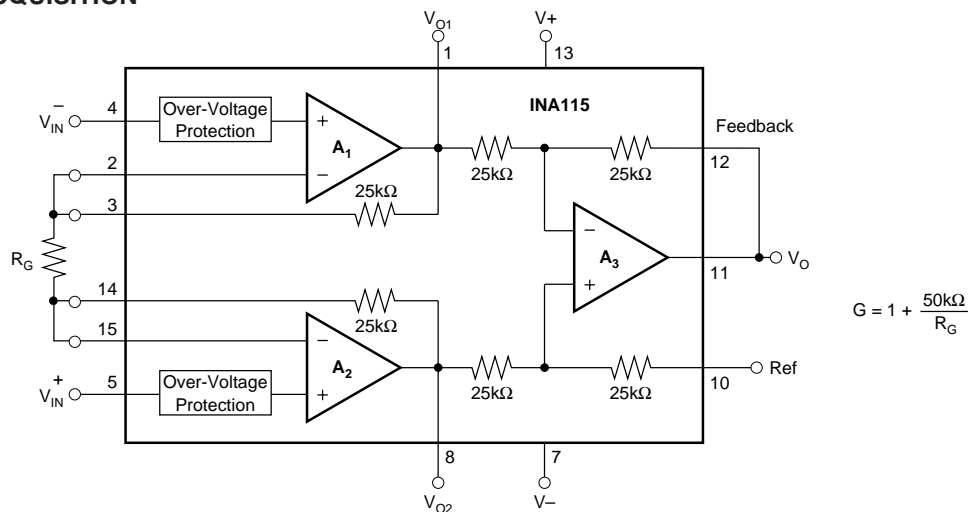
DESCRIPTION

The INA115 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and small size make it ideal for a wide range of applications. Similar to the model INA114, the INA115 provides additional connections to the input op amps, A₁ and A₂, which improve gain accuracy in high gains and are useful in forming switched-gain amplifiers.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA115 is laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G=1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA115 is available in the SOL-16 surface-mount package, specified for the -40°C to +85°C temperature range.



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 Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

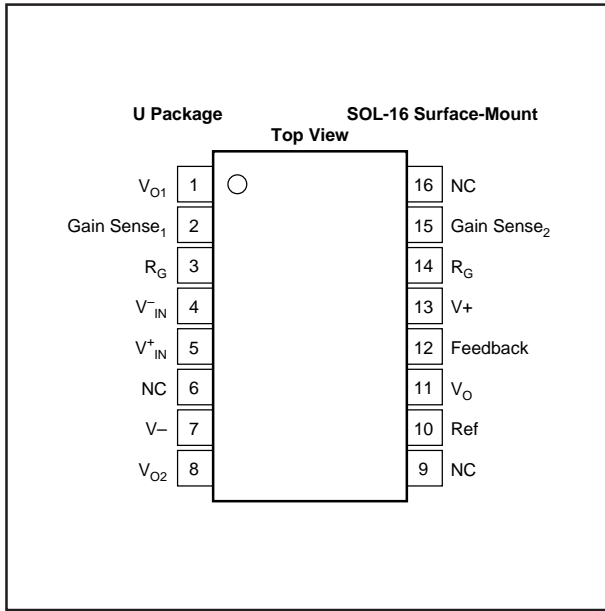
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	INA115BU			INA115AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT Offset Voltage, RTI Initial vs Temperature vs Power Supply Long-Term Stability Impedance, Differential Common-Mode Input Common-Mode Range Safe Input Voltage Common-Mode Rejection	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{MIN}}$ to T_{MAX} $V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$ $V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$ G = 1 G = 10 G = 100 G = 1000		$\pm 10 + 20/\text{G}$ $\pm 0.1 + 0.5/\text{G}$ $0.5 + 2/\text{G}$ $\pm 0.2 + 0.5/\text{G}$ $10^{10} \parallel 6$ $10^{10} \parallel 6$ ± 13.5	$\pm 50 + 100/\text{G}$ $\pm 0.25 + 5/\text{G}$ $3 + 10/\text{G}$		$\pm 25 + 30/\text{G}$ $\pm 0.25 + 5/\text{G}$ * * * * *	$\pm 125 + 500/\text{G}$ $\pm 1 + 10/\text{G}$ * * * * *	μV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{mo}$ $\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$ V V
BIAS CURRENT vs Temperature			± 0.5 ± 8	± 2		* *	± 5	nA $\text{pA}/^\circ\text{C}$
OFFSET CURRENT vs Temperature			± 0.5 ± 8	± 2		* *	± 5	nA $\text{pA}/^\circ\text{C}$
NOISE VOLTAGE, RTI f = 10Hz f = 100Hz f = 1kHz f _B = 0.1Hz to 10Hz Noise Current f=10Hz f=1kHz f _B = 0.1Hz to 10Hz	G = 1000, R _S = 0Ω		15 11 11 0.4			* * * *		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$
GAIN Gain Equation Range of Gain Gain Error Gain vs Temperature 50kΩ Resistance ⁽¹⁾ Nonlinearity	G = 1 G = 10 G = 100 G = 1000 G = 1 G = 1 G = 10 G = 100 G = 1000	1	$1 + (50\text{k}\Omega/R_G)$ ± 0.01 ± 0.02 ± 0.05 ± 0.5 ± 1 ± 2 ± 25 ± 0.0001 ± 0.0005 ± 0.0005 ± 0.002	10000 ± 0.05 ± 0.4 ± 0.5 ± 1 ± 10 ± 100 ± 0.001 ± 0.002 ± 0.002 ± 0.01	*	* * * * * * * * * * * *	* * ± 0.5 ± 0.7 ± 2 ± 10 * ± 0.002 ± 0.004 ± 0.004 ± 0.02	V/V V/V % % % % ppm/°C ppm/°C % of FSR % of FSR % of FSR % of FSR
OUTPUT⁽²⁾ Voltage Load Capacitance Stability Short Circuit Current	I _O = 5mA, T _{MIN} to T _{MAX} V _S = $\pm 11.4\text{V}$, R _L = 2kΩ V _S = $\pm 2.25\text{V}$, R _L = 2kΩ	± 13.5 ± 10 ± 1	± 13.7 ± 10.5 ± 1.5 1000 +20/-15			* * *		V V V pF mA
FREQUENCY RESPONSE Bandwidth, -3dB Slew Rate Settling Time, 0.01% Overload Recovery	G = 1 G = 10 G = 100 G = 1000 V _O = $\pm 10\text{V}$, G = 10 G = 1 G = 10 G = 100 G = 1000 50% Overdrive		1 100 10 1 0.6 18 20 120 1100 20			* * * * * * * * * *		MHz kHz kHz kHz V/μs μs μs μs μs μs
POWER SUPPLY Voltage Range Current	V _{IN} = 0V	± 2.25	± 15 ± 2.2	± 18 ± 3	*	* *	* *	V mA
TEMPERATURE RANGE Specification Operating θ _{JA}		-40 -40		+85 +125	* *		* *	°C °C °C/W

* Specification same as INA115BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) Output specifications are for output amplifier, A₃. A₁ and A₂ provide the same output voltage swing but have less output current drive. A₁ and A₂ can drive external loads of 25kΩ || 200pF.

PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE/ORDERING INFORMATION

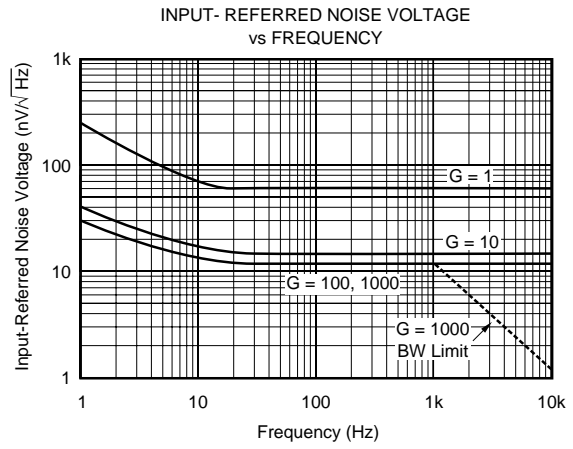
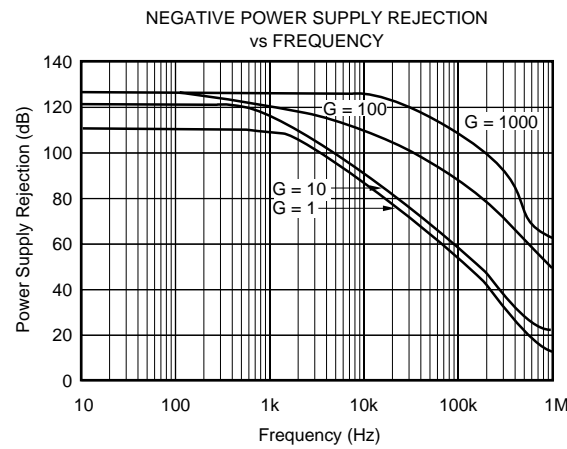
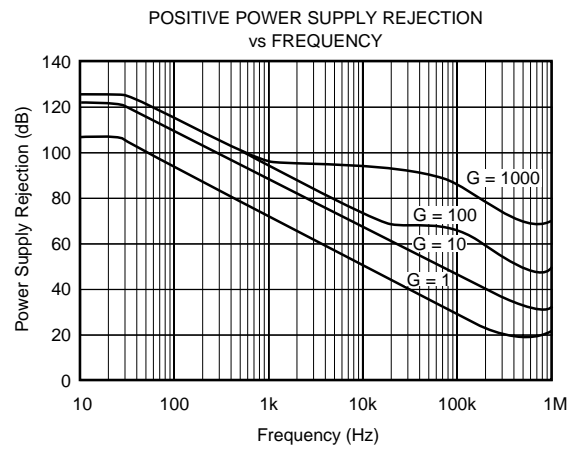
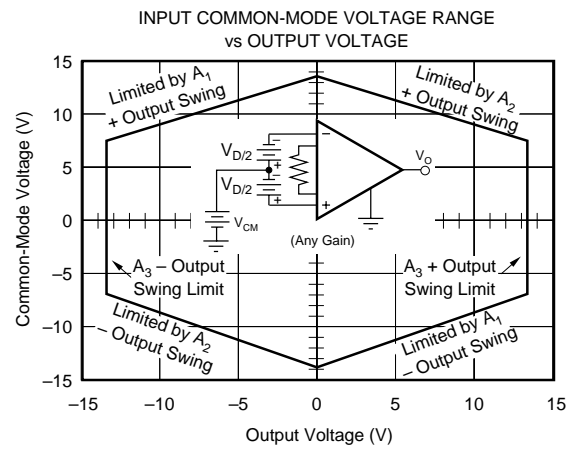
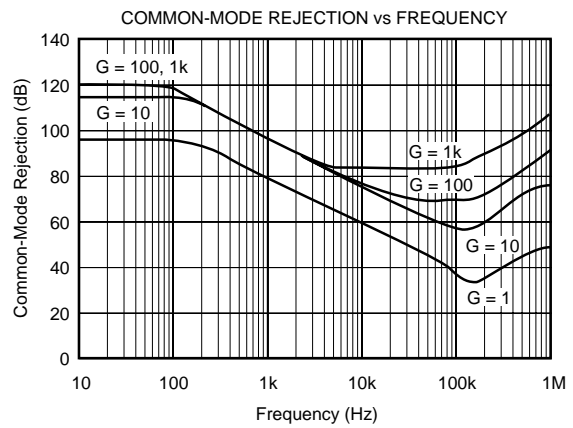
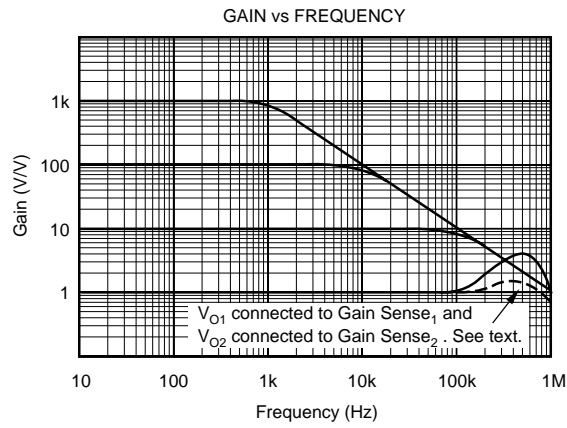
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
INA115AU	SOL-16 Surface-Mount	211	-40°C to +85°C
INA115BU	SOL-16 Surface-Mount	211	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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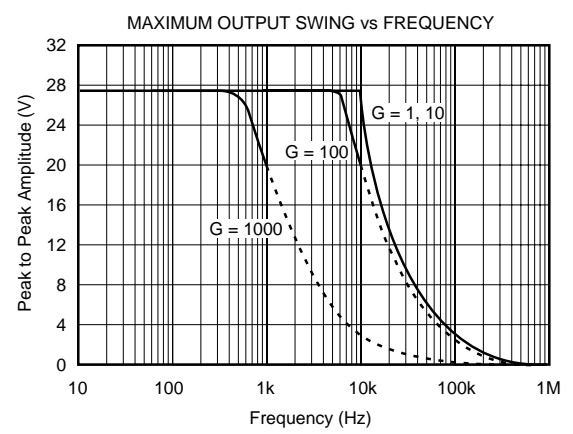
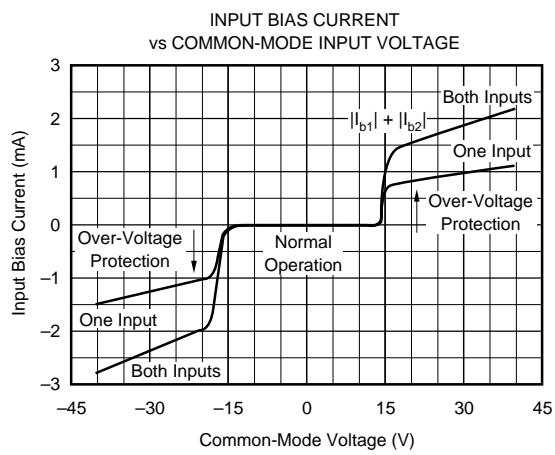
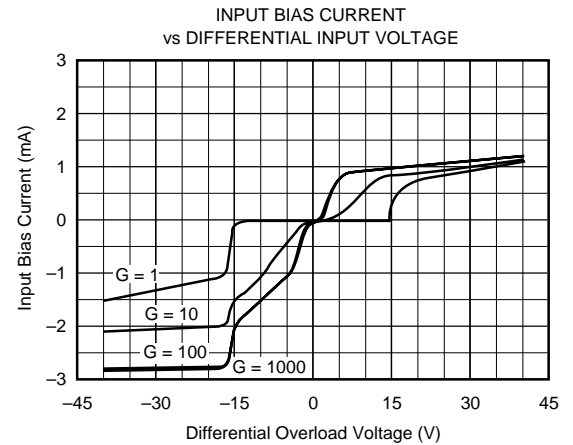
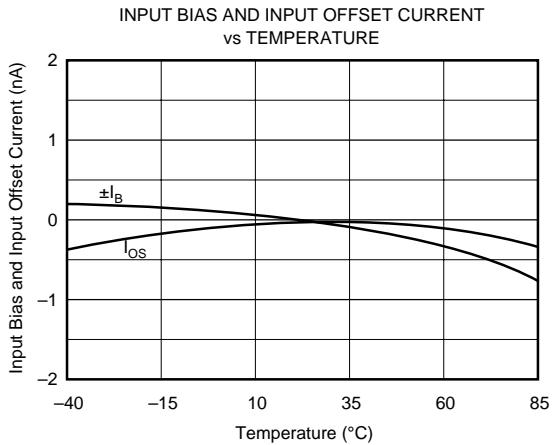
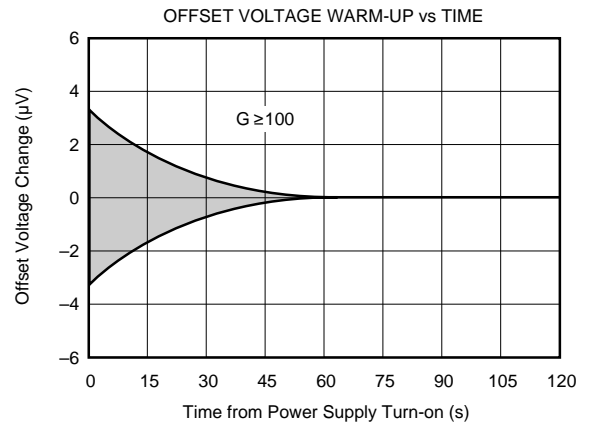
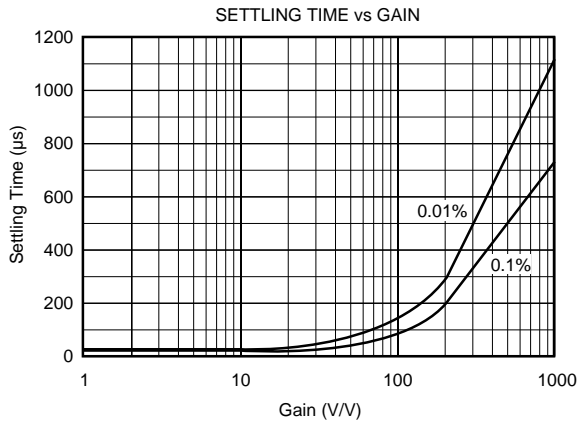
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



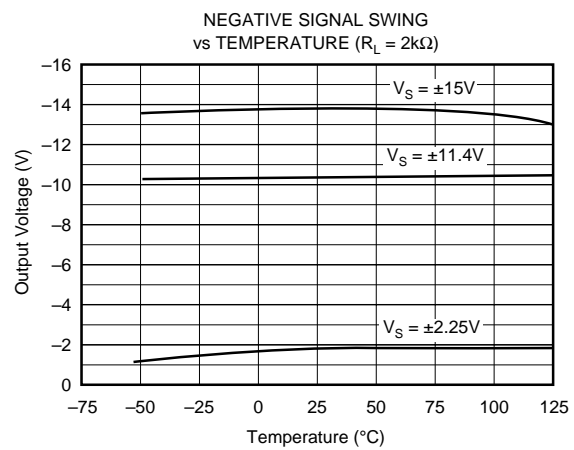
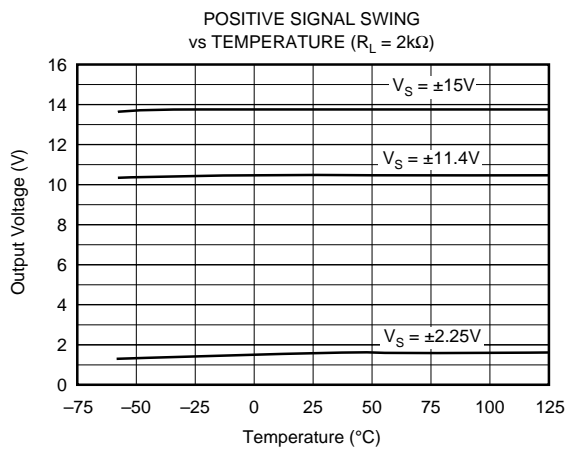
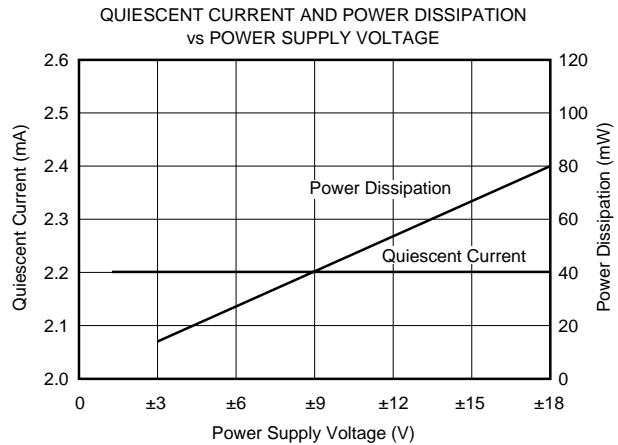
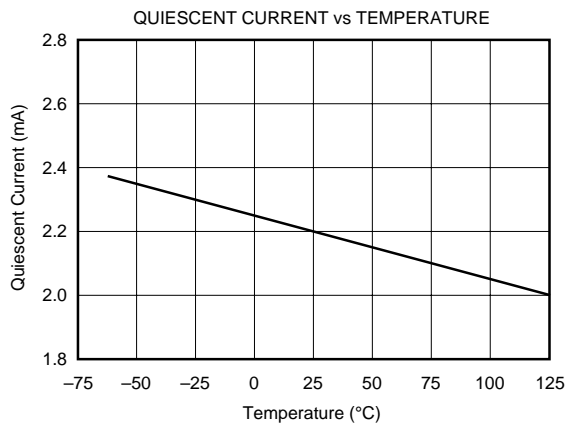
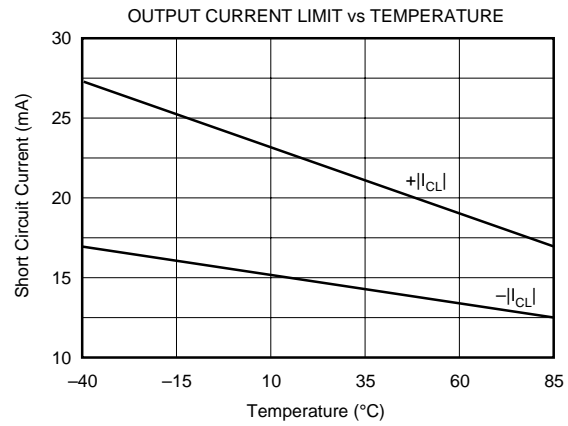
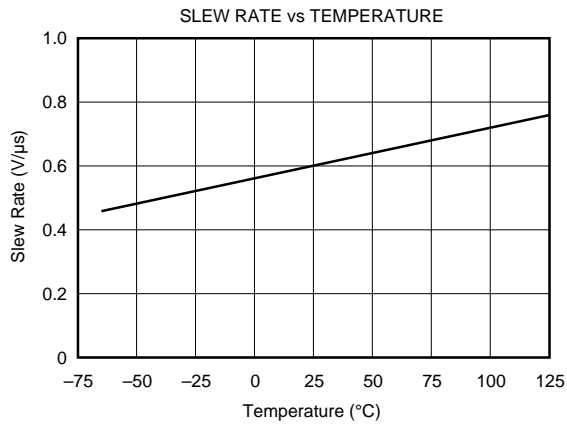
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

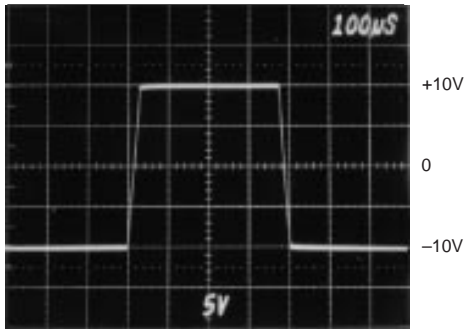
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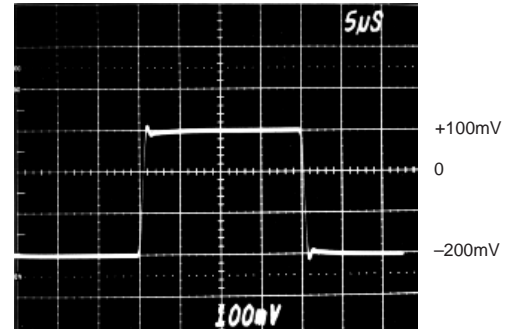
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

LARGE SIGNAL RESPONSE, $G = 1$

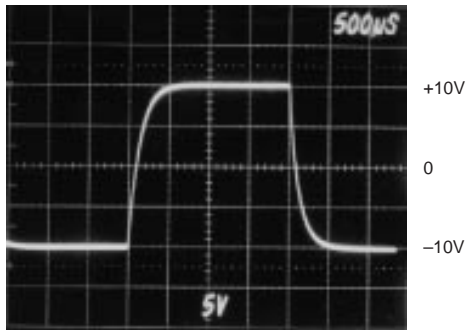


SMALL SIGNAL RESPONSE, $G = 1$

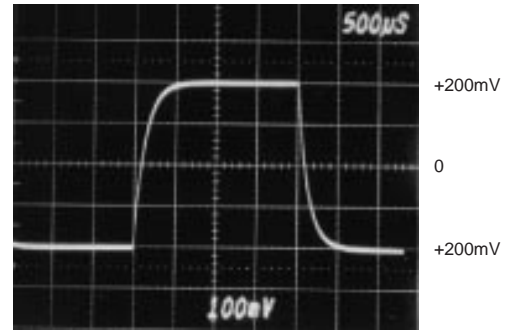


V_{O1} connected to Gain Sense₁, and
 V_{O2} connected to Gain Sense₂

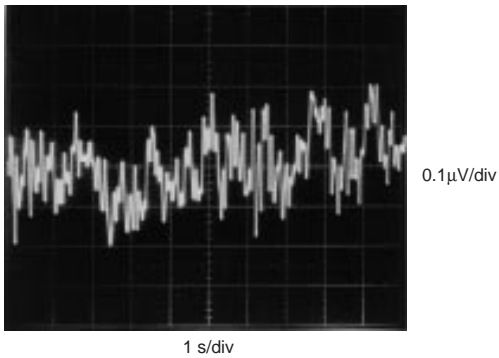
LARGE SIGNAL RESPONSE, $G = 1000$



SMALL SIGNAL RESPONSE, $G = 1000$



INPUT-REFERRED NOISE, 0.1 to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA115. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G=1).

The INA115 has a separate output sense feedback connection (pin 12). Pin 12 must be connected (normally to the output terminal, pin 11) for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

SETTING THE GAIN

Gain of the INA115 is set by connecting a single external resistor, R_G :

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

For $G=1$, no resistor is required, but connect pins 2-3 and connect pins 14-15. Gain peaking in $G=1$ can be reduced by shorting the internal 25kΩ feedback resistors (see typical performance curve Gain vs Frequency). To do this, connect pins 1-2-3 and connect pins 8-14-15.

The 50kΩ term in equation 1 comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA115.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain error and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. The “force and sense” type connections illustrated in Figure 1 help reduce the effect of interconnection resistance.

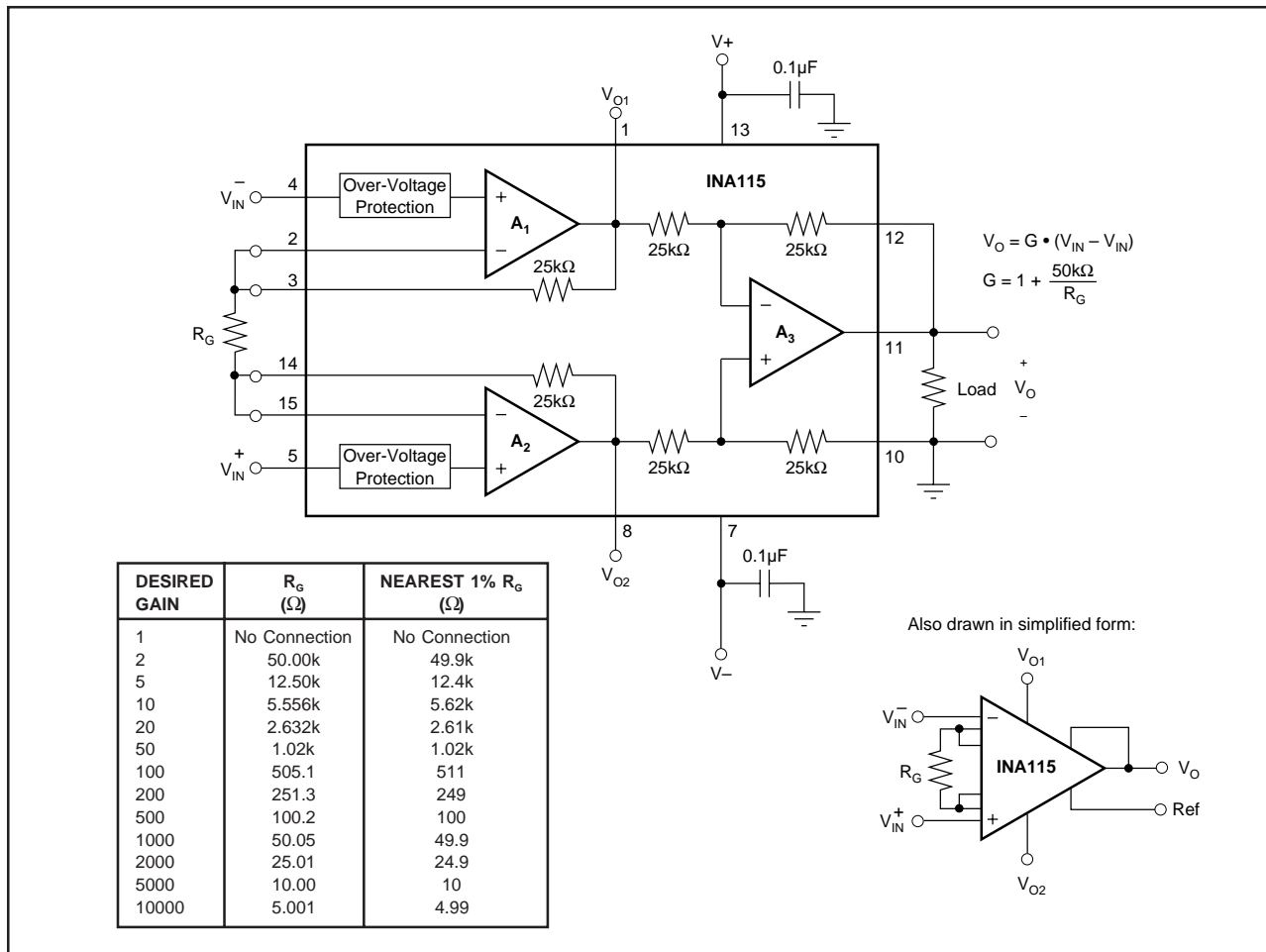


FIGURE 1. Basic Connections.

SWITCHED GAIN

Figure 2 shows a circuit for digital selection of four gains. Multiplexer “on” resistance does not significantly affect gain. The resistor values required for some commonly used gain steps are shown. This circuit uses the internal 25kΩ feedback resistors, so the resistor values shown cannot be scaled to a different impedance level.

Figure 3 shows an alternative switchable gain configuration. This circuit does not use the internal 25kΩ feedback resistors, so the nominal values shown can be scaled to other impedance levels. This circuit is ideal for use with a precision resistor network to achieve excellent gain accuracy and lowest gain drift.

NOISE PERFORMANCE

The INA115 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA115 is approximately 0.4μVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of “low noise” chopper-stabilized amplifiers.

OFFSET TRIMMING

The INA115 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 4 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA115 is extremely high—approximately 10¹⁰Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA115 is to operate properly. Figure 5 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA115 and the input amplifiers will saturate. If the differential source resistance is low, a bias current return path can be connected to one input (see thermocouple example in Figure 5). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

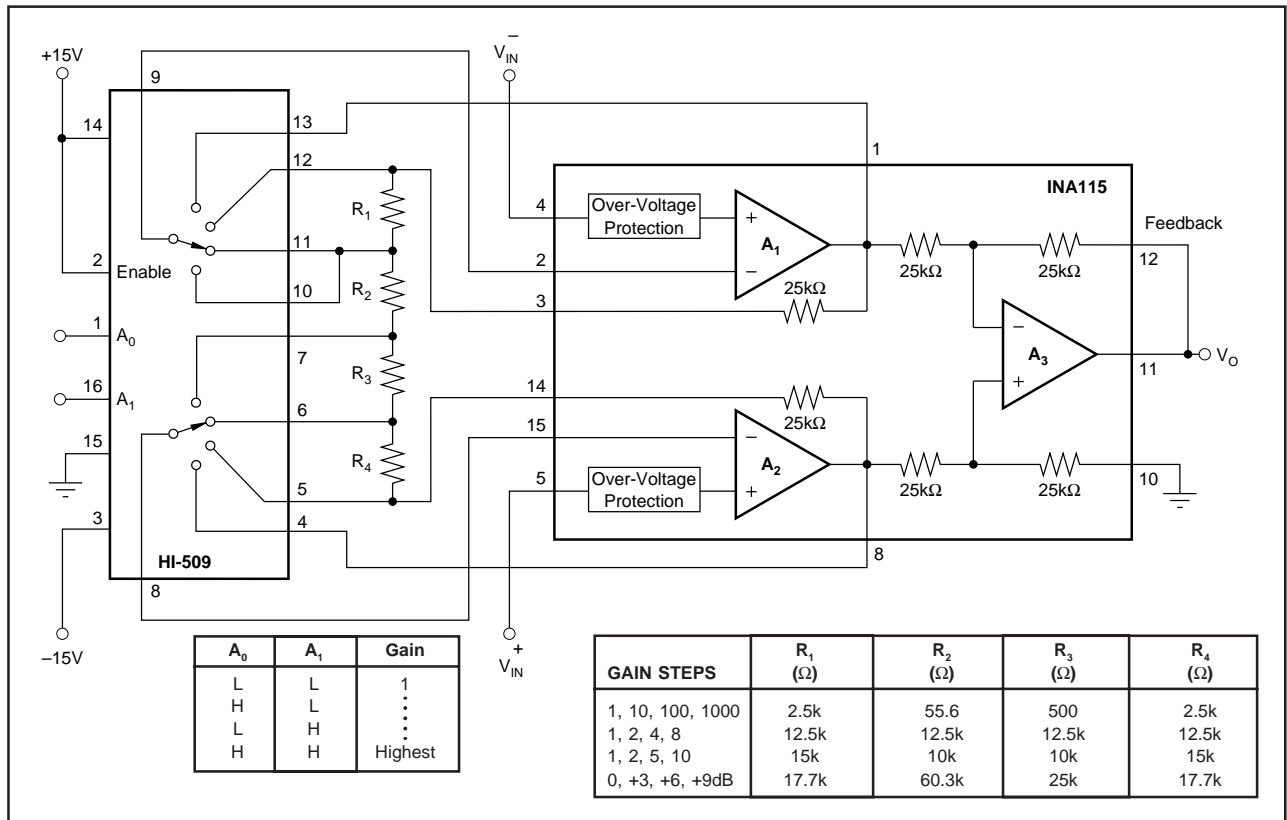


FIGURE 2. Switched-Gain Instrumentation Amplifier (minimum components).

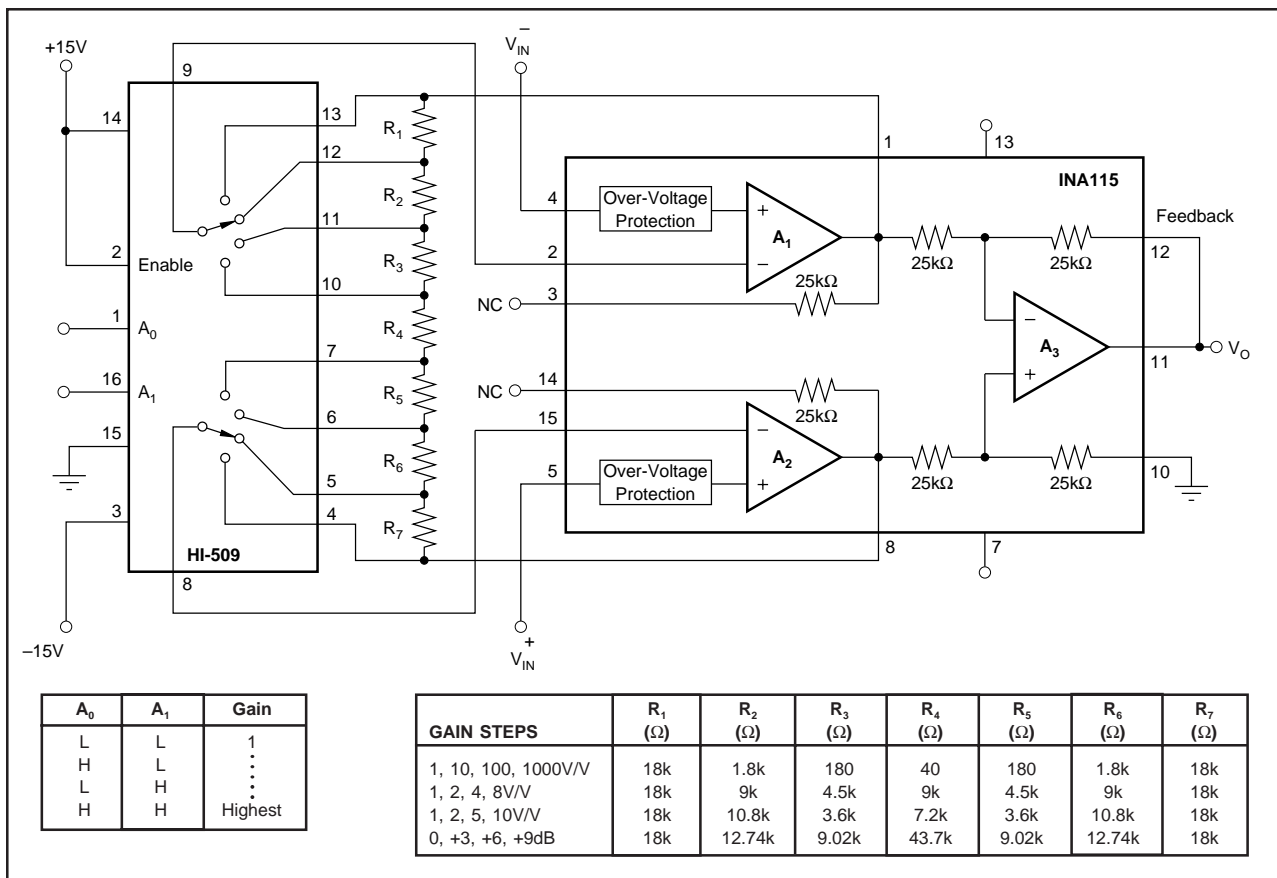


FIGURE 3. Switched-Gain Instrumentation Amplifier (improved gain drift).

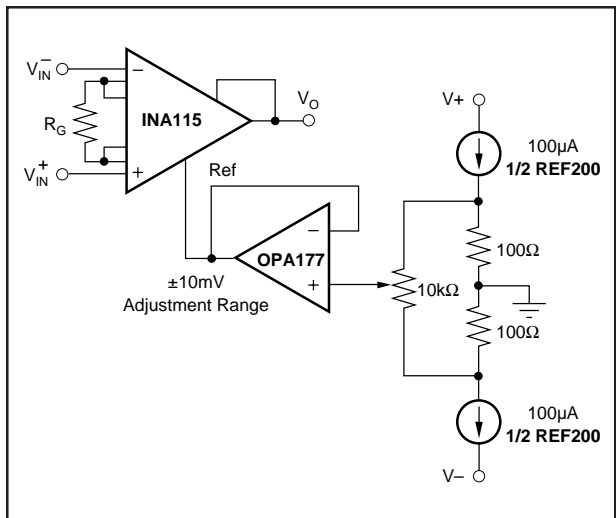


FIGURE 4. Optional Trimming of Output Offset Voltage.

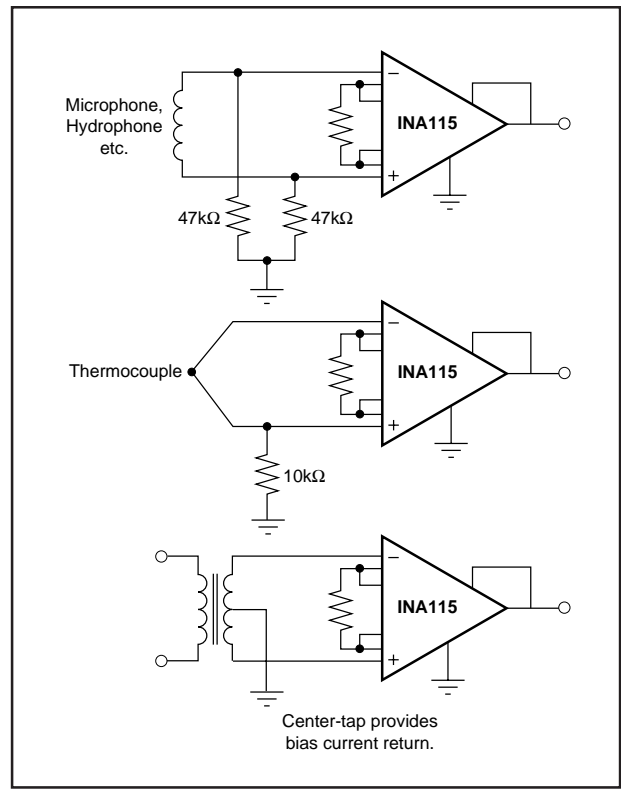


FIGURE 5. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA115 is approximately $\pm 13.75\text{V}$ (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The common-mode range is related to the output voltage of the complete amplifier—see performance curve “Input Common-Mode Range vs Output Voltage.”

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 6 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of the input amplifiers, A_1 and A_2 is the same as the output amplifier, A_3 . For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA115 in a lower gain (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the INA115 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of $+20\text{V}$ on one input and $+40\text{V}$ on the other input will obviously exceed the linear

common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA115 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA115 are individually protected for voltages up to $\pm 40\text{V}$. For example, a condition of -40V on one input and $+40\text{V}$ on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input current limit behavior. The inputs are protected even if the power supply voltage is zero.

OTHER APPLICATIONS

See the INA114 data sheet for other applications circuits of general interest.

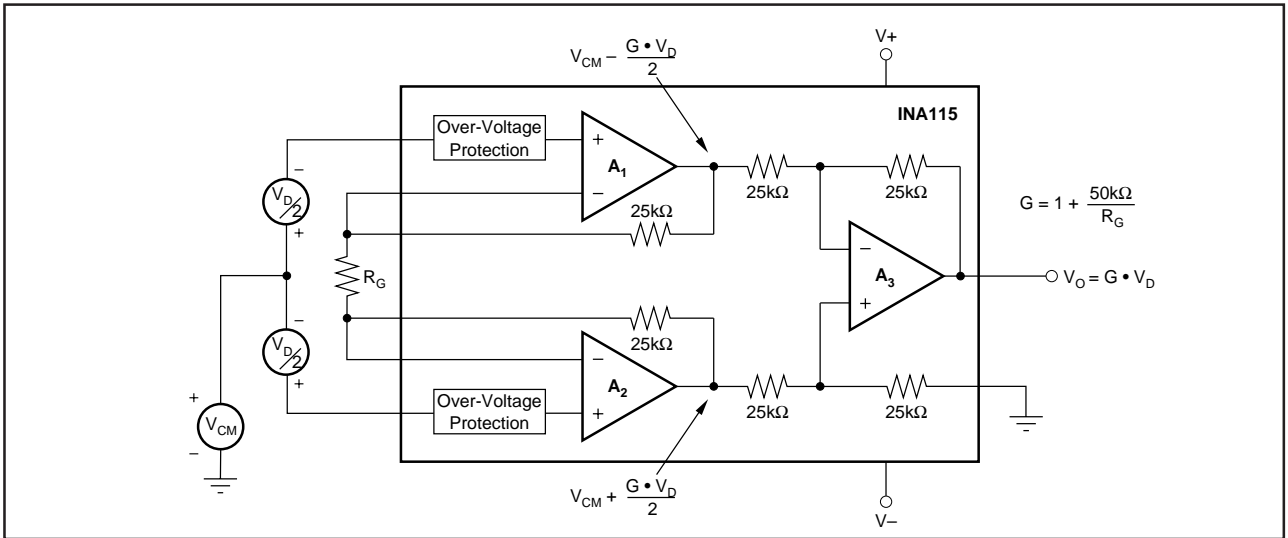


FIGURE 6. Voltage Swing of A_1 and A_2 .

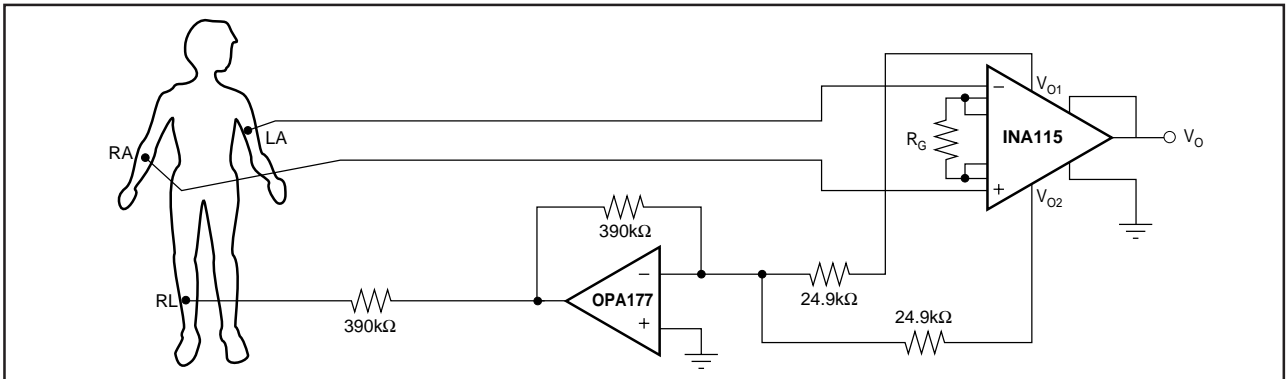


FIGURE 7. ECG Amplifier with Right Leg Drive.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA115AU	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA115AU	Samples
INA115AU/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR		INA115AU	Samples
INA115BU	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR		INA115BU	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA115AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA115AU/1K	SOIC	DW	16	1000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA115AU	DW	SOIC	16	40	507	12.83	5080	6.6
INA115BU	DW	SOIC	16	40	507	12.83	5080	6.6

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