

ESD2CANFD24 24V、車載ネットワーク用 2 チャネル ESD 保護ダイオード

1 特長

- IEC 61000-4-2 レベル 4 ESD 保護
 - 接触放電 $\pm 25\text{kV}$
 - 空中放電 $\pm 25\text{kV}$
- IEC 61000-4-5 に従ってテスト済み
- 24V の動作電圧
- 双方向 ESD 保護
- 1 つの部品で完全な ESD 保護機能を実現できる 2 チャネル・デバイス
- 下流の部品を保護する低いクランピング電圧
- I/O 容量: 2.5pF (標準値)
- SOT-23 (DBZ): 小型、標準、共通フットプリント
- 自動光学検査 (AOI) に適したリード付きパッケージ

2 アプリケーション

- 産業用制御ネットワーク:
 - DeviceNet IEC 62026-3
 - CANopen – CiA 301/302-2, EN 50325-4

3 概要

ESD2CANFD24 は、CAN (Controller Area Network) インターフェイス保護用の双方向 ESD 保護ダイオードです。ESD2CANFD24 は、IEC 61000-4-2 規格 (接触 $\pm 25\text{kV}$ 、気中 $\pm 25\text{kV}$) に規定された最大レベルを超える接触 ESD 衝撃を放散できるように定格が規定されています。低い動的抵抗および低いクランピング電圧により、過渡現象に対してシステム・レベルの保護を実現します。システムでは、安全アプリケーションに対して高レベルの堅牢性と信頼性が求められるので、この保護機能は重要です。

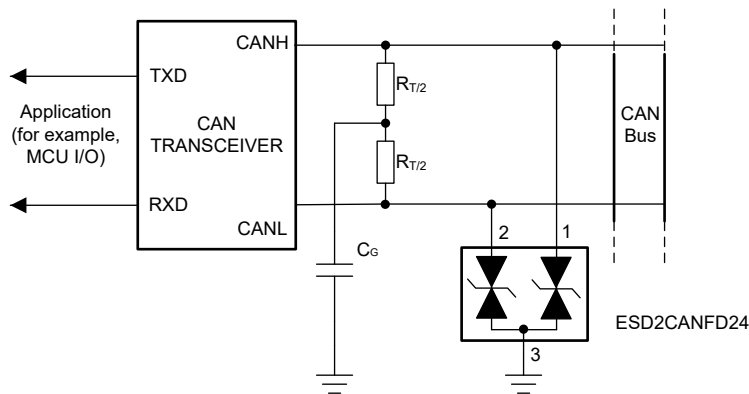
このデバイスはチャンネルごとの IO 容量が低く、静電放電 (ESD) とその他の過渡現象に起因する損傷から保護されるように 2 つの CAN バス・ライン (CANH、CANL) に適合したピン配置を備えています。また、ESD2CANFD24 の 2.5pF (標準値) 以下のライン容量は、最大 10Mbps のデータ・レートをサポートできる CAN、CANFD、CAN SiC、CAN-XL アプリケーションに適しています。

ESD2CANFD24 は、リード付きパッケージで供給され、フロー・スルー配線が容易になっています。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
ESD2CANFD24	DBZ (SOT-23, 3)	2.92mm × 1.30mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ESD2CANFD24 の代表的なアプリケーション



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4 Revision History

DATE	REVISION	NOTES
November 2022	*	Initial Release

5 Pin Configuration and Functions

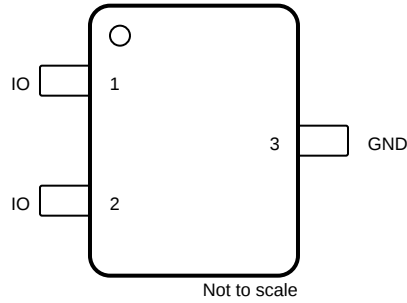


图 5-1. DBZ Package, 3-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

6 Specifications

6.1 絶対最大定格

自由気流での動作温度範囲内 (特に記述のない限り) ⁽¹⁾

パラメータ		デバイス	最小値	最大値	単位
P _{PP}	25°Cでの IEC 61000-4-5 の電力 (t _p – 8/20μs)	ESD2CANFD24		133	W
I _{PP}	25°Cでの IEC 61000-4-5 の電流 (t _p – 8/20μs)			3.5	A
T _A	自由気流での動作温度		-55	150	°C
T _J	接合部温度		-55	150	
T _{stg}	保存温度		-65	155	

- (1) 絶対最大定格の範囲外の動作は、デバイスの永続的な損傷の原因となる可能性があります。絶対最大定格は、この値の条件においても、または「推奨動作条件」に示された値を超えるいかなる条件においても、デバイスが正しく動作することを暗に示すものではありません。絶対最大定格の範囲内であっても、推奨動作条件の範囲外で使用した場合、本デバイスは完全に機能するとは限らず、このことが本デバイスの信頼性、機能、性能に影響を及ぼし、本デバイスの寿命を縮める可能性があります。

6.2 ESD 定格 - JEDEC 仕様

PARAMETER		TEST CONDITION	値	単位
V _(ESD)	静電気放電	人体モデル (HBM)、ANSI/ESDA/JEDEC JS-001 に準拠 ⁽¹⁾	±2500	V
		デバイス帯電モデル (CDM)、JEDEC 仕様 JS-002 に準拠 ⁽²⁾	±1000	

- (1) JEDEC のドキュメント JEP155 には、500V HBM であれば標準的な ESD 管理プロセスで安全な製造が可能であると記載されています。
 (2) JEDEC のドキュメント JEP157 には、250V CDM であれば標準的な ESD 管理プロセスで安全な製造が可能であると記載されています。

6.3 ESD 定格 - IEC 仕様

T_A = 25°C (特に記述のない限り)

パラメータ		テスト条件	デバイス	値	単位
V _(ESD)	静電気放電	IEC 61000-4-2 接触放電、すべてのピン	ESD2CANFD24	±25000	V
		IEC 61000-4-2 空中放電、すべてのピン		±25000	

6.4 推奨動作条件

自由気流での動作温度範囲内 (特に記述のない限り)

パラメータ		最小値	公称値	最大値	単位
V _{IN}	入力電圧	-24		24	V
T _A	自由気流での動作温度	-55		150	°C

6.5 熱に関する情報

熱評価基準 ⁽¹⁾		ESD2CANFD24		単位
		DBZ (SOT-23)		
		3 ピン		
R _{θJA}	接合部から周囲への熱抵抗	316.3		°C/W
R _{θJC(top)}	接合部からケース (上面) への熱抵抗	170.7		°C/W
R _{θJB}	接合部から基板への熱抵抗	156.2		°C/W
Ψ _{JT}	接合部から上部までの特性評価パラメータ	45.9		°C/W
Ψ _{JB}	接合部から基板までの特性評価パラメータ	155.1		°C/W
R _{θJC(bot)}	接合部からケース (底面) への熱抵抗	N/A		°C/W

- (1) 従来および最新の熱評価基準の詳細については、『[半導体および IC パッケージの熱評価基準](#)』アプリケーション・レポートを参照してください。

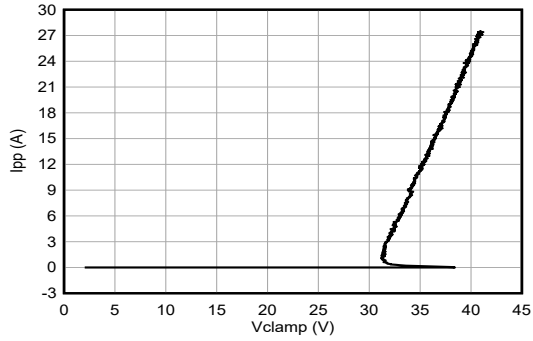
6.6 電気的特性

$T_A = 25^\circ\text{C}$ (特に記述のない限り)⁽¹⁾

パラメータ		テスト条件	デバイス	最小値	代表値	最大値	単位
V_{RWM}	逆スタンバイオフ電圧		ESD2CANFD24	-24		24	V
V_{BRF}	ブレイクダウン電圧 ⁽²⁾	$I_{IO} = 10\text{mA}$, IO から GND へ	ESD2CANFD24	25.5		35.5	V
V_{BRR}	ブレイクダウン電圧 ⁽²⁾	$I_{IO} = -10\text{mA}$, IO から GND へ	ESD2CANFD24	-35.5		-25.5	V
V_{CLAMP}	クランプ電圧 ⁽³⁾	$I_{PP} = 3.5\text{A}$, $t_p = 8/20\mu\text{s}$, IO から GND へ	ESD2CANFD24		37		V
V_{CLAMP}	クランプ電圧 ⁽⁴⁾	$I_{PP} = 16\text{A}$, TLP, IO から GND または GND から IO へ	ESD2CANFD24		36		V
I_{LEAK}	リーク電流	$V_{IO} = \pm 24\text{V}$, IO から GND へ	ESD2CANFD24	-50	5	50	nA
R_{DYN}	動的抵抗 ⁽⁴⁾	IO から GND または GND から IO へ	ESD2CANFD24		0.45		Ω
C_L	ライン容量 ⁽⁵⁾	$V_{IO} = 0\text{V}$, $f = 1\text{MHz}$, $V_{pp} = 30\text{mV}$	ESD2CANFD24		2.5	4.2	pF
V_{Hold}	スナップバック後の保持電圧	TLP	ESD2CANFD24		30		V

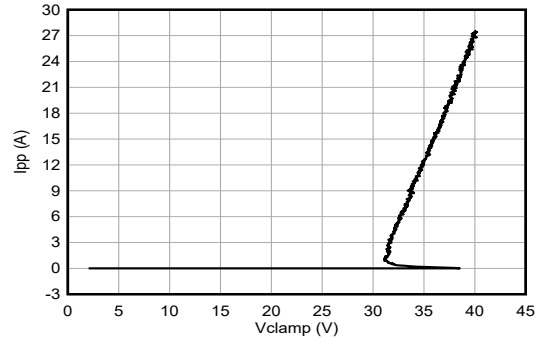
- (1) 各 IO チャンネルで測定を行います
- (2) V_{BRF} と V_{BRR} は、デバイスがスナップバック状態にラッチする前に、それぞれ正方向と負方向に $\pm 10\text{mA}$ を印加したときの電圧として定義されます
- (3) IEC 61000-4-5 に従い、 $8/20\mu\text{s}$ の指数減衰波形でデバイスにストレスを加えました
- (4) 非反復電流パルス、伝送ライン・パルス (TLP)、方形パルス、ANSI/ESD STM5.5.1-2008
- (5) 各チャンネルで IO から GND への測定

6.7 Typical Characteristics – ESD2CANFD24



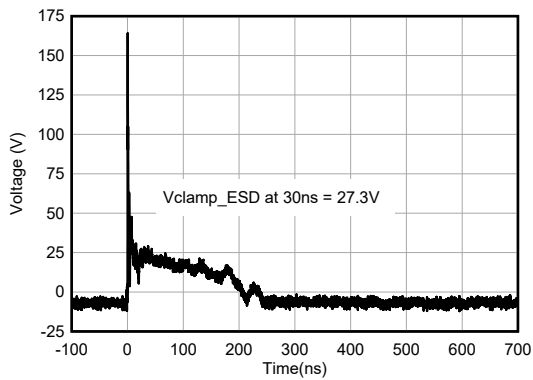
tp = 100 ns, Transmission Line Pulse (TLP)

6-1. Positive TLP Curve

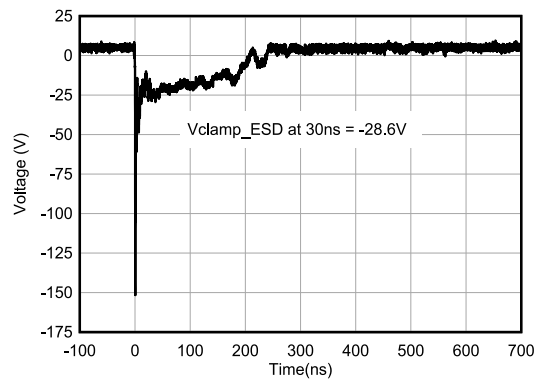


tp = 100 ns, Transmission Line Pulse (TLP)

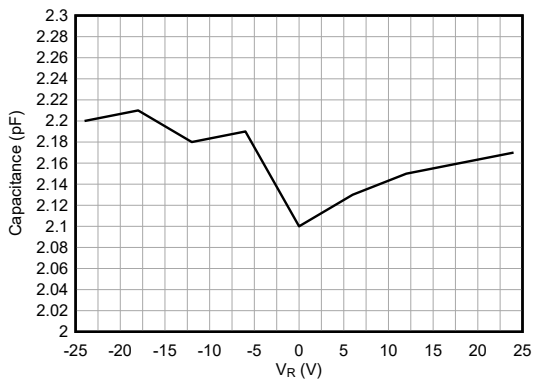
6-2. Negative TLP Curve



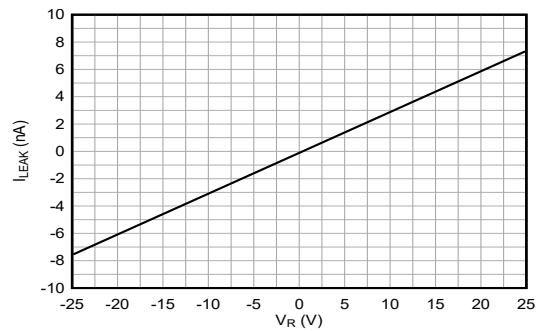
6-3. +8-kV Clamped IEC Waveform



6-4. -8-kV Clamped IEC Waveform



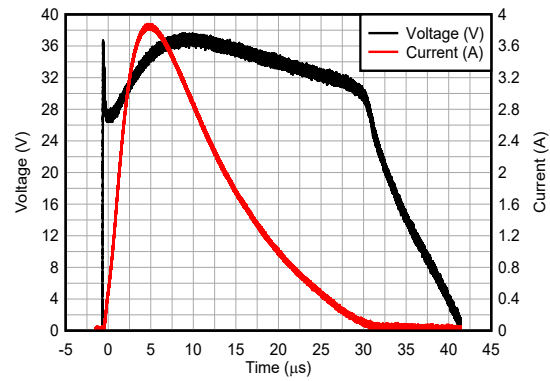
6-5. Capacitance vs. Bias Voltage



TA = 150 °C
 ILEAK is less than 1 nA at -55 °C and 25 °C.

6-6. Leakage Current vs. Bias Voltage Across Temperature

6.7 Typical Characteristics – ESD2CANFD24 (continued)



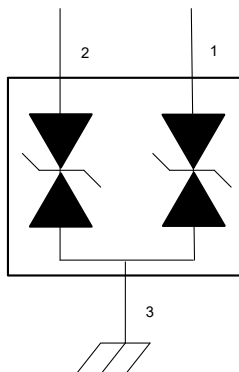
⊠ 6-7. 8/20 μs Surge Response at 3.5 A

7 Detailed Description

7.1 Overview

The ESD2CANFD24 is a dual-channel ESD TVS diode in SOT-23 leaded package which is convenient for automatic optical inspection. This product offers IEC 61000-4-2 ± 25 -kV air-gap, ± 25 -kV contact ESD protection, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support. The 2.5 pF (typical) or less line capacitance of this ESD protection diode is suitable for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 10 Mbps. A typical application for this product is ESD circuit protection for CAN transceivers.

7.2 Functional Block Diagram



7.3 Feature Description

The ESD2CANFD24 is a bidirectional TVS with a high ESD protection level. This device protects the circuit from ESD strikes up to ± 25 -kV contact and ± 25 -kV air-gap specified in the IEC 61000-4-2 standard. The device can also handle up to 3.5 A surge current (IEC 61000-4-5 8/20 μ s). The I/O capacitance of 2.5-pF (typical) supports a data rate up to 10 Mbps. This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 37 V when the device is taking 3.5 A transient surge current. The breakdown is bidirectional so this protection device is a good fit for CAN which is a differential signal. Low leakage allows the diode to conserve power when working below the V_{RWM} . The temperature range of -55°C to $+150^{\circ}\text{C}$ makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 package is good for applications requiring automatic optical inspection (AOI).

7.3.1 Temperature Range

This device is qualified to operate from -55°C to $+150^{\circ}\text{C}$.

7.3.2 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events of at least ± 25 -kV contact and ± 25 -kV air-gap in the leaded SOT-23 package according to the IEC 61000-4-2 standard. An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 3.5 A (8/20 μ s waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between the I/O pins is 2.5 pF (typical) or less. This capacitance supports data rates for CAN, CANFD, CAN SiC, and CAN-XL up to 10 Mbps.

7.3.5 Dynamic Resistance

The IO pins feature an ESD clamp that has a low R_{DYN} of 0.45 Ω (Pin 1 or Pin 2 to Pin 3) and 0.45 Ω (Pin 3 to Pin 1 or Pin 2) or less which prevents system damage during ESD events.

7.3.6 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of ± 25.5 V. This protects sensitive equipment from surges above the reverse standoff voltage of ± 24 V.

7.3.7 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of ± 50 nA (maximum) with a bias of ± 24 V.

7.3.8 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 37 V ($I_{PP} = 3.5$ A) and 36 V ($I_{PP} = 16$ A for TLP).

7.3.9 Industry Standard Leaded Packages

This device features an industry standard SOT-23 (DBZ) leaded package for automatic optical inspection (AOI).

7.4 Device Functional Modes

The ESD2CANFD24 is a dual channel passive clamp that has low leakage during normal operation when the voltage between pin 1 or pin 2 and pin 3 is below V_{RWM} , and activates when the voltage between pin 1 or pin 2 and pin 3 goes above V_{BR} . During IEC 61000-4-2 ESD events, transient voltages as high as ± 25 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD} , the device reverts back to the low leakage passive state.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD2CANFD24 is a dual channel TVS diode which is used to provide a path to ground for dissipating ESD events on differential CAN signal lines. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

8.2 Typical Application

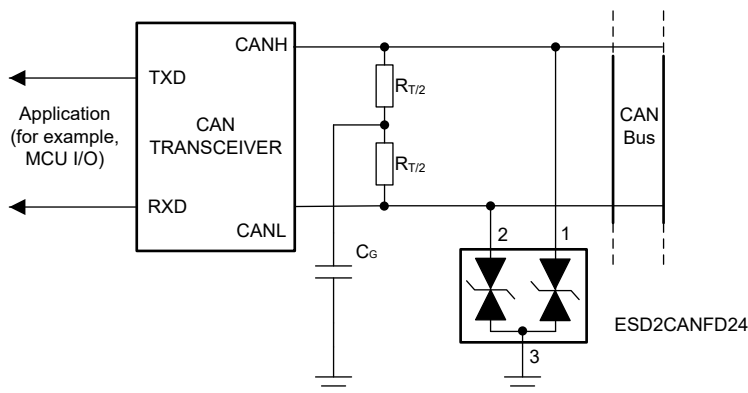


图 8-1. ESD2CANFD24 Typical Application

8.2.1 Design Requirements

For this design example, the ESD2CANFD24 is used to provide ESD protection for a CAN transceiver. 表 8-1 lists the known design parameters for this application.

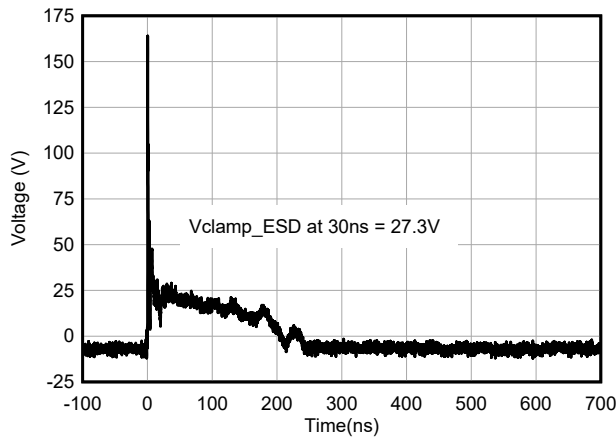
表 8-1. Design Parameters for the ESD2CANFD24 Typical Application

Design Parameter	Value
Diode configuration	Bidirectional
V_{IO} differential signal range	$> \pm 1.5$ V
V_{RWM}	± 24 V
Data rate	Up to 10 Mbps
RT/2	60 Ω

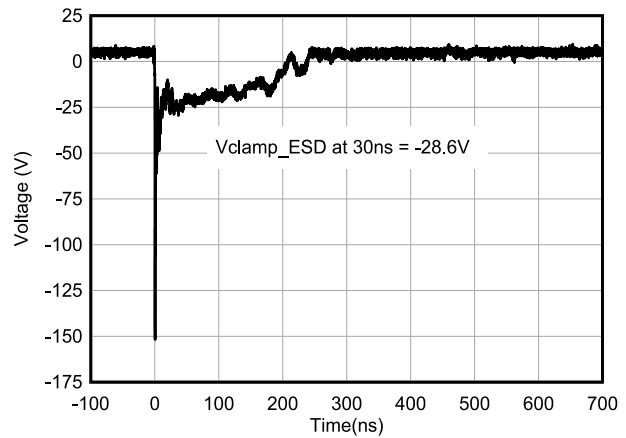
8.2.2 Detailed Design Procedure

The ESD2CANFD24 has a V_{RWM} of ± 24 V. The bidirectional characteristic enables the signal integrity of the differential CAN lines to not be impacted by the diode. The low capacitance of 2.5 pF (typical) or less enables data rates up to 10 Mbps, which allows the designer to meet the requirements for CAN, CANFD, CAN SiC, and CAN-XL. The 60 Ω split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

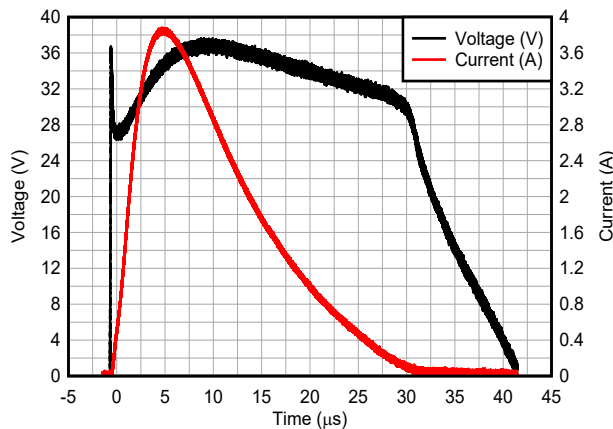
8.2.3 Application Curves



8-2. +8-kV Clamped IEC Waveform



8-3. -8-kV Clamped IEC Waveform



8-4. 8/20 μ s Surge Response at 3.5 A

9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, therefore there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

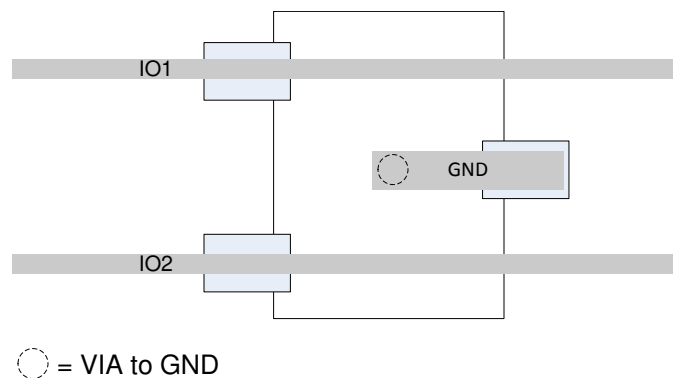
10 Layout

10.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

This example is typical of a dual channel differential data pair application, such as CAN.



 10-1. Routing with DBZ Package

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection data sheet](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD2CANFD24DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-50 to 150	2QO8	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ESD2CANFD24 :

- Automotive : [ESD2CANFD24-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

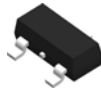

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD2CANFD24DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD2CANFD24DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

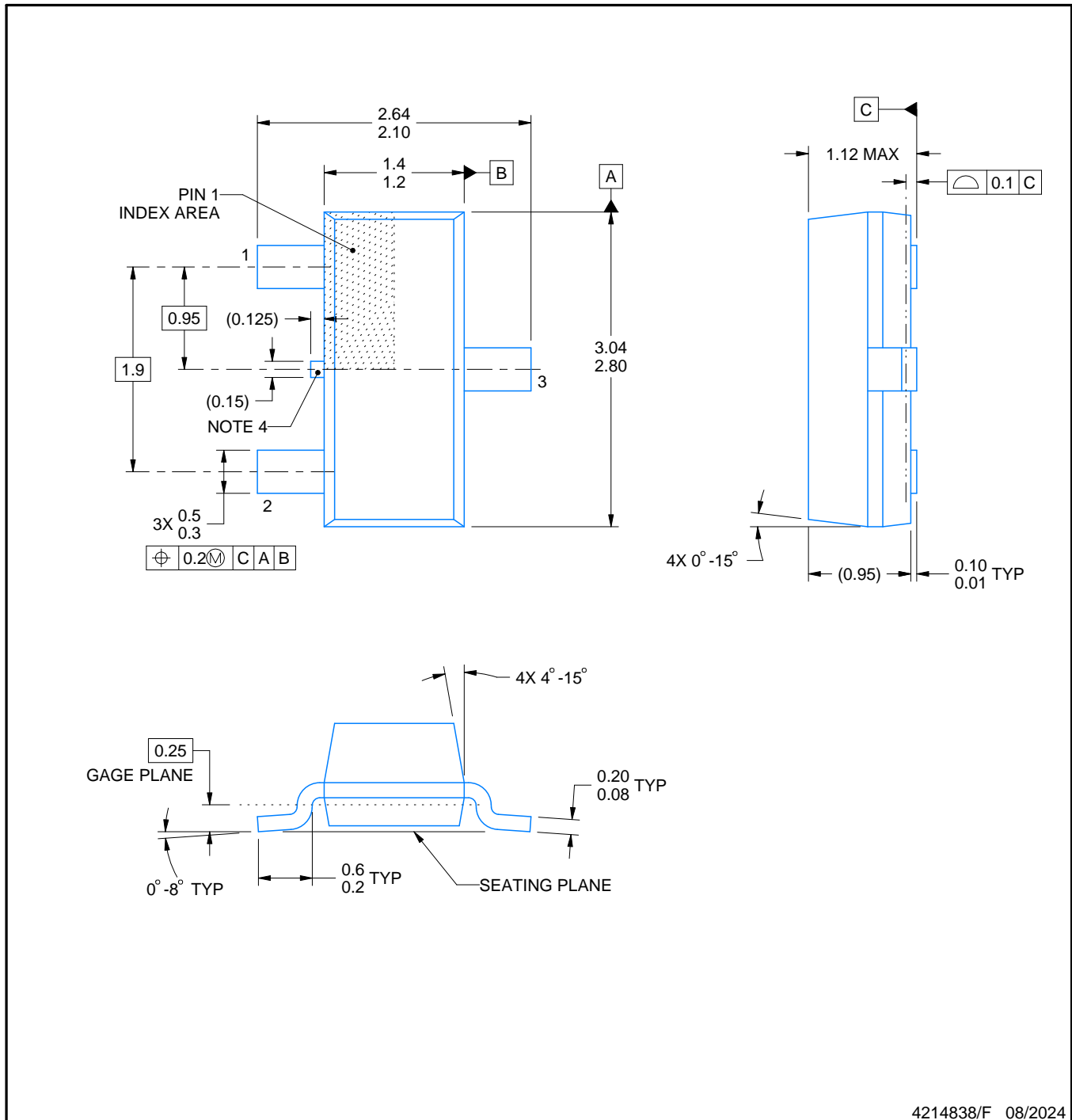


PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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