ESD204 4チャネル、低容量のサージおよびESD保護ダイオード

1 特長

- IEC 61000-4-2 レベル4 ESD保護
  - 接触放電 ±30kV
  - 空気ギャップ放電 ±30kV
- IEC 61000-4-4 EFT保護
  - 80A (5/50ns)
- IEC 61000-4-5 サージ保護
  - 5.5A (8/20µs)
  - 低いサージ・クランピング電圧
    5.5A I_{PP}で8.5V
- IO容量
  - 0.55pF (標準値)
- HDMI 2.0準拠
- DC降伏電圧: 5.5V (最小値)
- 非常に低いリーク電流: 10nA (最大値)
- 最大6Gbpsの高速インターフェイスをサポート
- 工業用温度範囲: -40℃～+125℃
- 使いやすいフロースルー配線パッケージ

2 アプリケーション

- 最終製品
  - IPネットワーク・カメラ
  - DVRおよびNVR
  - イーサネット・スイッチおよびルータ
  - ラップトップおよびデスクトップPC
  - セットトップ・ボックス
  - TVおよびモニタ
  - モバイルおよびタブレット
- インターフェイス
  - HDMI 2.0
  - HDMI 1.4
  - USB 3.0
  - DisplayPort 1.3
  - PCI Express 3.0
  - イーサネット10/100/1000Mbps

3 概要

ESD204は双方向のTVS ESD保護ダイオード・アレイで、最大5.5A (8/20µs)のHDMIおよびUSBサージ保護に対応しています。ESD204は、IEC 61000-4-2国際規格で規定されている最大レベル(レベル4)のESD耐性を備えています。

ESD204は、低いクランピングおよび高い差動帯域幅により、高速の信号をクリーンに通過させながら、下流のデバイスを堅牢に保護できます。このデバイスはチャネルごとの容量が0.55pFと低く、HDMI 2.0、HDMI 1.4、USB 3.0、イーサネット1Gなど、最高6Gbpsの高速インターフェイスを保護するために適しています。動的抵抗とクランピング電圧が低いため、過渡事象に対してシステム・レベルの保護が保証されます。

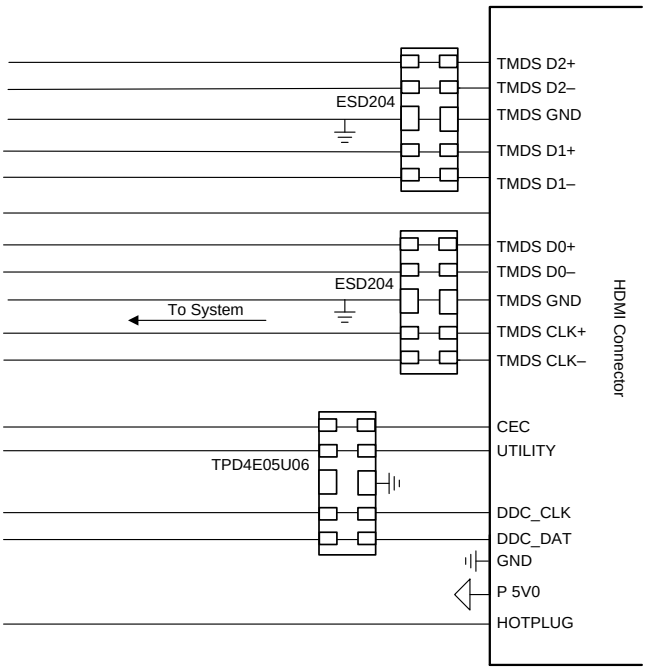
ESD204は、業界標準のUSON-10 (DQA)パッケージで供給されます。このパッケージはフロースルー配線と0.5mmピン・ピッチを採用しているため、実装が容易で、設計時間を短縮できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ESD204	USON (10)	2.50mm×1.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



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4 改訂履歴

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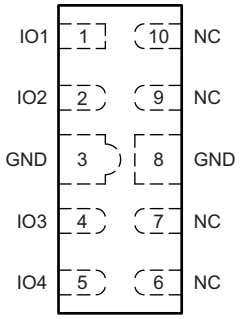
5 Pin Configuration and Functions

DQA Package
10-Pin USON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground
GND	8		
IO1	1	I/O	ESD protected channel. Connect to the line being protected.
IO2	2		
IO3	4		
IO4	5		
NC	6	NC	Not connected internally; Can be connected to line being protected for optional flow-through routing. Can also be left floating or grounded
NC	7		
NC	9		
NC	10		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25°C		80	A
Peak Pulse	IEC 61000-4-5 Surge (t_p 8/20 µs) Peak Power at 25°C		50	W
	IEC 61000-4-5 Surge (t_p 8/20 µs) Peak Current at 25°C		5.5	A
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings -JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-3.6		3.6	V
T_A	Operating Free Air Temperature	-40		125	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD204 DQA (USON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	184.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	138.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	41.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	137.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

At T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA, across operating temperature range	-3.6		3.6	V
V_{BRF}	Positive Breakdown Voltage, Each IO Pin to GND (1)	I_{IO} = 1 mA	5		7.9	V
V_{BRR}	Negative Breakdown Voltage, Each IO Pin to GND (1)	I_{IO} = -1 mA,	-7.9		-5	V
V_{HOLD}	Positive Holding Voltage, Each IO pin to GND (2)	I_{IO} = 1 mA		6.2		V
$V_{HOLD-NEG}$	Negative Holding Voltage, Each IO pin to GND (2)	I_{IO} = -1 mA		-6.2		V
V_{CLAMP}	Clamping voltage	Surge I_{PP} = 5.5 A, Each IO pin to GND, GND to Each IO pin, tp=8/20 μs		8.5		V
		TLP I_{PP} = 5 A, Each IO pin to GND, GND to Each IO pin, t_p=10/100 ns		8.2		V
		TLP I_{PP} = 16 A, Each IO pin to GND, GND to Each IO pin, t_p=10/100 ns		11.5		V
R_{DYN}	Dynamic resistance	Each IO Pin to GND, TLP t_p=10/100 ns		0.3		Ω
		GND to Each IO Pin, TLP t_p=10/100 ns		0.3		Ω
C_{LINE}	Line capacitance, any IO to GND	V_{IO} = 0 V, V_{p-p} = 30 mV, f = 1 MHz		0.55	0.65	pF
ΔC_{LINE}	Variation of line capacitance	C_{LINE1} - C_{LINE2}, V_{IO} = 0 V, Vp-p = 30 mV, f = 1 MHz		0.02	0.07	pF
C_{CROSS}	Line-to-line capacitance	V_{IO} = 0 V, V_{rms} = 30 mV, f = 1 MHz		0.25	0.35	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state

(2) VHOLD is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics

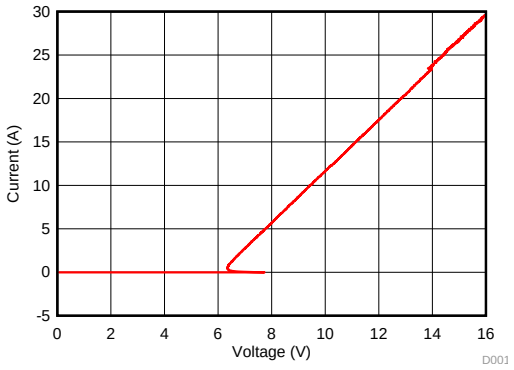


図 1. Positive TLP Curve, IO pin to GND (t_p = 100 ns)

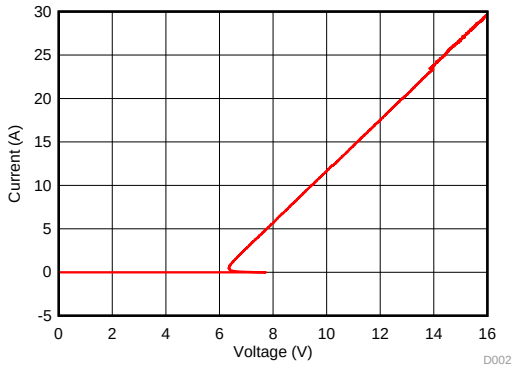


図 2. Negative TLP Curve, GND to IO pin (t_p=100 ns; Plotted as Positive TLP Curve from GND to IO pin)

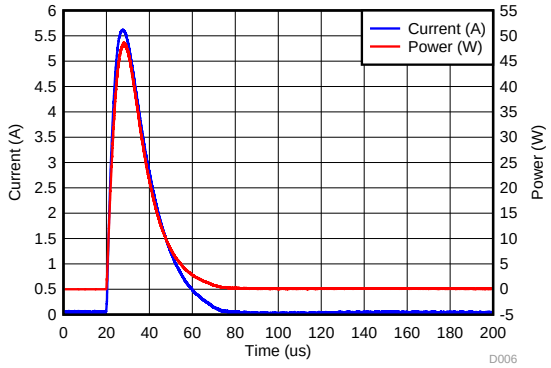


図 3. Surge Curve (t_p = 8/20 µs), any IO pin to GND

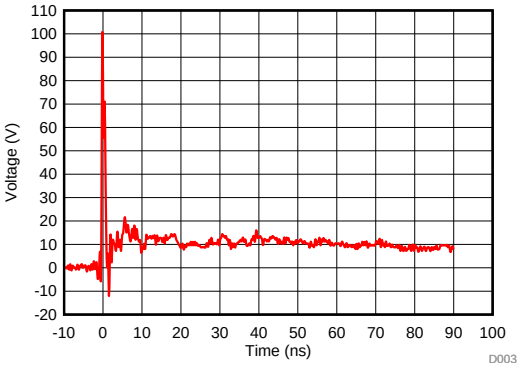


図 4. 8-kV IEC 61000-4-2 Clamping Voltage Waveform, IO pin to GND

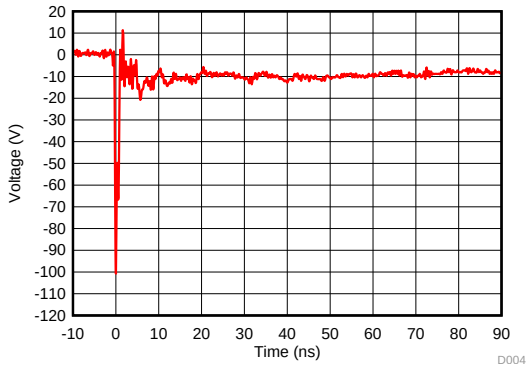


図 5. –8-kV IEC 61000-4-2 Clamping Voltage Waveform, GND pin to IO

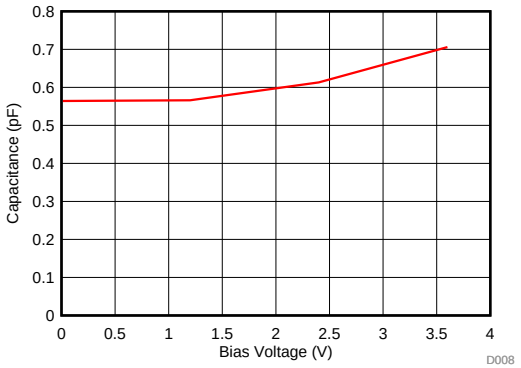


図 6. Capacitance vs Bias Voltage

Typical Characteristics (continued)

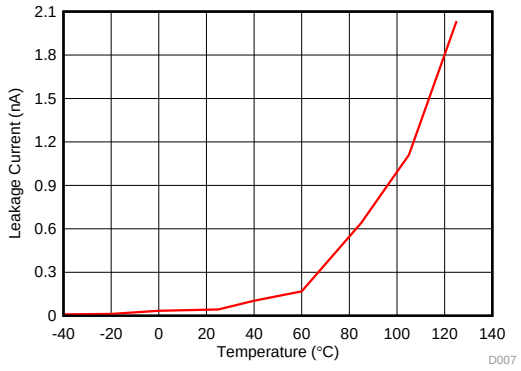


図 7. Leakage Current vs Temperature, IO pin to GND at 3.6 V Bias

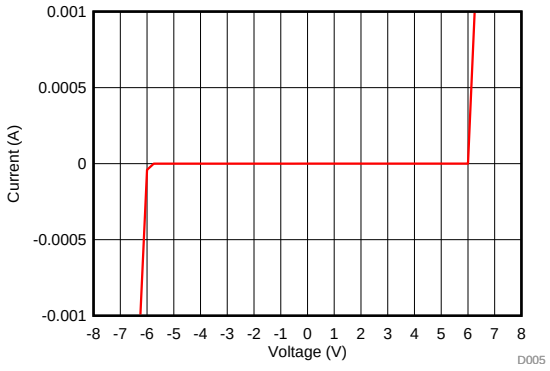


図 8. DC Voltage Sweep I-V Curve, IO pin to GND

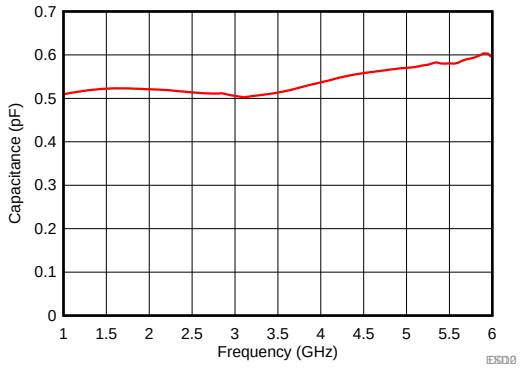


図 9. Capacitance vs Frequency

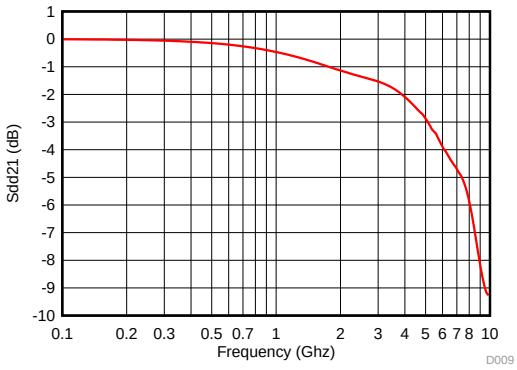


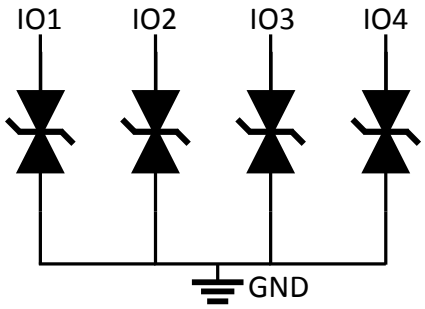
図 10. Differential Insertion Loss

7 Detailed Description

7.1 Overview

The ESD204 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes up to 30kV (Contact/Air) level specified by the IEC 61000-4-2 International Standard. Additionally, ESD204 dissipates 5.5 A of surge current (8/20 µs waveform) per IEC 61000-4-5 standard. The ultra-low capacitance makes this device capable of supporting any super high-speed signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

ESD204 provides ESD protection up to ±30-kV contact and ±30-kV air gap per IEC61000-4-2 standard. During an ESD event, ESD diode connected to the IO pin turns on and diverts the ESD current to ground. Additionally, ESD204 also provides protection against IEC 61000-4-5 surge currents up to 5.5 A (8/20 µs waveform) and up to 80 A per IEC 61000-4-4 electrical fast transient (EFT) standard. Please see the Application Note on IEC61000-4-x standard based tests. ESD204 provides a very low clamping voltage of 11.5 V at 16 A 100 ns TLP current and 8.5 V at 5.5 A surge current (8/20 µs waveform).

The capacitance between each I/O pin to ground is 0.55 pF (typical) and 0.65 pF (maximum). This device supports data rates up to 6 Gbps. The DC breakdown voltage of each I/O pin is a minimum of ±5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V. The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ±3.6 V.

7.4 Device Functional Modes

The ESD204 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±30 kV (contact/air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD204 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

> 注
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESD204 is a diode type TVS array which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between an interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

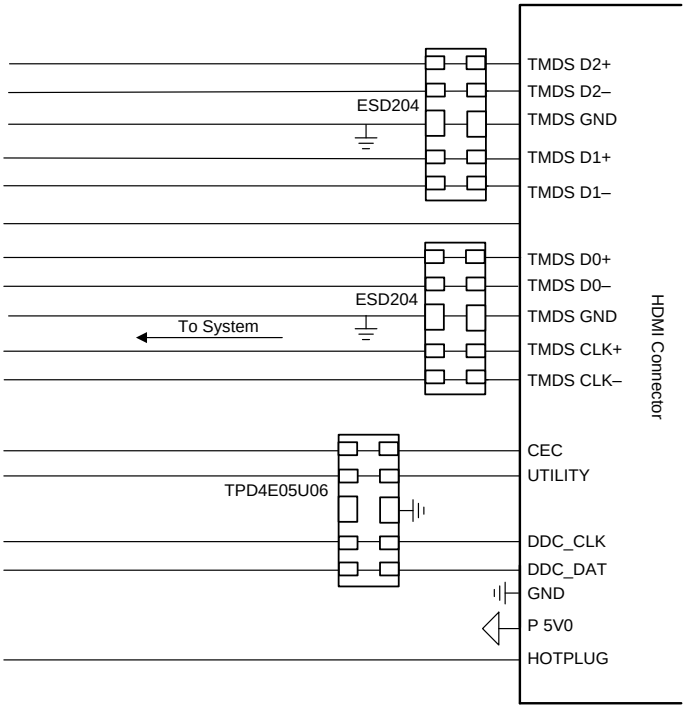


図 11. ESD204 Protecting the HDMI Interface

8.2.1 Design Requirements

In this design example, two ESD204 devices and one TPD4E05U06 device are used to protect an HDMI 2.0 interface. For HDMI 2.0 application design parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on high speed differential data lines	0 to 3.6 V
Operating frequency of high speed data lines	3 GHz (First Harmonic)
Signal range on control lines (CEC, UTILITY, DDC_CLK and DDC_DAT)	0 to 5 V

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

ESD204 supports signal ranges between –3.6 V and 3.6 V, which supports the high-speed lines on the HDMI 2.0 application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V, which supports the HDMI control lines.

8.2.2.2 Operating Frequency

The ESD204 has a 0.55 pF (typical) capacitance, which supports the HDMI 2.0 rate of 6 Gbps. The TPD4E05U06 has a typical capacitance of 0.5 pF, which easily support the control lines. The ESD204 has 4 identical protection channels for the differential HDMI high-speed signal lines. The symmetrical pin out of the device with a ground pin between the two differential signal pins makes it suitable for this application.

8.2.3 Application Curves

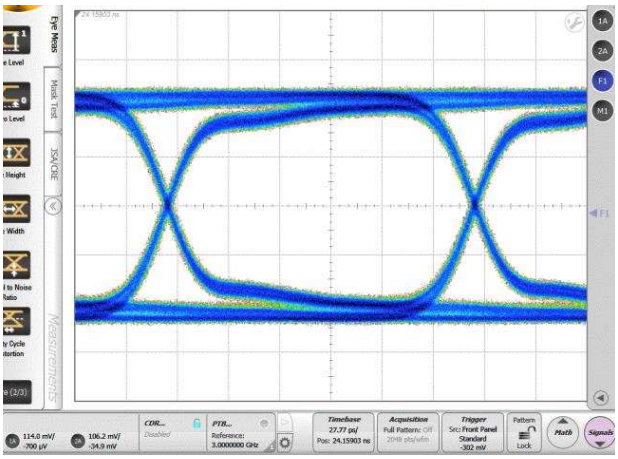


図 12. HDMI 2.0 6 Gbps EYE Diagram (Bare Board)

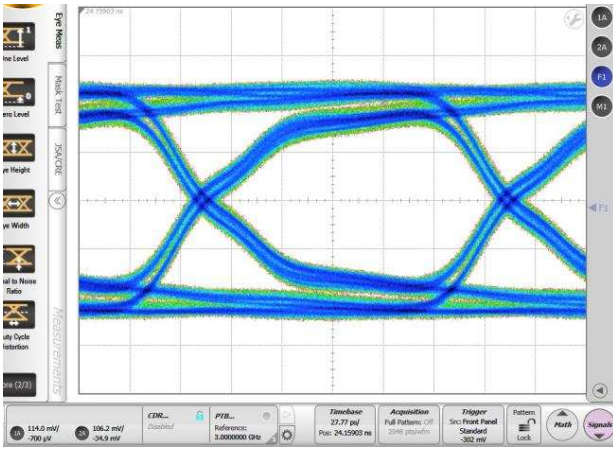


図 13. HDMI 2.0 6 Gbps Eye Diagram with ESD204

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

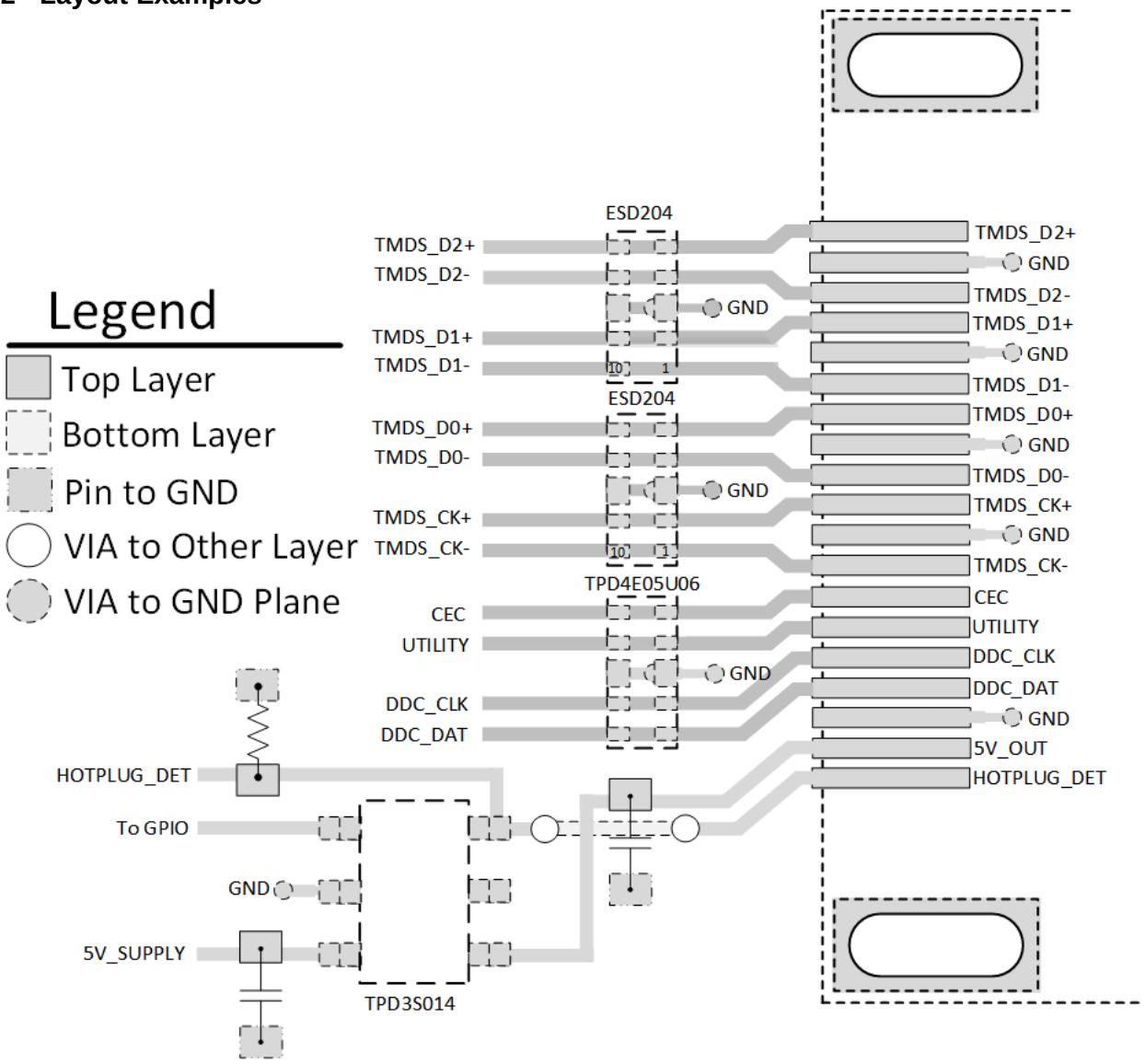


図 14. HDMI Type-A Transmitter Port Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.3 商標

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11.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD204DQAR	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CE5, CEG) CEY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

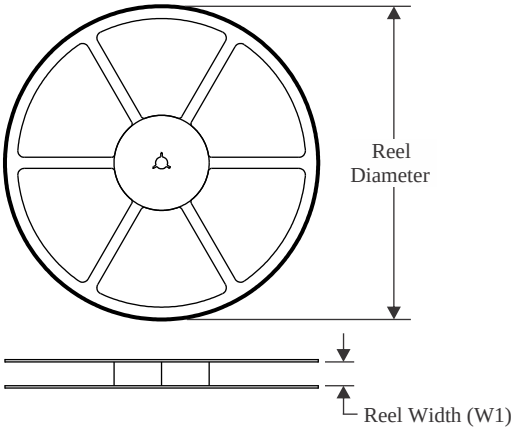
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

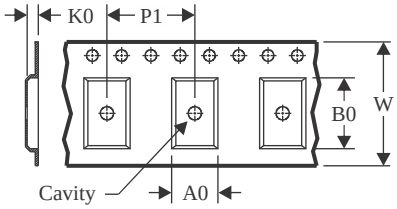
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

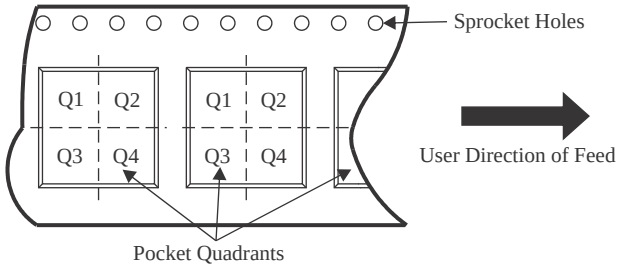


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

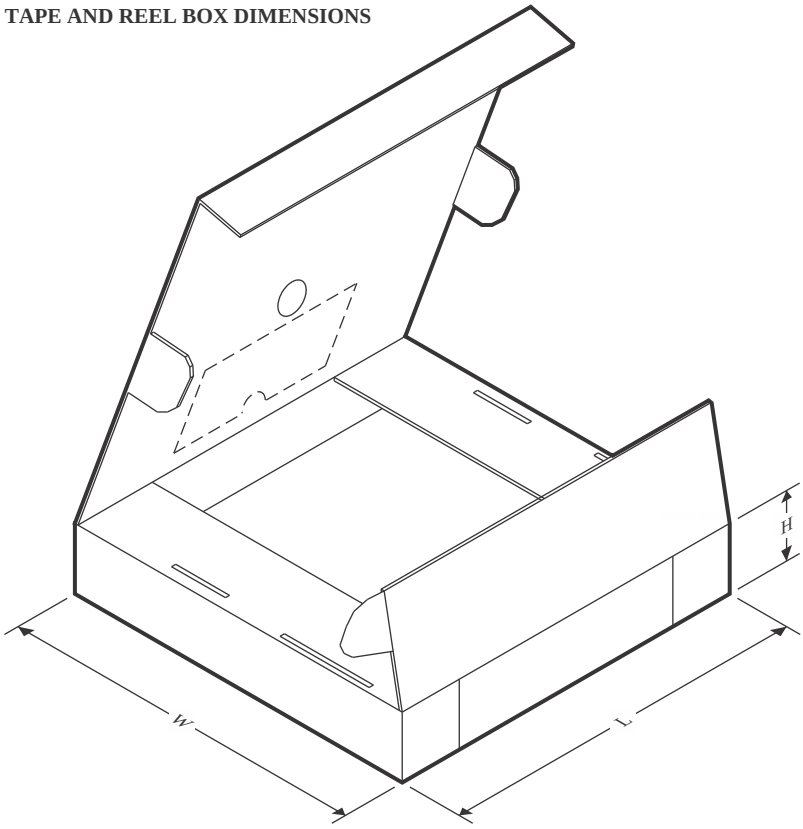
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD204DQAR	USON	DQA	10	3000	180.0	8.4	1.2	2.7	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD204DQAR	USON	DQA	10	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

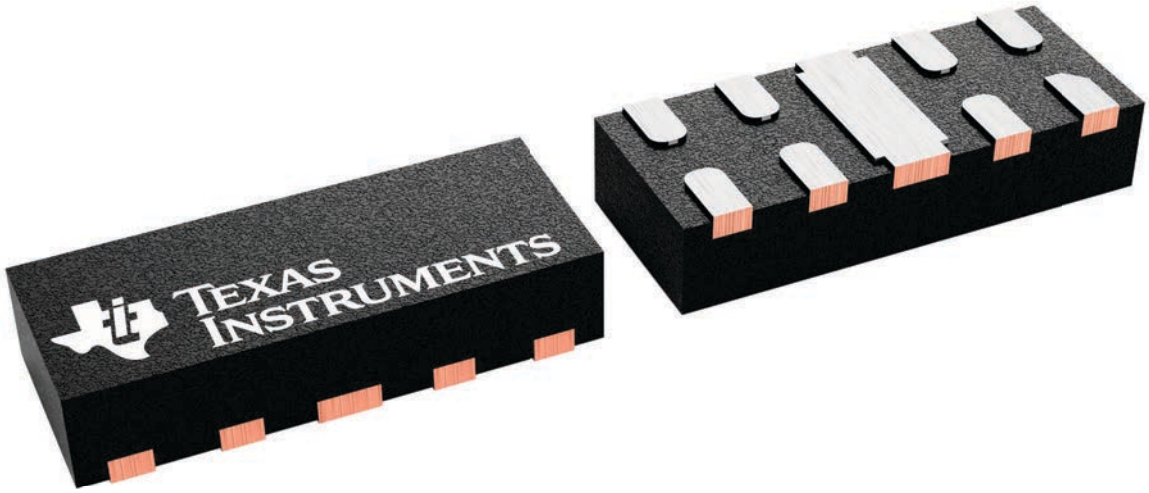
DQA 10

USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



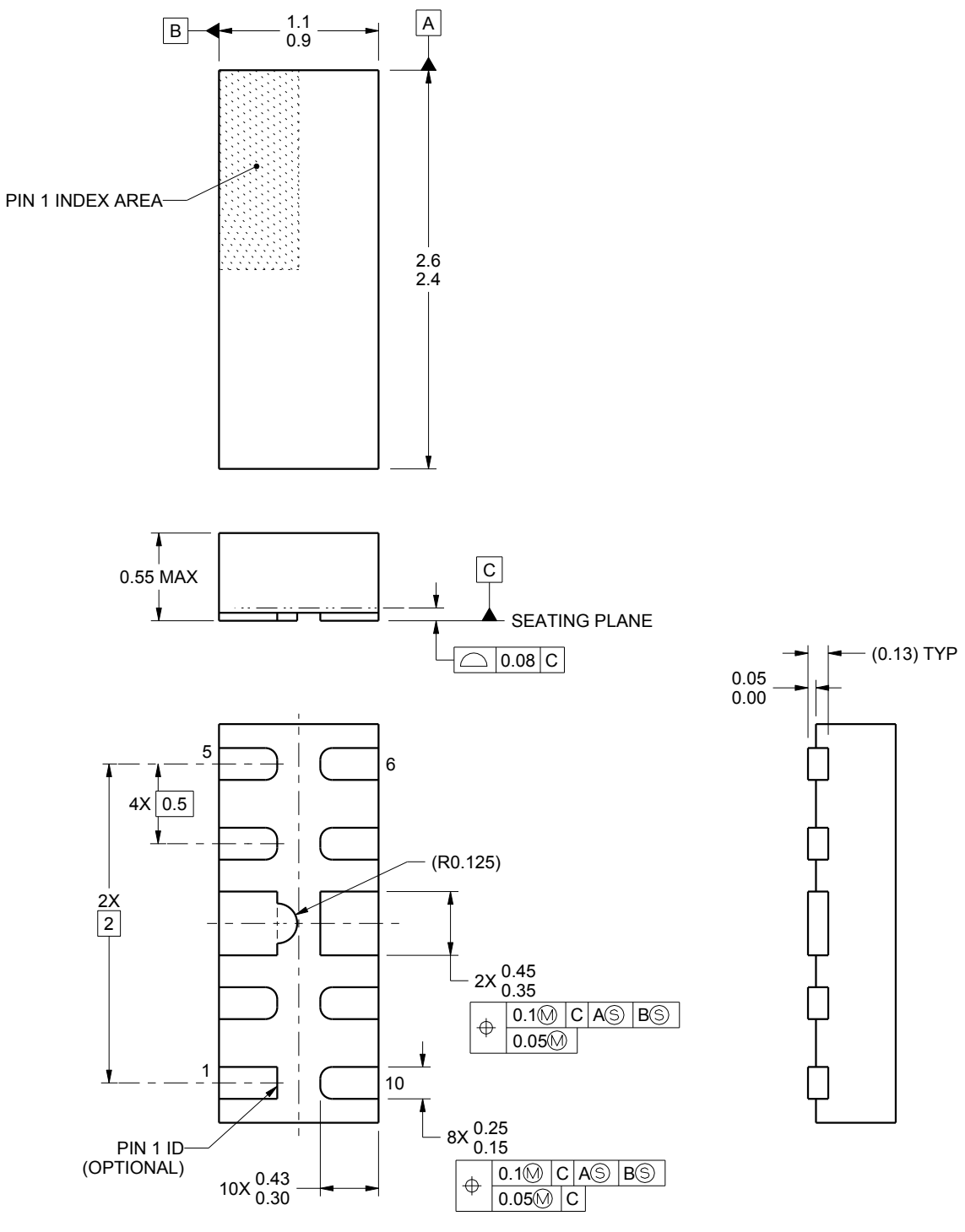
4230320/A

PACKAGE OUTLINE

DQA0010A

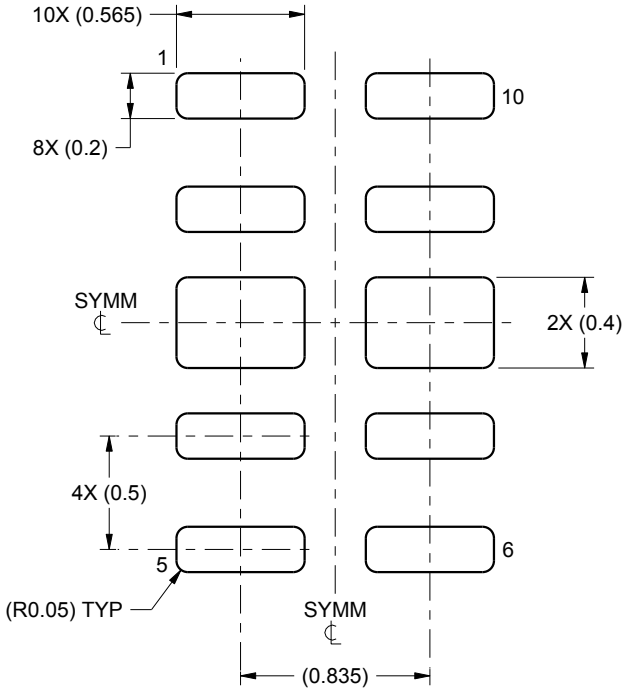
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

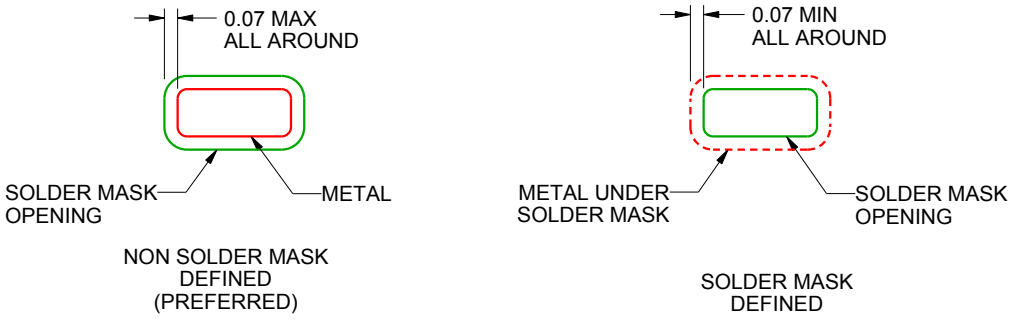


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

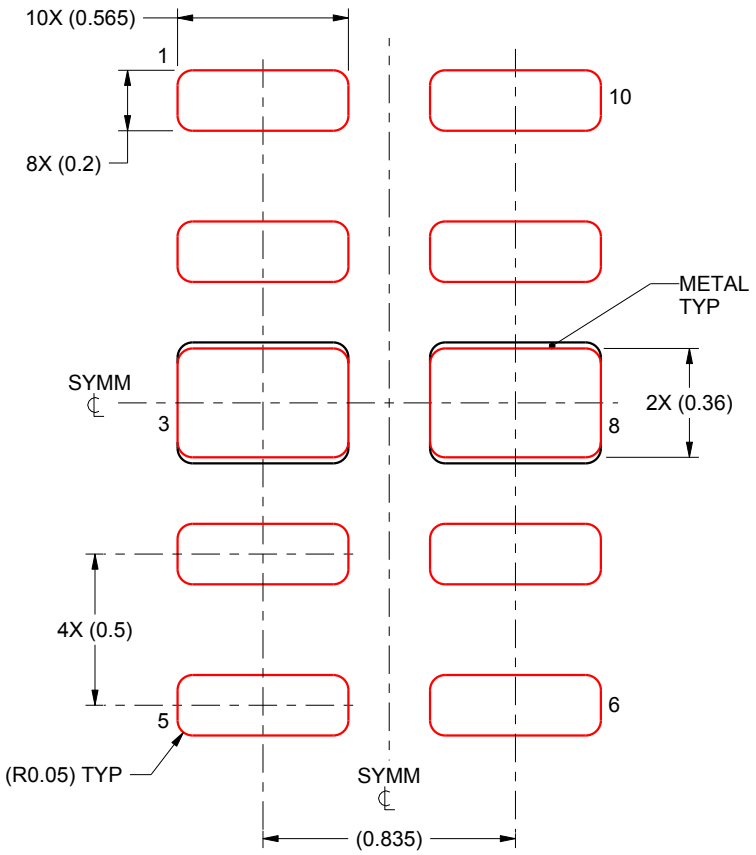
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

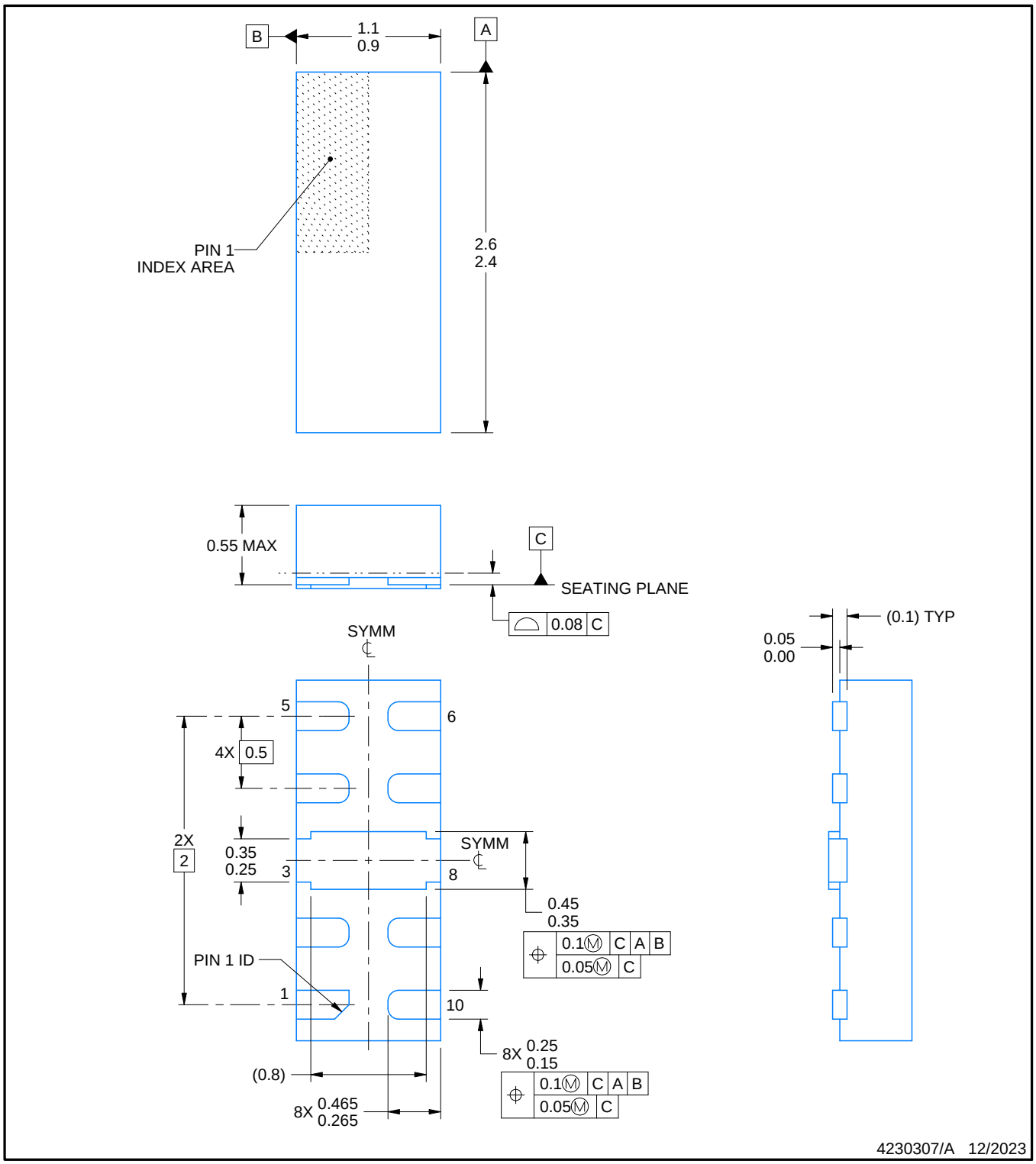
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DQA0010B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

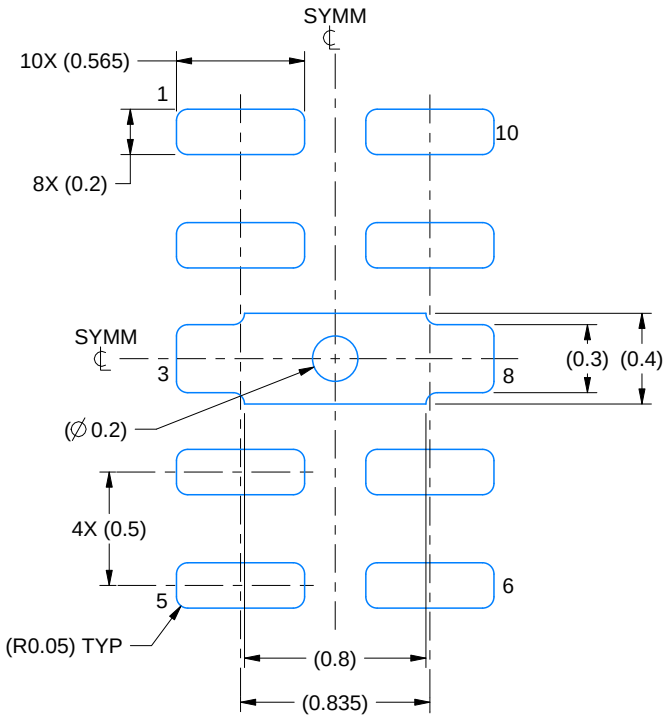
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

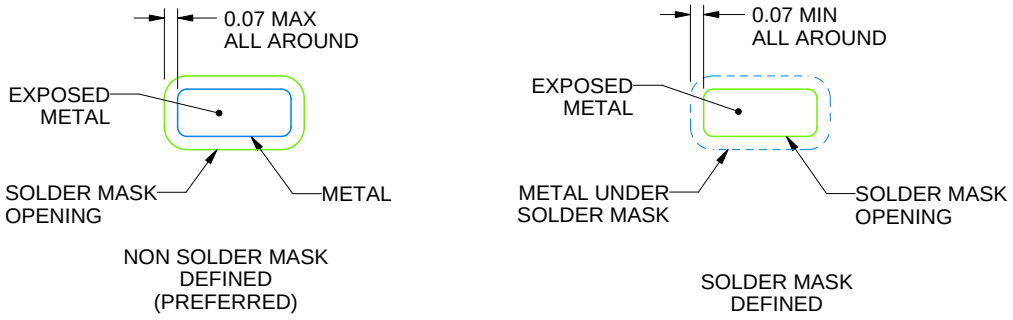
DQA0010B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

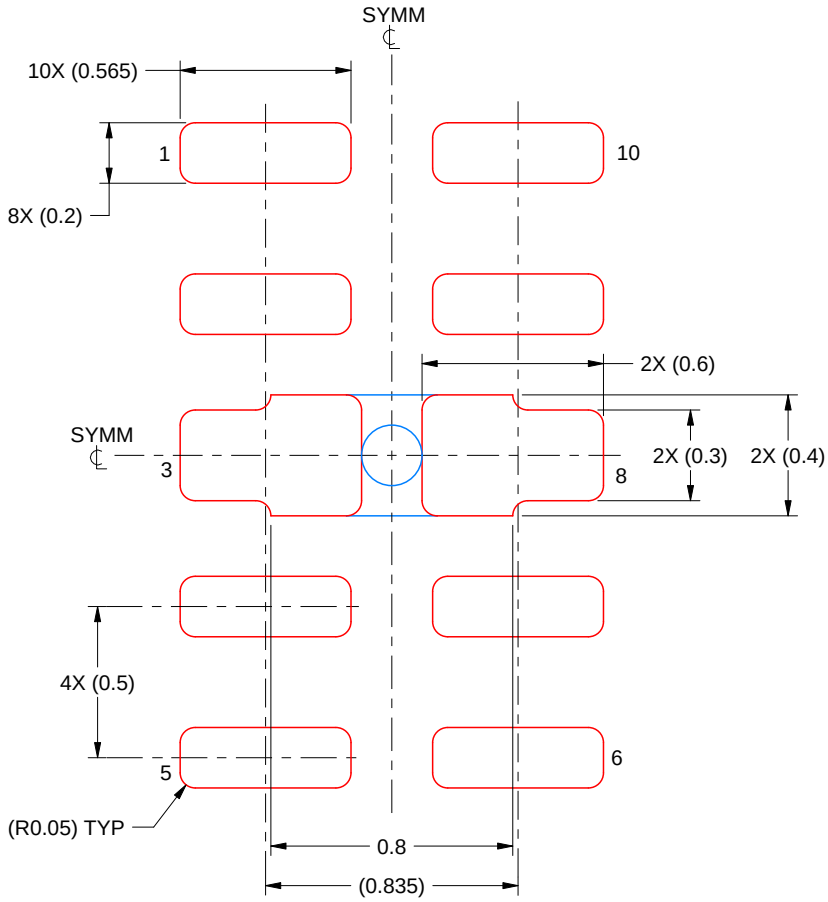


SOLDER MASK DETAILS

4230307/A 12/2023

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4230307/A 12/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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