TEXAS INSTRUMENTS
DS90UB635-Q1
JAJSMU0 – FEBRUARY 2023

DS90UB635-Q1 CSI-2 インターフェイスを搭載した、2.3MP/60fps カメラ、レーダー、他のセンサ用の FPD-Link III 4.16Gbps シリアライザ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 2:-40℃～+105℃の動作時周囲温度範囲
- ISO 10605 および IEC 61000-4-2 ESD に準拠
- Power-over-Coax (PoC) 対応トランシーバ
- 4.16Gbps グレードのシリアライザにより、フル HD 1080p 2.3MP 60fps および 4MP 30fps イメージャを含む高速センサをサポート
- D-PHY v1.2 および CSI-2 v1.3 準拠のシステム・インターフェイス
  - 最大 4 つのデータ・レーン、600Mbps～832Mbps/レーン
  - 最大 4 つの仮想チャネルをサポート
- 高精度なマルチカメラ・クロッキングおよび同期
- 柔軟でプログラム可能な出力クロック・ジェネレータ
- CRC データ保護、センサ・データ整合性チェック、I2C 書き込み保護、電圧および温度測定、プログラム可能なアラーム、BIST、パターン生成、ライン・フォルト検出を含む高度なデータ保護および診断機能
- シングルエンドの同軸またはシールド付きツイストペア (STP) ケーブルに対応
- 超低レイテンシの双方向 I2C および GPIO 制御チャネルにより、ECU からの ISP 制御が可能
- 1.8V の単一電源電圧
- 低消費電力 (標準値 0.28W)
- 超低レイテンシの双方向 I2C および GPIO 制御チャネルにより、ECU からの ISP 制御が可能
- 偽造防止向けの一意のダイ ID
- DS90UB638-Q1 デシリアライザおよび DS90UB662-Q1 ハブと互換
- 小型の 5mm × 5mm VQFN パッケージ、およびコンパクト・カメラ・モジュール設計向けの PoC ソリューション・サイズ

2 アプリケーション

- 先進運転支援システム (ADAS)
  - サラウンド・ビュー・システム (SVS)
  - カメラ監視システム (CMS)
  - 前方視野カメラ (FC)
  - ドライバー監視システム (DMS)
  - リアビュー・カメラ (RVC)
  - タイム・オブ・フライト (ToF) センサ・モジュール
  - サイド・ミラー・ディスプレイ (SMD)
  - 車載用衛星レーダー・モジュール
- セキュリティと監視
- 産業用および医療用イメージング

3 概要

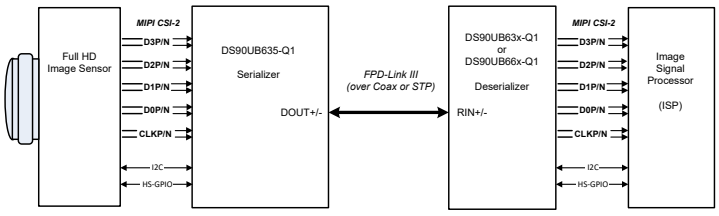
DS90UB635-Q1 シリアライザは、テキサス・インスツルメンツの FPD-Link III デバイス・ファミリの製品であり、2.3MP/60fps のイメージャを搭載した高速 RAW データ・センサや、4MP/30fps のカメラ、衛星用レーダー、LIDAR、タイム・オブ・フライト (ToF) センサをサポートするように設計されています。このチップは、4.16Gbps の順方向チャネルと超低レイテンシの 50Mbps の双方向制御チャネルを備えており、1 本の同軸ケーブル (PoC) または STP ケーブルによる給電をサポートしています。DS90UB635-Q1 は、高度なデータ保護および診断機能により、ADAS および自動運転をサポートします。デシリアライザと組み合わせることで、DS90UB635-Q1 は高精度のマルチカメラ・センサ・クロックおよびセンサ同期を実現します。

DS90UB635-Q1 は、温度範囲が -40℃～105℃と広く、AEC-Q100 認定済みです。このシリアライザは、スペースの制約があるセンサ・アプリケーション向けに小型の 5mm × 5mm VQFN パッケージで供給されます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
DS90UB635-Q1	VQFN (32)	5.00mm × 5.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2023	*	Initial Release

5 Pin Configuration and Functions

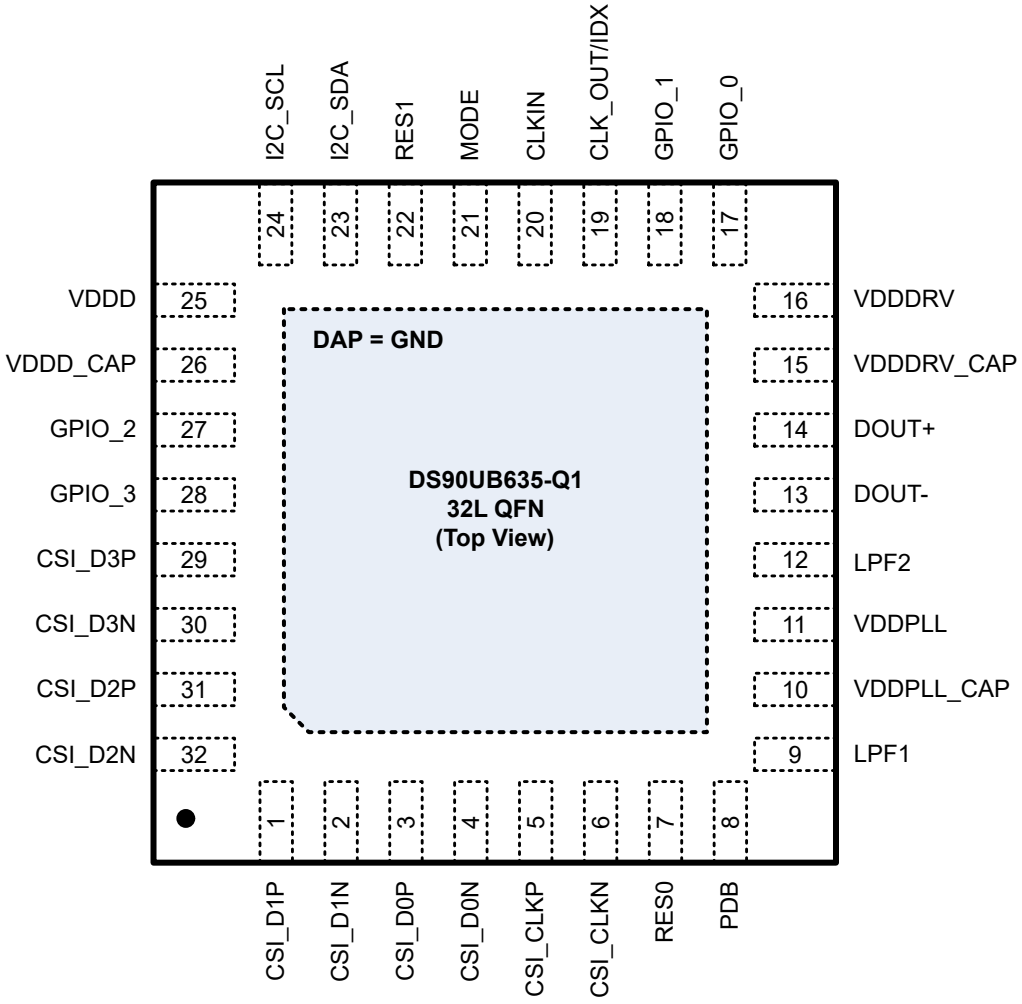


図 5-1. RHB Package
32-Pin VQFN
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CSI INTERFACE			
CSI_CLKP	5	I, DPHY	CSI-2 clock input pins. Connect to a CSI-2 clock source with matched 100-Ω (±5%) impedance interconnects.
CSI_CLKN	6	I, DPHY	
CSI_D0P	3	I, DPHY	CSI-2 data input pins. Connect to a CSI-2 data sources with matched 100-Ω (±5%) impedance interconnects. If unused, these pins may be left floating.
CSI_D0N	4	I, DPHY	
CSI_D1P	1	I, DPHY	
CSI_D1N	2	I, DPHY	
CSI_D2P	31	I, DPHY	
CSI_D2N	32	I, DPHY	
CSI_D3P	29	I, DPHY	
CSI_D3N	30	I, DPHY	

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SERIAL CONTROL INTERFACE			
I2C_SDA	23	OD	I2C Data and Clock Pins. Typically pulled up by 470-Ω to 4.7-kΩ resistors to either 1.8-V or 3.3-V supply rail depending on IDX setting. See *I2C Interface Configuration* for further details on the I2C implementation of the DS90UB635-Q1.
I2C_SCL	24	OD	
CONFIGURATION and CONTROL			
RES0	7	I	Reserved pin – Connect to GND
RES1	22	I	Reserved pin – Do not connect (leave floating)
PDB	8	I, PD	Power-down inverted Input Pin. Internal 1-MΩ pulldown. Typically connected to processor GPIO with pull down. When PDB input is brought HIGH, the device is enabled and internal register and state machines are reset to default values. Asserting PDB signal low will power down the device and consume minimum power. The default function of this pin is PDB = LOW; POWER DOWN. PDB should remain low until after power supplies are applied and reach minimum required levels. See *Power Down (PDB)* for further details on the function of PDB. **PDB INPUT IS NOT 3.3-V TOLERANT**. PDB = 1.8 V, device is enabled (normal operation) PDB = 0, device is powered down.
MODE	21	I, S	Mode select configuration input. Default operational mode will be strapped at start-up based on the MODE input voltage when PDB transitions LOW to HIGH. Typically connected to voltage divider through external pullup to VDD18 and pulldown to GND applying an appropriate bias voltage. See *MODE* for details.
CLK_OUT/IDX	19	I/O, S	IDX pin sets the I2C pullup voltage and device address; connect to external pullup to VDD and pulldown to GND to create a voltage divider. When PDB transitions LOW to HIGH, the strap input voltage is sensed at the CLOCK_OUT/IDX pin to determine functionality and then converted to CLK_OUT. See *I2C Interface Configuration* for details. If CLK_OUT is used, the minimum resistance on the pin is 35 kΩ. If unused, CLK_OUT/IDX may be tied to GND.
FPD-LINK III INTERFACE			
DOUT-	13	I/O	FPD-Link III Input/Output pins. These pins must be AC-coupled. See 図 8-5 and 図 8-6 for typical connection diagrams and 表 8-3 for recommended capacitor values.
DOUT+	14	I/O	
POWER AND GROUND			
VDDD_CAP	26	D, P	A connection for an internal analog regulator decoupling capacitor. Typically connected to 10-µF, 0.1-µF, and 0.01-µF capacitors to GND. Do not connect to an external supply rail. See *Typical Application* for more details.
VDDDRV_CAP	15	D, P	A connection for an internal analog regulator decoupling capacitor. Typically connected to 10-µF, 0.1-µF, and 0.01-µF capacitors to GND. Do not connect to an external supply rail. See *Typical Application* for more details.
VDDPLL_CAP	10	D, P	A connection for an internal analog regulator decoupling capacitor. Typically connected to 10-µF, 0.1-µF, and 0.01-µF capacitors to GND. Do not connect to an external supply rail. See *Typical Application* for more details.
VDDD	25	P	1.8-V (±5%) Power Supply pin. Typically connected to 1-µF and 0.01-µF capacitors to GND.
VDDDRV	16	P	1.8-V (±5%) Analog Power Supply pin. Typically connected to 1-µF and 0.01-µF capacitors to GND.
VDDPLL	11	P	1.8-V (±5%) Analog Power Supply pin. Typically connected to 1-µF and 0.01-µF capacitors to GND.
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the VQFN package. Connect to the ground plane (GND).
LOOP FILTER			
LPF1	9	P	Loop Filter 1: Connect as described in *セクション 8.2.2.4*.
LPF2	12	P	Loop Filter 2: Connect as described in *セクション 8.2.2.4*.
CLOCK INTERFACE AND GPIO			
GPIO_0	17	I/O, PD	General-Purpose Input/Output pins. These pins can also be configured to sense the voltage at their inputs. See *Voltage and Temperature Sensing*. At power up, these GPIO pins default to inputs with a 300-kΩ (typical) internal pulldown resistor. These pins may be left floating if unused, but TI recommends to set the GPIOx_INPUT_EN to 0 to disable the pins. See *セクション 7.3.6* for programmability.
GPIO_1	18	I/O, PD	
GPIO_2	27	I/O, PD	General-Purpose Input/Output pins. At power up, these GPIO pins default to inputs with a 300-kΩ (typical) internal pulldown resistor. These pins may be left floating if unused, but TI recommends to set the GPIOx_INPUT_EN to 0 to disable the pins. See *セクション 7.3.6* for programmability.
GPIO_3	28	I/O. PD	
CLKIN	20	I	Reference Clock Input pin. If operating in non-sync external clock mode, connect this pin to a local clock source. If unused (like other clocking modes), this pin may be left open. See 表 7-8 for more information on clocking modes.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	PIN OR FREQUENCY	MIN	MAX	UNIT
Supply voltage, VDD	VDDD, VDDDRV, VDDPLL	–0.3	2.16	V
Input voltage	GPIO[3:0], PDB, CLKIN, IDX, MODE, CSI_CLKP/N, CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N	–0.3	V_{DD} + 0.3	V
FPD-Link III output voltage	DOUT+, DOUT-	–0.3	1.21	V
Open-drain voltage	I2C_SDA, I2C_SCL	–0.3	3.96	V
Junction temperature, T_J			150	°C
Storage termperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) ESD Classification Level 3A, per AEC Q100-002(1)	All pins except Media Dependent Interface Pins	±4000	V
			Media Dependent Interface Pins		
		Charged-device model (CDM) ESD Classification Level C6, per AEC Q100-011		±1500	V
		IEC 61000-4-2 R_D = 330 Ω, C_S = 150 pF	Contact Discharge (DOUT+ and DOUT-)	±8000	V
			Air Discharge (DOUT+ and DOUT-)	±18000	V
		ISO 10605 R_D = 330 Ω, C_S = 150 pF and 330 pF R_D = 2 kΩ, C_S = 150 pF and 330 pF	Contact Discharge (DOUT+ and DOUT-)	±8000	V
			Air Discharge (DOUT+ and DOUT-)	±18000	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	VDD (VDDD, VDDDRV, VDDPLL)	1.71	1.8	1.89	V
Open-drain voltage	I2C_SDA, I2C_SCL = $V_{(I2C)}$	1.71		3.6	V
Operating free-air temperature (T_A)		–40	25	105	°C
Mipi data rate (per CSI-2 lane)		600		832	Mbps
Reference clock input frequency		25		104	MHz
Local I^2C frequency (f_{I2C})				1	MHz
Supply noise(3)	VDD (VDDD, VDDDRV, VDDPLL)			25	mV_{p-p}
Differential supply noise between DOUT+ and DOUT- (PSR)	f = 10 KHz - 50 MHz (coax mode only)			25	mV_{p-p}
	f = 30 Hz, 10-90% Rise/Fall Time > 100µs (coax mode only)			25	mV_{p-p}
Input clock jitter for non-synchronous mode (t_{JIT})	CLKIN			0.05	UI_CLK_IN(2)
Back channel input jitter (t_{JIT-BC})	DOUT+, DOUT-			0.4	UI_BC(1)

(1) The back channel unit interval (UI_BC) is 1/(BC line-rate). For example, the typical UI_BC is 1/100 MHz = 10 ns. If the jitter tolerance is 0.4 UI, convert the jitter in UI to seconds using this equation: 10 ns × 0.4 UI = 4 ns
(2) Non-synchronous mode - For a given clock, the UI is defined as 1/clock_freq. For example when the clock = 50Mhz, the typical UI_CLK_IN is 1/50 MHz = 20 ns.
(3) DC - 50 MHz

6.4 Thermal Information

THERMAL METRIC(1)		DS90UB635-Q1 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
POWER CONSUMPTION							
I_{DD_TOTAL}	Supply current	416-MHz CSI Input Clock, 4 Lane Mode, Checkerboard Pattern	VDDPLL, VDDD, VDDDRV		160	225	mA
I_{DDPLL}			VDDPLL		55	80	
I_{DDD}			VDDD		45	70	
I_{DDDRV}			VDDDRV		60	75	
1.8-V LVCMOS I/O (VDD) = 1.71 V to 1.89 V							
V_{OH}	High level output voltage	I_{OH} = –4 mA	GPIO[3:0], CLK_OUT	$V_{(VDD)}$ – 0.45		$V_{(VDD)}$	V
V_{OL}	Low level output voltage	I_{OL} = +4 mA	GPIO[3:0], CLK_OUT	GND		0.45	V
V_{IH}	High level input voltage		GPIO[3:0], PDB, CLKIN	$V_{(VDD)}$ × 0.65		$V_{(VDD)}$	V
V_{IL}	Low level input voltage		GPIO[3:0], PDB, CLKIN	GND		$V_{(VDD)}$ × 0.35	V
I_{IH}	Input high current	V_{IN} = $V_{(VDD)}$	GPIO[3:0], PDB, CLKIN			20	µA
I_{IL}	Input low current	V_{IN} = GND	GPIO[3:0], PDB, CLKIN	-20			µA
I_{OS}	Output short-circuit current	V_{OUT} = 0 V			-36		mA
I_{OZ}	TRI-STATE output current	V_{OUT} = $V_{(VDD)}$, V_{OUT} = GND	GPIO[3:0], CLK_OUT			±20	µA
C_{IN}	Input capacitance				5		pF

6.5 Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
FPD-LINK III INPUT/OUTPUT							
V_{IN-BC}	Single-ended input voltage	Coaxial configuration, 50 Ω, maximum cable length	DOUT+, DOUT-	120			mV
V_{ID-BC}	Differential input voltage	STP configuration, 100 Ω, maximum cable length	DOUT+, DOUT-	240			
E_{H-FC}	Forward channel eye height	Coaxial configuration, FPD-Link forward channel = 4.16 Gbps	DOUT+, DOUT-		425		mVp-p
		STP configuration, FPD-Link forward channel = 4.16 Gbps	DOUT+, DOUT-		850		
t_{TR-FC}	Forward channel output transition time	FPD-Link forward channel = 4.16Gbps; 20% to 80%	DOUT+, DOUT-		65		ps
t_{JIT-FC}	Forward channel output jitter	Synchronous mode, measured with f/15 – 3dB CDR Loop BW	DOUT+, DOUT-		0.21		UI
		Non-synchronous mode, measured with f/15 –3dB CDR Loop BW	DOUT+, DOUT-		0.22		
f_{REF}	Internal reference frequency	Non-synchronous internal clocking mode		24.2		25.5	MHz
FPD-LINK III DRIVER SPECIFICATIONS (DIFFERENTIAL)							
V_{ODp-p}	Output differential voltage	R_L = 100 Ω	DOUT+, DOUT-	1040	1150	1340	mV_{p-p}
ΔV_{OD}	Output voltage imbalance		DOUT+, DOUT-		5	24	mV
V_{OS}	Output differential offset voltage		DOUT+, DOUT-		575		mV
ΔV_{OS}	Offset voltage imbalance		DOUT+, DOUT-		2		mV
I_{OS}	Output short-circuit current	DOUT = 0 V	DOUT+, DOUT-		–22		mA
R_T	Internal termination resistance	Between DOUT+ and DOUT-	DOUT+, DOUT-	80	100	120	Ω
FPD-LINK III DRIVER SPECIFICATIONS (SINGLE-ENDED)							
V_{OUT}	Output single-ended voltage	R_L = 50 Ω	DOUT+, DOUT-	520	575	670	mV_{p-p}
I_{OS}	Output short-circuit current	DOUT = 0 V	DOUT+, DOUT-		–22		mA
R_T	Single-ended termination resistance		DOUT+, DOUT-	40	50	60	Ω
VOLTAGE AND TEMPERATURE SENSING							
V_{ACC}	Voltage accuracy	See Voltage and Temperature Sensing	GPIO[1:0]		±1		LSB
T_{ACC}	Temperature accuracy	See Voltage and Temperature Sensing			±1		LSB

6.5 Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
CSI-2 HS INTERFACE DC SPECIFICATIONS							
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N	70		330	mV
V_{IDTH}	Differential input high threshold		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N			70	mV
V_{IDTL}	Differential input low threshold		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N	–70			mV
Z_{ID}	Differential input impedance		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N	80	100	125	Ω
CSI-2 HS INTERFACE AC SPECIFICATIONS							
t_{HOLD}	Data to clock setup time		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N	0.15			UI
t_{SETUP}	Data to clock hold time		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N	0.15			UI
CSI-2 LP INTERFACE DC SPECIFICATIONS							
V_{IH}	Logic high input voltage		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N	880	790		mV
V_{IL}	Logic low input voltage		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N		710	550	mV
V_{HYST}	Input hysteresis		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLKP/N	25	75		mV

6.5 Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LVCMOS I/O							
t_{CLH}	LVCMOS low-to-high transition time	$V_{(VDD)}$ = 1.71 to 1.89 V	GPIO[3:0]		2		ns
t_{CHL}	LVCMOS high-to-low transition time	$V_{(VDD)}$ = 1.71 to 1.89 V	GPIO[3:0]		2		ns
t_{PDB}	PDB reset pulse width	Voltage supplies applied and stable	PDB	3			ms
SERIAL CONTROL BUS							
V_{IH}	Input high level		I2C_SCL, I2C_SDA	0.7 × $V_{(I2C)}$		$V_{(I2C)}$	mV
V_{IL}	Input low level		I2C_SCL, I2C_SDA	GND		0.3 × $V_{(I2C)}$	mV
V_{HY}	Input hysteresis		I2C_SCL, I2C_SDA		>50		mV
V_{OL}	Output low level	$V_{(I2C)}$ < 2 V, I_{OL} = 3 mA, Standard-mode/ Fast-mode	I2C_SCL, I2C_SDA	0		0.2 × $V_{(I2C)}$	V
		$V_{(I2C)}$ < 2 V, I_{OL} = 20 mA, Fast-mode plus	I2C_SCL, I2C_SDA	0		0.2 × $V_{(I2C)}$	V
		$V_{(I2C)}$ > 2 V, I_{OL} = 3 mA, Standard-mode/ Fast-mode	I2C_SCL, I2C_SDA	0		0.4	V
		$V_{(I2C)}$ > 2 V, I_{OL} = 20 mA, Fast-mode plus	I2C_SCL, I2C_SDA	0		0.4	V
I_{IH}	Input high current	V_{IN} = $V_{(I2C)}$	I2C_SCL, I2C_SDA	-10		10	µA
I_{IL}	Input low current	V_{IN} = 0 V	I2C_SCL, I2C_SDA	-10		10	µA
I_{IL}	Input low current	V_{IN} = 0 V	I2C_SCL, I2C_SDA	-10		10	µA
C_{IN}	Input capacitance		I2C_SCL, I2C_SDA		5		pf

6.6 Recommended Timing for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard-mode	>0		100	kHz
		Fast-mode	>0		400	kHz
		Fast-mode Plus	>0		1	MHz
t_{LOW}	SCL Low Period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_{HIGH}	SCL High Period	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{SU;STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard-mode	0			µs
		Fast-mode	0			µs
		Fast-mode Plus	0			µs
$t_{SU;DAT}$	Data set up time	Standard-mode	250			ns
		Fast -mode	100			ns
		Fast-mode Plus	50			ns
$t_{SU;STO}$	Set up time for STOP condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_r	SCL & SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
t_f	SCL & SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	pF
		Fast-mode Plus			550	pF
$t_{VD;DAT}$	Data valid time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
$t_{VD;ACK}$	Data vallid acknowledge time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
t_{SP}	Input filter	Fast-mode			50	ns
		Fast-mode Plus			50	ns

6.7 Timing Diagrams

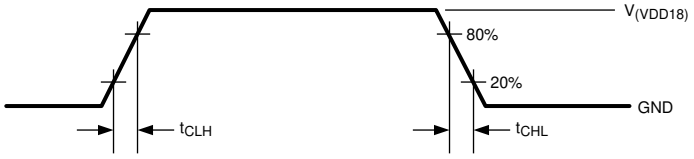


図 6-1. LVCMOS Transition Times

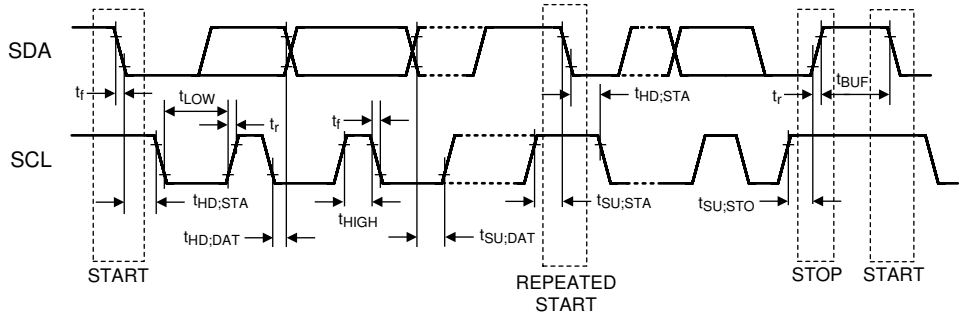


図 6-2. I²C Serial Control Bus Timing

6.8 Typical Characteristics

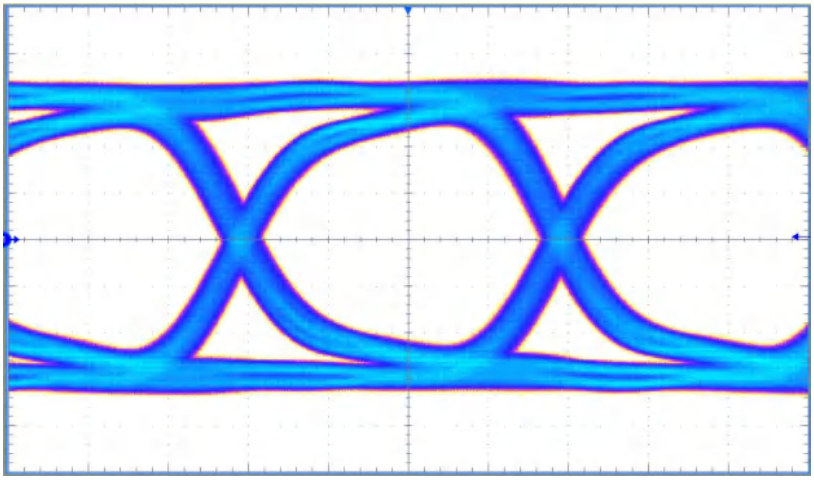


図 6-3. Eye Diagram at 4-Gbps FPD-Link III Forward Channel Rate From Serializer Output Vertical Scale: 100 mV/DIV Horizontal Scale: 62.5 ps/DIV

7 Detailed Description

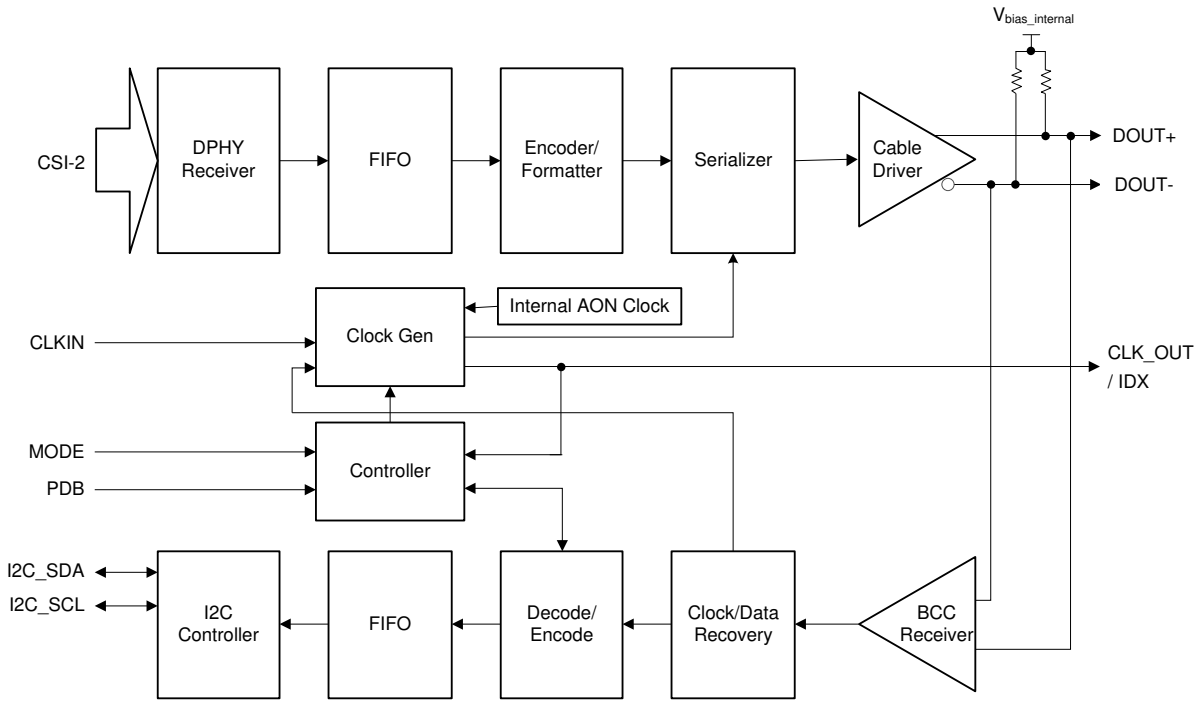
7.1 Overview

The DS90UB635-Q1 serializes data from high-resolution image sensors or other sensors using the MIPI CSI-2 interface. The DS90UB635-Q1 serializer is optimized to interface with the DS90UB63x-Q1 deserializers, the DS90UB66x-Q1 deserializers (quad hubs), as well as other potential future deserializers. The interconnect between the serializer and the deserializer can be either a coaxial cable or shielded-twisted pair (STP) cable. The DS90UB635-Q1 was designed to support multi-sensor systems such as surround view, and as such has the ability to synchronize sensors through the DS90UB63x-Q1 and DS90UB66x-Q1 hubs.

The DS90UB635-Q1 serializer and companion deserializer incorporate an I2C-compatible interface. The I2C-compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between the serializer and deserializer, as well as between remote I2C target devices.

The bidirectional control channel (BCC) is implemented through embedded signaling in the high-speed forward channel (serializer to deserializer), combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another.

7.2 Functional Block Diagram



7.3 Feature Description

The DS90UB635-Q1 FPD-Link III serializer is designed to support high-speed raw data sensors including 2-MP imagers at 60 fps, as well as 4-MP and 30-fps cameras, satellite RADAR, LIDAR, and time of flight (ToF) cameras. The chip features a forward channel capable of up to 4.16 Gbps, as well as an ultra-low latency 50-Mbps bidirectional control channel. The transmission of the forward channel, bidirectional control channel, and power is supported over coaxial (Power-over-Coax) or STP cables. The DS90UB635-Q1 features advanced data protection and diagnostic features to support ADAS and autonomous driving. Together with a companion deserializer, the DS90UB635-Q1 delivers precise multi-camera sensor clock and sensor synchronization.

7.3.1 CSI-2 Receiver

The DS90UB635-Q1 receives CSI-2 video data from the sensor. During CSI-2 operation, the D-PHY consists of a clock lane and one or more data lanes. The DS90UB635-Q1 is a target device and only supports unidirectional lane in the forward direction. Low Power Escape mode is not supported.

7.3.1.1 CSI-2 Receiver Operating Modes

During normal operation a data lane will be in either control or high-speed mode. In high-speed mode, the data transmission happens in a burst and starts and ends at a stop state (LP-11). There is a transition state to take the D-PHY from a normal mode to the low-power state.

The sequence to enter high-speed mode is: LP-11, LP-01, LP-00. After the sequence is entered, the data lane remains in high-speed mode until a stop state (LP-11) is received.

7.3.1.2 CSI-2 Receiver High-Speed Mode

During high-speed data transmission, the digital D-PHY will enable termination signal to allow proper termination of the HS RX of the Analog D-PHY, and the LP RX should stay at LP-00 state. Both CSI-2 data lane and clock lane operate in the same manner. The DS90UB635-Q1 supports both CSI-2 continuous and non-continuous clock lane modes which must be set using register 0x02[6] and should follow the image sensor clock mode. In the continuous clock lane mode, the clock lane remains in high-speed mode.

7.3.1.3 CSI-2 Protocol Layer

There are two different types of CSI-2 packets: a short packet and a long packet. Short packets have information such as the frame start/ line start, and long packets carry the data after the frame start is asserted. 図 7-1 shows the structure of the CSI-2 protocol layer with short and long packets. The DS90UB635-Q1 supports 1, 2, and 4 lane configurations.

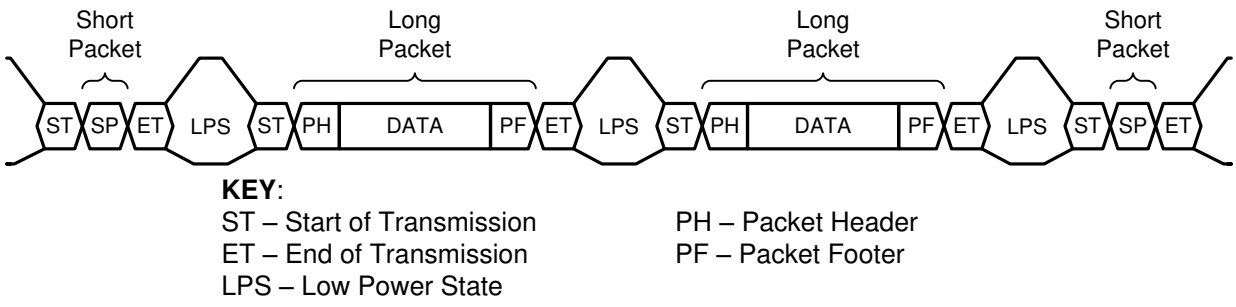


図 7-1. CSI-2 Protocol Layer With Short and Long Packets

7.3.1.4 CSI-2 Short Packet

The short packet provides frame or line synchronization. 図 7-2 shows the structure of a short packet. A short packet is identified by data types 0x00 to 0x0F.

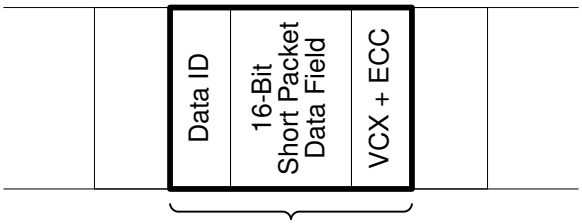


図 7-2. CSI-2 Short Packet Structure

7.3.1.5 CSI-2 Long Packet

A long packet consists of three elements: a 32-bit packet header (PH), an application-specific data payload with a variable number of 8-bit data words, and a 16-bit packet footer (PF). The packet header is further composed of three elements: an 8-bit data identifier, a 16-bit word count field, and an 8-bit ECC. The packet footer only has one element—a 16-bit checksum. 図 7-3 shows the structure of a long packet.

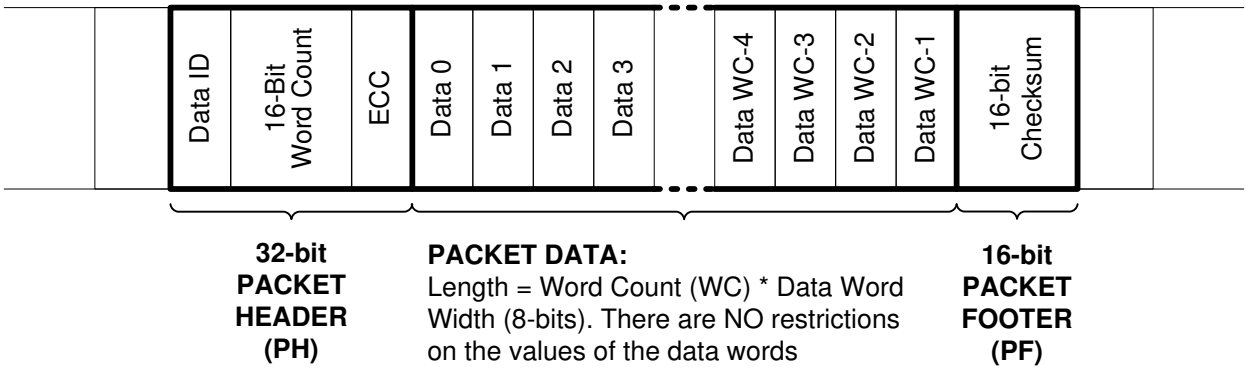


図 7-3. CSI-2 Long Packet Structure

表 7-1. CSI-2 Long Packet Structure Description

PACKET PART	FIELD NAME	SIZE (BIT)	DESCRIPTION
Header	VC / Data ID	8	Contains the virtual channel identifier and the data-type information.
	Word Count	16	Number of data words in the packet data. A word is 8 bits.
	ECC	8	ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC × 8	Application-specific payload (WC words of 8 bits).
Footer	Checksum	16	16-bit cyclic redundancy check (CRC) for packet data.

7.3.1.6 CSI-2 Errors and Detection

7.3.1.6.1 CSI-2 ECC Detection and Correction

CSI-2 packet header contains 6-bit Error Correction Code (ECC). ECC in the 32-bit long packet header can be corrected when there is a 1-bit error and detected when there is a 2-bit error. This feature is added to monitor the CSI-2 input for ECC 1-bit error correction. When ECC error is detected, ECC error detection register will be set and an alarm indicator bit can be sent to the deserializer to indicate the ECC error has been detected. A register control can be used to either enable or disable the alarm.

7.3.1.6.2 CSI-2 Check Sum Detection

A CSI-2 long packet header contains a 16-bit check sum before the end of transmission. The DS90UB635-Q1 calculates the check sum of the incoming CSI-2 data. If a check sum error is detected, the check sum error

status can be saved in the CSI_ERR_STATUS register (0x5D), then forwarded to the deserializer through the bidirectional control channel.

7.3.1.6.3 D-PHY Error Detection

DS90UB635-Q1 detect and reports SoT and SoT Sync errors.

7.3.1.6.4 CSI-2 Receiver Status

For the receive ports, several status functions can be tracked and monitored through register access. The status indications are available for error conditions as well as indications of change in line length measurements. These are available through the CSI_ERR_CNT (0x5C), CSI_ERR_STATUS (0x5D), CSI_ERR_DLANE01 (0x5E), CSI_ERR_DLANE23 (0x5F), and CSI_ERR_CLK_LANE (0x60) registers.

7.3.2 FPD-Link III Forward Channel Transmitter

The DS90UB635-Q1 features a high-speed signal transmitter capable of driving signals at rates of up to 4.16 Gbps.

7.3.2.1 Frame Format

The DS90UB635-Q1 formats the data into 40-bit long frames. Each frame is encoded to ensure DC balance and to ensure sufficient data line transitions. Each frame contains video payload data, I2C forward channel data, CRC information, framing information, and information regarding the state of the CSI-2 interface.

7.3.3 FPD-Link III Back Channel Receiver

The FPD-Link III back channel receives an encoded back channel signal over the FPD-Link III interface. The back channel frame is a 30-bit frame that contains I2C commands and GPIO data. The back channel frame receives an encoded clock and data from the deserializer, thus the data bit rate is one-half the frequency of the highest frequency received.

The back channel frequency is programmable for operation with compatible deserializers. The default setting is determined by the MODE strap pin. For operation with the DS90UB638-Q1 or DS90UB662-Q1, the back channel should be programmed for 50-Mbps operation in DS90UB635-Q1 synchronous mode and programmed for 10-Mbps operation for non-synchronous modes.

7.3.4 Serializer Status and Monitoring

The DS90UB635-Q1 features enhanced FPD-Link III diagnostics, system monitoring, and Built-In Self Test capabilities. The device monitors forward channel and back channel data for errors and reports them in the status registers. The device also supports voltage and temperature measurement for system level diagnostics. The Built-In Self Test feature allows testing of the forward channel and back channel data transmissions without external data connections.

The DS90UB635-Q1 can send alarms and sensor status data through the forward channel to monitor the CSI-2 interface, Bidirectional Control Channel (BCC), GPIO voltage sensors and internal temperature sensor. The data can then be accessed through the SENSOR_STS_X registers (0x51) to (0x54) on the compatible linked deserializer. Status bits are always transmitted, and transmission of Alarm bits needs to be enabled from registers (0x1C) to (0x1E) on the serializer.

The CSI-2 error status and alarms on the deserializer SENSOR_STS are: CSI-2 alarm, CSI-2 control error, CSI-2 synchronization error, CSI-2 start of transmission error, CSI-2 checksum error, and CSI-2 ECC 2-bit error. The status for these bits can also be read from registers (0x5D) to (0x60) on the serializer. The BCC error alarm is triggered by are BCC link detect and CRC errors which can be read from register (0x52).

The voltage sense level and voltage sense alarms correspond to Sensor V0 (0x58) and Sensor V1 (0x59). And the temperature sense levels and alarm are monitored from Sensor T (0x5A).

7.3.4.1 Forward Channel Diagnostics

The DS90UB635-Q1 monitors the status of the forward channel link. The forward channel high-speed PLL lock status is reported in the HS_PLL_LOCK bit (Register 0x52[2]). When paired with the DS90UB638-Q1 or

DS90UB662-Q1, the FPD-Link III deserializer LOCK status is also reported in the RX_LOCK_DETECT bit (Register 0x52[6]).

7.3.4.2 Back Channel Diagnostics

The DS90UB635-Q1 monitors the status of the back channel link. The back channel CRC errors are reported in the CRC_ERR bit (Register 0x52[1]). The number of CRC errors are stored in the CRC error counters and reported in the CRC_ERR_CNT1 (Register 0x55) and CRC_ERR_CNT2 (Register 0x56) registers. The CRC error counters are reset by setting the CRC_ERR_CLR (Register 0x49[3]) to 1.

When running the BIST function, the DS90UB635-Q1 reports if a BIST CRC error is detected in the BIST_CRC_ERR bit (Register 0x52[3]). The number of BIST errors are reported in the BIST_ERR_CNT field (Register 0x54). The BIST CRC error counter is reset by setting the BIST_CRC_ERR_CLR (Register 0x49[5]) to 1.

7.3.4.3 Voltage and Temperature Sensing

The DS90UB635-Q1 supports voltage measurement and temperature measurement. The temperature and voltage sensors are both equipped with a 3-bit ADC. The engineer can configure these sensors to monitor a signal and raise a flag when a signal goes outside of a set limit. For example, a voltage sensor can be used to monitor the 1.8-V line and raise a flag if the voltage goes above 1.85 V or below 1.75 V. This flag can then be transferred to the deserializer and set an interrupt at the deserializer end of the link. In a similar manner, the temperature sensor will trigger an alarm bit when the internal temperature of DS90UB635-Q1 is outside the range.

Both GPIO0 and GPIO1 can be configured to sense the voltage applied at their inputs. 表 7-32 through 表 7-38 cover the registers specific to this section.

For a given voltage or temperature, the measurement accuracy is ±1 LSB. This means that for a given input voltage or temperature corresponding to the nearest value in 表 7-2 and 表 7-3, the resulting ADC output code will be accurate to the nearest ±1 code.

表 7-2. ADC Code vs Input Voltage

GPIO VIN (V)	CODE
VIN < 0.85	000
0.85 < VIN < 0.90	001
0.90 < VIN < 0.95	010
0.95 < VIN < 1.00	011
1.00 < VIN < 1.05	100
1.05 < VIN < 1.10	101
1.10 < VIN < 1.15	110
1.15 < VIN	111

表 7-3. ADC Code vs Temperature

TEMPERATURE (°C)	CODE
T < –30	000
–30 < T < –10	001
–10 < T < 15	010
15 < T < 35	011
35 < T < 55	100
55 < T < 75	101
75 < T < 100	110
100 < T	111

7.3.4.3.1 Programming Example

This section gives an example on how to configure the DS90UB635-Q1 and DS90UB638-Q1 to monitor the voltage on the DS90UB635-Q1 GPIO1 and set an alarm, which can then assert the INT pin on the DS90UB638-Q1

```
# DS90UB635-Q1 Settings
WriteI2C(0x17,0x3E) # Enable Sensor, Select GPIO1 to sense
WriteI2C(0x18,0xB2) # Enable Sensor Gain Setting (Use Default)
WriteI2C(0x1A,0x62) # Set Sensor Upper and Lower Limits (Use Default)
WriteI2C(0x1D,0x3F) # Enable Sensor Alarms
WriteI2C(0x1E,0x7F) # Enable Sending Alarms over BCC
# Register 0x57 readout (bits 2 and 3), indicates if the voltage on the GPIO1 is below or above the
thresholds set in the register 0x1A.
# DS90UB638-Q1 Settings
WriteI2C(0x23,0x81) # Enable Interrupts, Enable Interrupts for the camera attached to RX0
WriteI2C(0x4C,0x01) # Enable Writes to RX0 registers
WriteI2C(0xD8,0x08) # Interrupt on change in Sensor Status
# Register 0x51 and 0x52  readouts indicate Sensor data. Register 0x24[7] bit readout indicates the
Alarm bit. The alarm bit can be routed to GPIO3/INT through GPIO_PIN_CTL and GPIO_OUT_SRC registers.
```

7.3.4.4 Built-In Self Test

An optional at-speed Built-In Self Test (BIST) feature supports high-speed serial link and back channel testing without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

BIST mode is enabled by the BIST configuration register 0xB3[0] on the deserializer, and should only run in the synchronous mode. When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the back channel. The serializer outputs a continuous stream of a pseudo-random sequence and drives the link at speed. The deserializer detects the test pattern and monitors the pattern for errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame. While the lock indications are required to identify the beginning of proper data reception, the best indication of any link failures or data corruption is the content of the error counter in the BIST_ERR_COUNT register 0x57 for each RX port on the deserializer side. BIST mode is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

7.3.5 FrameSync Operation

When paired with compatible deserializers, any of the DS90UB635-Q1 GPIO pins can be use for frame synchronization. This feature is useful when multiple sensors are connected to a deserializer hub. A frame synchronization signal (FrameSync) can be sent through the back channel using any of the back channel GPIOs. The FrameSync signal arrives at the serializers with limited skew.

7.3.5.1 External FrameSync

In External FrameSync mode, an external signal is input to the deserializer through one of the GPIO pins on the device. The external FrameSync signal may be propagated to one or more of the attached FPD-Link III serializers through a GPIO signal in the back channel. The expected skew timing for external FrameSync mode is on the order of one back channel frame period or 600 ns when operating at 50 Mbps.

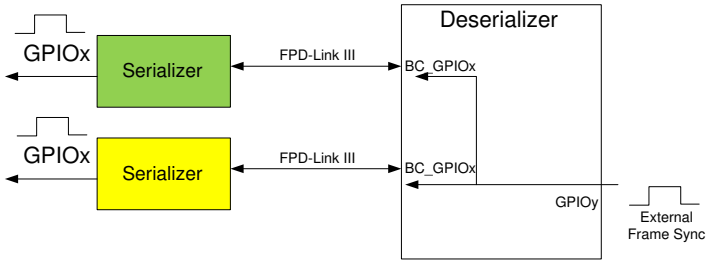


図 7-4. External FrameSync

Enabling the external FrameSync mode is done on the deserializer side. Refer to the deserializer data sheet for more information.

7.3.5.2 Internally Generated FrameSync

In Internal FrameSync mode, an internally generated FrameSync signal is sent to one or more of the attached FPD-Link III Serializers through a GPIO signal in the back channel.

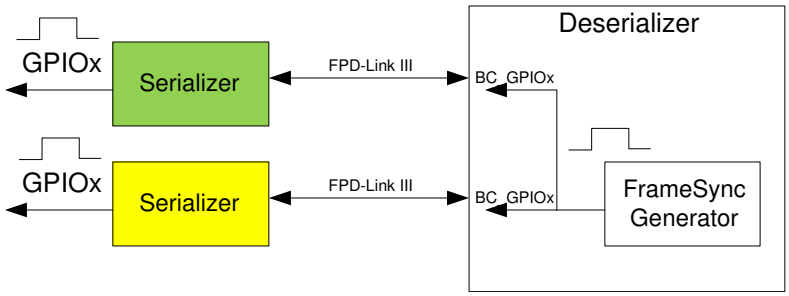


図 7-5. Internal FrameSync

FrameSync operation is controlled by the deserializer registers. Refer to the deserializer data sheet for more information.

7.3.6 GPIO Support

The DS90UB635-Q1 supports four pins, GPIO0 through GPIO3, which can be monitored, configured, and controlled through the I2C bus in registers 0x0D, 0x0E, and 0x53. These GPIOs are programmable for use in multiple situations. GPIO0 and GPIO1 have additional diagnostics functionality and may be programmed to sense external voltage levels.

7.3.6.1 GPIO Status

The status HIGH or LOW of each GPIO pin 0 through 3 may be read through the GPIO_STS bits in the GPIO_PIN_STS register 0x53. This register read operation provides the status of the GPIO pins when they are configured as an input by setting the corresponding GPIOx_INPUT_EN bits in the GPIO_INPUT_CTRL register (0x0E). To read the GPIO status when the GPIO is used as output, both GPIOx_INPUT_EN and GPIOx_OUT_EN bits in the GPIO_INPUT_CTRL register (0x0E) can be set.

表 7-4. GPIO Configuration

Configuration	Valid	Valid	Valid	Not Valid
Purpose	GPIO used as Output	GPIO used as Output	GPIO used as Input	GPIO used as Input
GPIOx_INPUT_EN	0	1(1)	1	1
GPIOx_OUT_EN	1	1	0	1
GPIO_STS	non-functional	functional	functional	N/A

注

(1) When GPIOx_INPUT_EN is set, the internal pull down will be connected to the GPIO output and the user should ensure that the pull down resistor will not interfere with the application-specific use.

7.3.6.2 GPIO Input Control

Upon initialization, GPIO0 through GPIO3 are enabled as inputs by default. The GPIO_INPUT_CTRL (0x0E) register (bits 3:0) allows control of the input enable. If a GPIO_INPUT_CTRL[3:0] bit is set to 1, then the corresponding GPIO_INPUT_CTRL[7:4] bit must be set to 0. The number of GPIOs should be set and enabled using FC_GPIO_EN in register (0x33).

7.3.6.3 GPIO Output Control

Individual GPIO output control is programmable through the GPIO_INPUT_CTRL (0x0E) register (bits 7:4) in 表 7-27. The GPIO_INPUT_CTRL[7:4] bits should be set to 1 to use the GPIOs as output pins.

7.3.6.4 Forward Channel GPIO

The input on the DS90UB635-Q1 GPIO pins can be forwarded to compatible deserializers over the FPD-Link III interface. Up to four GPIOs are supported in the forward direction.

The timing for the forward channel GPIO is dependent on the number of GPIOs assigned at the serializer. When a single GPIO input from the DS90UB635-Q1 serializer is linked to a compatible deserializer GPIO output, the value is sampled at every forward channel transmit frame. Two linked GPIO are sampled every two forward channel frames, and three or four linked GPIO are sampled every five frames. The typical latency for the GPIO is approximately 225 ns but will vary with the length of the cable. As the information is spread over multiple frames, the jitter is typically increased on the order of the sampling period (number of forward channel frames). TI recommends that the user maintain a 4x oversampling ratio for linked GPIO throughput. For example, when operating in 4-Gbps synchronous mode with REFCLK = 25 MHz, the maximum recommended GPIO input frequency based on the number of GPIO linked over the forward channel is shown in 表 7-5.

表 7-5. Forward Channel GPIO Typical Timing

NUMBER OF LINKED FORWARD CHANNEL GPIOs (FC_GPIO_EN)	SAMPLING FREQUENCY (MHz) AT FPD-Link III LINE RATE = 4 Gbps	MAXIMUM RECOMMENDED FORWARD CHANNEL GPIO FREQUENCY (MHz)	TYPICAL LATENCY (ns)	TYPICAL JITTER (ns)
1	100	25	225	12
2	50	12.5	225	24
4	20	5	225	60

7.3.6.5 Back Channel GPIO

When enabled as an output, each DS90UB635-Q1 GPIO pin can be programed to output remote data coming from the compatible deserializer using the LOCAL_GPIO_DATA register (0x0D). The maximum signal frequency that can be received over the FPD-Link III back channel is dependent on the DS90UB635-Q1 clocking mode as shown in 表 7-6.

表 7-6. Back Channel GPIO Typical Timing

DS90UB635-Q1 CLOCKING MODE	BACK CHANNEL RATE (Mbps)	SAMPLING FREQUENCY (kHz)	MAXIMUM RECOMMENDED BACK CHANNEL GPIO FREQUENCY (kHz)	TYPICAL LATENCY (µs)	TYPICAL JITTER (µs)
Synchronous Mode	50	1670	416	1.5	0.7
Non-Synchronous Modes	10	334	83.5	3.2	3
DVP Mode	2.5	83.5	20	12.2	12

7.3.7 Unique ID

Each device is programmed with a Unique DIE-ID that is burnt into devices at wafer level; Unique DIE-ID with a 16 bytes customer readable value indicating wafer lot and position of each IC inside a wafer. Combination of Unique DIE-IDs can be read and maintained by customer in a database or in a Hash table. Each system can be identified by the Unique DIE-ID programmed into the devices. Authenticity of the overall system can be established at the powerup/initialization or periodically by checking the Unique DIE-ID.

A Unique DIE-ID is programmed into each device and can be read using I2C reads. To read the Unique DIE-ID, set the IA_SEL (0xB0[4:2]) register to DIE ID Data (010), then set register IND_ACC_ADDR (0xB1) address to the Unique ID register being read, and then read the IND_ACC_DATA (0xB2) register to get the Unique DIE-ID. There are 16 Unique ID registers, each of the registers contain 8 bits of the total unique DIE-ID. The table below lists the Unique ID registers addresses.

表 7-7. Unique ID Registers

Unique ID register	IND_ACC_ADDR address
UNIQUE_ID_0	0x00
UNIQUE_ID_1	0x01
UNIQUE_ID_2	0x02
UNIQUE_ID_3	0x03
UNIQUE_ID_4	0x04
UNIQUE_ID_5	0x05
UNIQUE_ID_6	0x06
UNIQUE_ID_7	0x07
UNIQUE_ID_8	0x08
UNIQUE_ID_9	0x09
UNIQUE_ID_10	0x0A
UNIQUE_ID_11	0x0B
UNIQUE_ID_12	0x0C
UNIQUE_ID_13	0x0D
UNIQUE_ID_14	0x0E
UNIQUE_ID_15	0x0F

7.4 Device Functional Modes

7.4.1 Clocking Modes

The DS90UB635-Q1 supports several clocking schemes, which are selected through the MODE pin. In the DS90UB635-Q1, the forward channel operates at a higher bandwidth than the requirement set by the video data transported, and the forward channel data rate is set by a reference clock. The clocking mode determines what the device uses as the reference clock, and the most common configuration is synchronous mode in which no local reference oscillator is required. See 表 7-8 for more information.

The default mode of the DS90UB635-Q1 is set by the application of a bias on the MODE pin during power up. More information on setting the operation modes can be found in *セクション 7.4.2*.

表 7-8. Clocking Modes

MODE	DIVIDE	REFERENCE SOURCE	REF FREQUENCY (MHz)	FC DATA RATE	CSI BANDWIDTH ≤(4)	CLK_OUT (3)
Synchronous	N/A	Back Channel(1)	23 - 26	f × 160	f × 128	f × 160 / HS_CLK_DIV × (M/N)

表 7-8. Clocking Modes (continued)

MODE	DIVIDE	REFERENCE SOURCE	REF FREQUENCY (MHz)	FC DATA RATE	CSI BANDWIDTH ≤(4)	CLK_OUT (3)
Synchronous (Half-rate)	N/A	Back Channel(1)	11.5 - 13	f × 160	f × 128	f × 160 / HS_CLK_DIV × (M/N)
Non-Synchronous external clock	CLKIN_DIV = 1,	External Clock(2)	25 - 52	f × 80	f × 64	f × 80 / HS_CLK_DIV × (M/N)
	CLKIN_DIV = 2,	External clock (2)	50 - 104	f × 40	f × 32	f × 40 / HS_CLK_DIV × (M/N)
Non-Synchronous Internal Clock	CLKIN_DIV = 1, OSCCLK_SEL = 1	635 Internal Clock	48.4 - 51	f × 80	f × 64	N/A
Non-Synchronous Internal Clock (Half-rate)	OSCCLK_SEL = 0	635 Internal Clock	24.2 - 25.5	f × 80	f × 64	N/A
DVP External Clock Deserializer Mode: RAW10	N/A	External clock	25 - 66.5	f × 28	f × 20	f × 28 / HS_CLK_DIV × (M/N)
DVP External Clock Deserializer Mode: RAW12 HF	N/A	External clock	25 - 70	f × 28	f × 18	f × 28 / HS_CLK_DIV × (M/N)

(1) The back channel is recovered from the FPD-Link III bidirectional control channel. A local reference clock source is not required. Refer to the deserializer data sheet for the back channel frequency settings.
(2) A local reference clock source is required. Provide a clock source to the DS90UB635-Q1's CLKIN pin.
(3) HS_CLK_DIV typically should be set to either 16, 8, or 4 (default).
(4) CSI-2 lane speed must be ≥ 600Mbps/lane

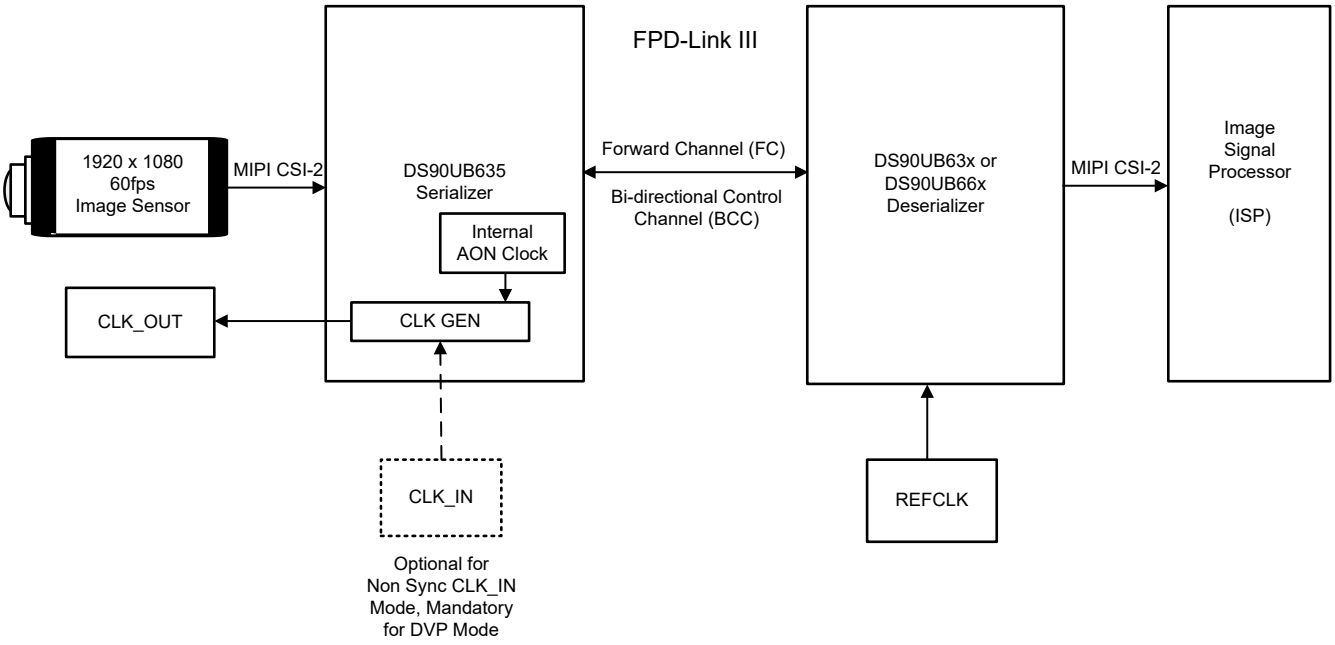


図 7-6. Clocking System Diagram

7.4.1.1 Synchronous Mode

Operation in synchronous mode offers the advantage that the receiver and all of the sensors in a multi-sensor system are locked to a common clock in the same clock domain, which reduces or eliminates the need for data buffering and resynchronization. The synchronous clocking mode also eliminates the cost, space, and potential failure point of a reference oscillator within the sensor module.

In this mode, a clock is passed from the deserializer to the serializer through the FPD-Link III back channel, and the serializer is able to use this clock both as a reference clock for an attached image sensor, as well as a reference clock for the link back to the deserializer (FPD-Link III forward channel). For operation in this mode, the DS90UB635-Q1 must be paired with a deserializer that can support this feature such as the DS90UB638-Q1 or the DS90UB662-Q1.

7.4.1.2 Non-Synchronous Clock Mode

In the non-synchronous clock mode, the external reference clock is supplied to the serializer. The serializer uses this clock to derive the FPD-Link III forward channel and an external reference clock for an attached image sensor. When in CSI-2 mode, the CSI-2 interface may be synchronous to this clock. The CSI-2 rate must be lower than the line rate. For example, with a 52-MHz clock, the FPD-Link III forward channel rate is 4.16 Gbps, and the CSI-2 throughput must be 600 Mbps to 3.328 Gbps (see 表 7-8).

7.4.1.3 Non-Synchronous Internal Mode

In the non-synchronous internal clocking mode, the serializer uses the internal Always-on Clock (AON) as the reference clock for the forward channel. The OSCCLK_SEL select must be asserted (0x05[3]=1) to enable maximum data rate when using internal clock mode, and the CLK_OUT function must be disabled. A separate reference is provided to the image sensor or ISP. The CSI-2 rate must be lower than the line rate. For example, with the internal clock of 48.4 MHz, the FPD-Link III forward channel rate is 3.872 Gbps and the CSI-2 throughput must be 600 Mbps to 3.097 Gbps (See 表 7-8).

7.4.1.4 DVP Backwards Compatibility Mode

The DS90UB635-Q1 serializer can be placed into DVP mode to be backward-compatible with the DS90UB6xx-Q1 deserializer in DVP Backwards Compatibility Mode. While the mode should have been configured using the Mode pin on the DS90UB635-Q1 serializer, the register MODE_SEL register 0x03[2:0] can be used to verify or override the current mode. This field always indicates the mode setting of the device. When bit 4 of this register is 0, this field is read-only and shows the mode setting. Mode is latched from strap value when PDB transitions LOW to HIGH, and the value should read back 101 (0x5) if the resistive strap is set correctly to DVP external clock backward-compatible mode. Alternatively, when bit 4 of this register is set to 1, the MODE field is read/write and can be programmed to 101 to assign the correct backward-compatible MODE. This is shown in 表 7-16.

CSI-2 input data provided to the DS90UB635-Q1 serializer must be synchronized to the input frequency applied to CLKIN when using DVP external clock mode. The PCLK frequency output from the DS90UB6xx-Q1 deserializer will also be related to CLKIN when in DVP external clock mode. See *Backward compatibility modes for operation with parallel output deserializers* (SNLA270) for more information.

表 7-9. List of Registers Used for DVP Configuration

REGISTER	REGISTER NAME	REGISTER DESCRIPTION
0X03	MODE_SEL	Used to override and verify strapped value, if necessary, and to configure for DVP with an external clock.
0X04	BC_MODE_SELECT	Allows DVP mode overwrites to RAW 10 or RAW 12.
0X10	DVP_CFG	Allows configuration of data in DVP mode. This includes data types like long, YUV, and specified types.
0X11	DVP_DT	Allows packets with certain data type regardless of RAW 10 or 12 mode if DVP_DT_MATCH_EN is asserted.

7.4.1.5 Configuring CLK_OUT

When using the DS90UB635-Q1 in either synchronous or non-synchronous external clock modes, CLK_OUT is intended as a reference clock for the image sensor. CLK_OUT functionality is disabled when operating in non-synchronous internal clocking mode. The frequency of the external CLK_OUT is set by (see 式 1 and 式 2).

$$CLK\_OUT = FC \times \frac{M}{HS\_CLK\_DIV \times N} \quad (1)$$

where

- FC is the forward channel data rate, and M, HS_CLK_DIV, and N are parameters set by registers 0x06 and 0x07

$$\frac{FC}{HS\_CLK\_DIV} < 1.05\ GHz \quad (2)$$

The PLL that generates CLK_OUT is a digital PLL, and as such, has very low jitter if the ratio N/M is an integer. If N/M is not an integer, then the jitter on the signal is approximately equal to HS_CLK_DIV/FC—so if it is not possible to have an integer ratio of N/M, it is best to select a smaller value for HS_CLK_DIV.

If a particular CLK_OUT frequency, such as 37.125 MHz, is required for a system, the designer can select the values M=9, N=0xF2, and HS_CLK_DIV=4 to achieve an output frequency of 37.190 MHz and a frequency error of 0.175% with an associate jitter of approximately 1 ns. Alternately, the designer could use M=1, N=0x1B, HS_CLK_DIV=4 for CLK_OUT = 37.037 MHz, and a frequency error of 0.24% for less jitter. A third alternative would be to use M=1, N=0x1B, and HS_CLK_DIV=4, but rather than using a 25.000-MHz reference clock frequency (REFCLK) for the deserializer in synchronous mode, use a frequency of 25.059 MHz. The 2x reference then fed to the DS90UB635-Q1 from the deserializer back channel will allow generating CLK_OUT = 37.124 MHz with both low jitter and a low frequency error.

7.4.2 MODE

The DS90UB635 can operate in one of many different modes. The default mode is selected by the bias voltage applied to the MODE pin during power-up. To set this voltage, a potential divider between VDD and GND is used to apply the appropriate bias After Power up, the MODE can be read, or changed through register access.

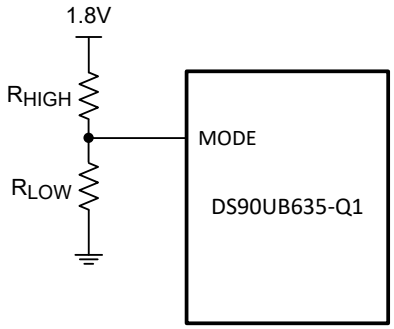


図 7-7. MODE Configuration

表 7-10. Strap Configuration Mode Select

MODE SELECT		V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		DESCRIPTION
MODE	NAME	RATIO MIN	RATIO TYP	RATIO MAX	$V_{(VDD)}$ = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	
0	Synchronous	0	0	0.133 x $V_{(VDD)}$	0	OPEN	10	CSI-2 Synchronous mode – FPD-Link III Clock reference derived from the deserializer.
2	Non-Synchronous External Clock	0.288 x $V_{(VDD)}$	0.325 x $V_{(VDD)}$	0.367 x $V_{(VDD)}$	0.586	75	35.7	CSI-2 Non-synchronous clock – FPD-Link III Clock reference derived from external clock reference input on CLKIN pin.
3	Non-Synchronous Internal Clock	0.412 x $V_{(VDD)}$	0.443 x $V_{(VDD)}$	0.474 x $V_{(VDD)}$	0.792	71.5	56.2	CSI-2 Non-synchronous – FPD-Link III Clock reference derived from internal AON clock.
5 (1)	DVP Mode	0.642 x $V_{(VDD)}$	0.673 x $V_{(VDD)}$	0.704 x $V_{(VDD)}$	1.202	39.2	78.7	DVP with External clock.

(1) The DS90UB6xx-Q1 DVP deserializers also contain a Mode pin (21). However, the mode pin on the deserializer determines the expected data format: RAW10, RAW12 LF, or RAW12 HF. Note that RAW12 LF is not supported on the DS90UB635-Q1.

7.5 Programming

7.5.1 I2C Interface Configuration

This serializer may be configured by the use of an I2C-compatible serial control bus. Multiple devices may share the serial control bus (up to two device addresses are supported). The device address is set through a resistor divider (R_{HIGH} and R_{LOW} – see Circuit to Bias IDX Pin) connected to the IDX pin.

7.5.1.1 IDX

The IDX pin configures the control interface to one of two possible device addresses—either the 1.8-V or 3.3-V referenced I2C address. A pull-up resistor and a pulldown resistor must be used to set the appropriate voltage on the IDX input pin (see below). The IDX resistor divider must be referred to Pin #25 (after the ferrite filter on the DS90UB635-Q1 pin side).

表 7-11. IDX Configuration Setting

IDX	V_{TARGET} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		I2C 8-BIT ADDRESS	I2C 7-BIT ADDRESS	$V_{(I2C)}$ (I2C I/O VOLTAGE)
	RATIO MIN	RATIO TYP	RATIO MAX	V_{VDD} = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)			
1	0	0	0.131 x $V_{(VDD18)}$	0	Open	40.2	0x30	0x18	1.8 V
2	0.178 x $V_{(VDD18)}$	0.214 x $V_{(VDD18)}$	0.256 x $V_{(VDD18)}$	0.385	180	47.5	0x32	0x19	1.8 V
3	0.537 x $V_{(VDD18)}$	0.564 x $V_{(VDD18)}$	0.591 x $V_{(VDD18)}$	1.015	82.5	102	0x30	0x18	3.3 V
4	0.652 x $V_{(VDD18)}$	0.679 x $V_{(VDD18)}$	0.706 x $V_{(VDD18)}$	1.223	68.1	137	0x32	0x19	3.3 V

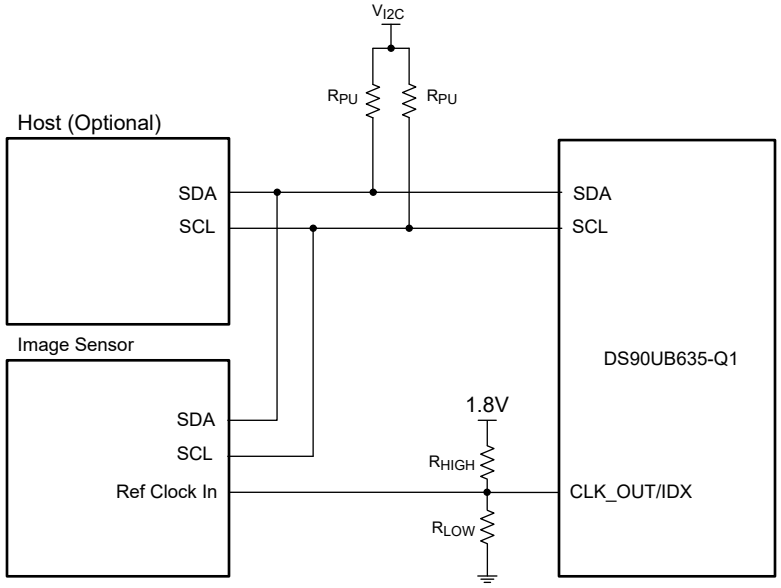


図 7-8. Circuit to Bias IDX Pin

7.5.2 I2C Interface Operation

The serial control bus consists of two signals: SCL and SDA. SCL is a Serial Bus Clock Input / Output signal and the SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to V_{I2C}, chosen to be either 1.8 V or 3.3 V.

For the standard and fast I2C modes, a pullup resistor of R_{PU} = 4.7 kΩ is recommended, while a pullup resistor of R_{PU} = 470 Ω is recommended for the fast plus mode. However, the pullup resistor value may be additionally

adjusted for capacitive loading and data rate requirements. The signals are either pulled High or driven Low. The IDX pin configures the control interface to one of two possible device addresses. A pullup resistor (R_{HIGH}) and a pulldown resistor (R_{LOW}) may be used to set the appropriate voltage on the IDX input pin.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions Low while SCL is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See 図 7-9.

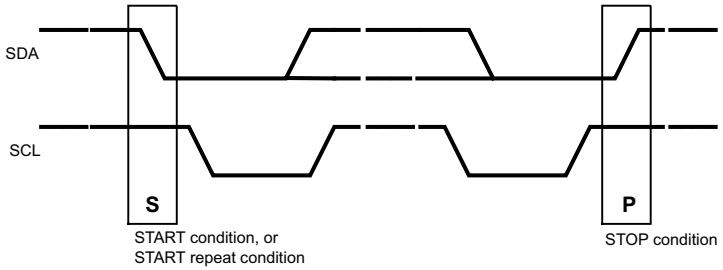


図 7-9. Start and Stop Conditions

To communicate with an I2C target, the host controller (controller) sends data to the target address and waits for a response. This response is referred to as an acknowledge bit (ACK). If a target on the bus is addressed correctly, the target Acknowledges (ACKs) the controller by driving the SDA bus low. If the address does not match a target address of the device, the target Not-acknowledges (NACKs) the controller by pulling the SDA High. ACKs also occur on the bus when data is being transmitted. When the controller is writing data, the target ACKs after every data byte is successfully received. When the controller is reading data, the controller ACKs after every data byte is received to let the target know that the controller wants to receive another data byte. When the controller wants to stop reading, the controller NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a start condition or a repeated start condition. All communication on the bus ends with a stop condition. A READ is shown in 図 7-10 and a WRITE is shown in 図 7-11.

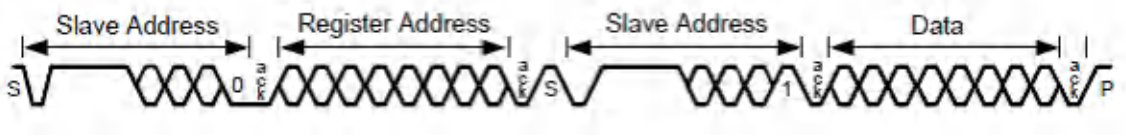


図 7-10. I2C Bus Read

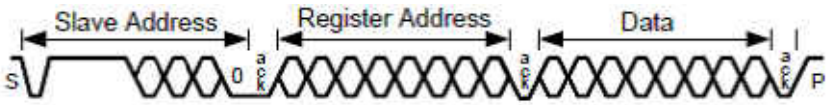


図 7-11. I2C Bus Write

Any I2C controller located at the serializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to the TI application note *I2C communication over FPD-Link III with bidirectional control channel* (SNLA131).

7.5.3 I2C Timing

The proxy controller timing parameters are based on the internal reference clock. The I2C controller regenerates the I2C read or write access using timing controls in registers 0x0B and 0x0C to regenerate the clock and data signals to meet the desired I2C timing in standard, fast, or fast-plus modes of operation.

I2C controller SCL high time is set in register 0x0B. This field configures the high pulse width of the SCL output when the serializer is the controller on the local I2C bus. The default value is set to provide a minimum 5-µs SCL high time with the internal reference clock at 26.25 MHz including five additional oscillator clock periods or

synchronization and response time. Units are 38.1 ns for the nominal oscillator clock frequency, giving Min_delay = 38.1 ns × (SCL_HIGH_TIME + 5).

I2C controller SCL low time is set in register 0x0C. This field configures the low pulse width of the SCL output when the serializer is the controller on the local deserializer I2C bus. This value is also used as the SDA setup time by the I2C target for providing data prior to releasing SCL during accesses over the bidirectional control channel. The default value is set to provide a minimum 5-µs SCL high time with the reference clock at 26.25 MHz including five additional oscillator clock periods or synchronization and response time. Units are 38.1 ns for the nominal oscillator clock frequency, giving Min_delay = 38.1 ns × (SCL_HIGH_TIME + 5). See 表 7-12 example settings for standard mode, fast mode, and fast mode plus timing.

表 7-12. Typical I2C Timing Register Settings

I2C MODE	SCL HIGH TIME		SCL LOW TIME	
	0x0B	NOMINAL DELAY	0x0C	NOMINAL DELAY
Standard	0x7F	5.03 µs	0x7F	5.03 µs
Fast	0x13	0.914 µs	0x26	1.64 µs
Fast - Plus	0x06	0.419 µs	0x0B	0.648 µs

7.6 Pattern Generation

The DS90UB635-Q1 supports an internal pattern generation feature to provide a simple way to generate video test patterns for the CSI-2 transmitter outputs. Two types of patterns are supported: Reference color bar patterns and fixed color patterns accessed by the pattern generator page 0 in the indirect register set.

7.6.1 Reference Color Bar Pattern

The reference color bar patterns are based on the pattern defined in Appendix D of the mipi_CTS_for_D-PHY_v1-1_r03 specification. The pattern is an 8-color bar pattern designed to provide high, low, and medium frequency outputs on the CSI-2 transmit data lanes.

The CSI-2 reference pattern provides 8 color bars by default with the following byte data for the color bars: X bytes of 0xAA (high-frequency pattern, inverted), X bytes of 0x33 (mid-frequency pattern), X bytes of 0xF0 (low-frequency pattern, inverted), X bytes of 0x7F (lone 0 pattern), X bytes of 0x55 (high-frequency pattern), X bytes of 0xCC (mid-frequency pattern, inverted), X bytes of 0x0F (low-frequency pattern), and Y bytes of 0x80 (long 1 pattern). In most cases, Y will be the same as X. For certain data types, the last color bar may need to be larger than the others to properly fill the video line dimensions.

The pattern generator is programmable with the following options:

- Number of color bars (1, 2, 4, or 8)
- Number of bytes per line
- Number of bytes per color bar
- CSI-2 datatype field and VC-ID
- Number of active video lines per frame
- Number of total lines per frame (active plus blanking)
- Line period (possibly program in units of 10 ns)
- Vertical front porch – number of blank lines prior to the FrameEnd packet
- Vertical back porch – number of blank lines following the FrameStart packet

The pattern generator relies on proper programming by software to ensure the color bar widths are set to multiples of the block (or word) size required for the specified datatype. For example, for RGB888, the block size is 3 bytes which also matches the pixel size. In this case, the number of bytes per color bar must be a multiple of 3. The pattern generator is implemented in the CSI-2 transmit clock domain, providing the pattern directly to the CSI-2 transmitter. The circuit generates the CSI-2 formatted data.

7.6.2 Fixed Color Patterns

When programmed for fixed color pattern mode, the pattern generator can generate a video image with a programmable fixed data pattern. The basic programming fields for image dimensions are the same as used with

the color bar patterns. When sending fixed color patterns, the color bar controls allow the user to alternate between the fixed pattern data and the bit-wise inverse of the fixed pattern data.

The fixed color patterns assume a fixed block size for the byte pattern. The block size is programmable through a register and is designed to support most 8-bit, 10-bit, and 12-bit pixel formats. The block size should be set based on the pixel size converted to blocks that are an integer multiple of bytes. For example, an RGB888 pattern would consist of 3-byte pixels and would therefore require a 3-byte block size. A 2x12-bit pixel image would also require 3-byte block size, while a 3x12-bit pixel image would require 9 bytes (2 pixels) to send an integer number of bytes. Sending a RAW10 pattern typically requires a 5-byte block size for 4 pixels, so 1x10-bit and 2x10-bit could both be sent with a 5-byte block size. For 3x10-bit, a 15-byte block size would be required.

The fixed color patterns support block sizes up to 16 bytes in length, allowing additional options for patterns in some conditions. For example, an RGB888 image could alternate between four different pixels by using a twelve-byte block size. An alternating black and white RGB888 image could be sent with a block size of 6-bytes by setting the first three bytes to 0xFF and the next three bytes to 0x00.

To support up to 16-byte block sizes, a set of sixteen registers are implemented to allow programming the value for each data byte.

7.6.3 Packet Generator Programming

The information in this section provides details on how to program the pattern generator to provide a specific color bar pattern, based on datatype, frame size, and line size.

Most basic configuration information is determined directly from the expected video frame parameters. The requirements should include the datatype, frame rate (frames per second), number of active lines per frame, number of total lines per frame (active plus blanking), and number of pixels per line.

- PGEN_ACT_LPF – Number of active lines per frame
- PGEN_TOT_LPF – Number of total lines per frame
- PGEN_LSIZE – Video line length size in bytes. Compute based on pixels per line multiplied by pixel size in bytes
- CSI-2 DataType field and VC-ID.
- Optional: PGEN_VBP – Vertical back porch. This is the number of lines of vertical blanking following Frame Valid.
- Optional: PGEN_VFP – Vertical front porch. This is the number of lines of vertical blanking preceding Frame Valid.
- PGEN_LINE_PD – Line period in 10-ns units. Compute based on Frame Rate and total lines per frame.
- PGEN_BAR_SIZE – Color bar size in bytes. Compute based on datatype and line length in bytes (see details below).

7.6.3.1 Determining Color Bar Size

The color bar pattern should be programmed in units of a block or word size dependent on the datatype of the video being sent. The sizes are defined in the MIPI CSI-2 specification. For example, RGB888 requires a 3-byte block size which is the same as the pixel size. RAW10 requires a 5-byte block size which is equal to 4 pixels. RAW12 requires a 3-byte block size which is equal to 2 pixels.

When programming the Pattern Generator, software should compute the required bar size in bytes based on the line size and the number of bars. For the standard 8-color bar pattern, that would require the following algorithm:

- Select the desired datatype, and a valid length for that datatype (in pixels).
- Convert pixels/line to blocks/line (by dividing by the number of pixels/block, as defined in the datatype specification).
- Divide the blocks/line result by the number of color bars (8), giving blocks/bar.
- Round result down to the nearest integer.
- Convert blocks/bar to bytes/bar and program that value into the PGEN_BAR_SIZE register.

As an alternative, the blocks/line can be computed by converting pixels/line to bytes/line and dividing by bytes/block.

7.6.4 Code Example for Pattern Generator

```
#Patgen RGB888 1920x1080p30 Fixed 8 Colorbar
WriteI2C(0xB0,0x00) # Indirect Pattern Gen Registers
WriteI2C(0xB1,0x01) # PGEN_CTL
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x02) # PGEN_CFG
WriteI2C(0xB2,0x33)
WriteI2C(0xB1,0x03) # PGEN_CSI_DI
WriteI2C(0xB2,0x24) # RGB888
WriteI2C(0xB1,0x04) # PGEN_LINE_SIZE1
WriteI2C(0xB2,0x16)
WriteI2C(0xB1,0x05) # PGEN_LINE_SIZE0
WriteI2C(0xB2,0x80)
WriteI2C(0xB1,0x06) # PGEN_BAR_SIZE1
WriteI2C(0xB2,0x02)
WriteI2C(0xB1,0x07) # PGEN_BAR_SIZE0
WriteI2C(0xB2,0xD0)
WriteI2C(0xB1,0x08) # PGEN_ACT_LPF1
WriteI2C(0xB2,0x04)
WriteI2C(0xB1,0x09) # PGEN_ACT_LPF0
WriteI2C(0xB2,0x38)
WriteI2C(0xB1,0x0A) # PGEN_TOT_LPF1
WriteI2C(0xB2,0x04)
WriteI2C(0xB1,0x0B) # PGEN_TOT_LPF0
WriteI2C(0xB2,0x65)
WriteI2C(0xB1,0x0C) # PGEN_LINE_PD1
WriteI2C(0xB2,0x0B)
WriteI2C(0xB1,0x0D) # PGEN_LINE_PD0
WriteI2C(0xB2,0x93)
WriteI2C(0xB1,0x0E) # PGEN_VBP
WriteI2C(0xB2,0x21)
WriteI2C(0xB1,0x0F) # PGEN_VFP
WriteI2C(0xB2,0x0A)
```

7.7 Register Maps

In the register definitions under the *TYPE* and *DEFAULT* heading, the following definitions apply:

- R = Read only access
- R/W = Read / Write access
- R/RC = Read only access, Read to Clear
- (R/W)/SC = Read / Write access, Self-Clearing bit
- (R/W)/S = Read / Write access, Set based on strap pin configuration at start-up
- LL = Latched Low and held until read
- LH = Latched High and held until read
- S = Set based on strap pin configuration at start-up

7.7.1 I2C Device ID Register

表 7-13. Device ID Register (Address 0x00)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	DEVICE_ID	S, R/W	S	7-bit I2C ID of Serializer. This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and shows the strapped ID. When bit 0 of this register is 1, this field is read/write and can be used to assign any valid I2C ID.
0	SER_ID_OVERRIDE	R/W	0x0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value

7.7.2 Reset

表 7-14. RESET_CTL Register (Address 0x01)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R/W	0x00	Reserved.
2	RESTART_AUTOLOAD	(R/W)/SC	0x0	Restart ROM Auto-load. Setting this bit to 1 causes a reload of the ROM. This bit is self-clearing.
1	DIGITAL_RESET_1	(R/W)/SC	0x0	Digital Reset 1. Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
0	DIGITAL_RESET_0	(R/W)/SC	0x0	Digital Reset 0. Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

7.7.3 General Configuration

表 7-15. General_CFG (Address 0x02)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6	CONTS_CLK	R/W	0x0	CSI-2 Clock Lane Configuration. 0 : Non Continuous Clock 1 : Continuous Clock
5:4	CSI_LANE_SEL	R/W	0x3	CSI-2 Data lane configuration. 00: 1-lane configuration 01: 2-lane configuration 11: 4-lane configuration
3:2	RESERVED	R/W	0x0	Reserved.

表 7-15. General_CFG (Address 0x02) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
1	CRC_TX_GEN_ ENABLE	R/W	0x1	Transmitter CRC Generator. 0: Disable 1: Enable
0	I2C_STRAP_MODE	S, R/W	S	I2C Strap Mode. This field indicates the I2C voltage level of the device. Upon device start-up, this field will display the I2C voltage level setting from the strapped IDX pin. This field is write capable and can be used to assign the I2C voltage level. Programming this bit to change the I2C voltage level should only be performed remotely over the back channel from a connected deserializer. 0: 3.3 V 1: 1.8 V

7.7.4 Forward Channel Mode Selection

表 7-16. MODE_SEL (Address 0x03)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6	RESERVED	S, R	S	Reserved.
5	RESERVED	R/W	0x0	Reserved.
4	MODE_OV	R/W	0x0	0: Serializer Mode from the strapped MODE pin 1: Register Mode overrides strapped value
3	MODE_DONE	R	0x0	Indicates MODE value has stabilized and been latched.
2:0	MODE	S, R/W	S	This field always indicates the MODE setting of the device. When bit 4 of this register is 0, this field is read-only and shows the Mode Setting. When bit 4 of this register is 1, this field is read/write and can be used to assign MODE. Mode is latched from strap value when PDB transitions LOW to HIGH. Mode of operation: 000: CSI-2 Synchronous Mode 001: Reserved 010: CSI-2 Non-synchronous external clock Mode (Requires a local clock source) 011: CSI-2 Non-synchronous Internal AON Clock 101: DVP External Clock Backward-Compatible Mode (Requires local clock source)

7.7.5 BC_MODE_SELECT

表 7-17. BC_MODE_SELECT (Address 0x04)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R/W	0x0	Reserved.
2	MODE_OVERWRITE _100m	R/W	0x0	28-bit RAW 10 Mode operation. Backward-compatible RAW 10 DVP mode (28-bit) is automatically configured by the Bidirectional Control Channel once RX lock has been detected. Software may overwrite the value, but must also set the DVP_MODE_OVER_EN to prevent overwriting by the Bidirectional Control Channel.
1	MODE_OVERWRITE _75m	R/W	0x0	28-bit RAW 12 Mode operation. Backward-compatible RAW 12 HF DVP mode (28-bit) is automatically configured by the Bidirectional Control Channel once RX lock has been detected. Software may overwrite the value, but must also set the DVP_MODE_OVER_EN to prevent overwriting by the Bidirectional Control Channel.
0	DVP_MODE_OVER_ EN	R/W	0x0	Prevent auto-loading of the backward-compatible DVP mode (28-bit) operation by the Bidirectional Control Channel.

7.7.6 PLL Clock Control

表 7-18. PLLCLK_CTRL Register (Address 0x05)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:4	CLKIN_DIV	R/W	0x0	CLKIN clock divide ratio to generate internal reference. 3'b000 : CLKIN Div by 1 3'b001 : CLKIN Div by 2 3'b010 : CLKIN Div by 4 3'b011 : CLKIN Div by 8 3'b100 - 3'b111 : RESERVED
3	OSCCLK_SEL	R/W	0x0	Internally generated OSC clock reference when operating with Non-Synchronous internal clock or external system clock not detected. 0: 24.2 MHz to 25.5 MHz, set for 2 Gbps line rate 1: 48.4 MHz to 51 MHz, set for 4 Gbps line rate mode.
2:0	RESERVED	R/W	0x3	Reserved.

7.7.7 Clock Output Control 0

The DS90UB635-Q1 provides an option for a programmable reference output clock to meet the system clock input requirements of various sensors. The control of the clock output frequency is set by the input divider and M value in register 0x06 and the N value in register 0x07.

表 7-19. CLKOUT_CTRL0 (Address 0x06)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	HS_CLK_DIV	R/W	0x2	Clock source of M/N divider is based on the forward channel data rate divided by this register field. 000: Div by 1 001: Div by 2 010: Div by 4 011: Div by 8 100: Div by 16
4:0	DIV_M_VAL	R/W	0x01	M value for M/N divider for CLKOUT. CLKOUT can be programmed using the M/N ratio of an internal high-speed clock to generate a clock output based on the system sensor requirement. When selecting the M/N ratio, they should be set to yield the CLKOUT frequency less than 100 MHz. The M value should be ≥ 0. Setting M to 0 will disable CLKOUT and output will remain static high or low.

7.7.8 Clock Output Control 1

The DS90UB635-Q1 provides option for a programmable reference output clock to meet the system clock input requirements of various sensors. The control of the clock output frequency is set by the input divider and M value in register 0x06 and the N value in register 0x07.

表 7-20. CLKOUT_CTRL1 (Address 0x07)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	DIV_N_VAL	R/W	0x28	N value for M/N divider for CLKOUT. CLKOUT can be programmed using the M/N ratio of an internal high-speed clock to generate a clock output based on the system sensor requirement. When selecting the M/N ratio, they should be set to yield the CLKOUT frequency less than 100 MHz. N must be set to non-zero value.

7.7.9 Back Channel Watchdog Control

表 7-21. BCC_WATCHDOG (Address 0x08)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	BCC_WD_TIMER	R/W	0x7F	BCC_WD_TIMER sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0. The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time.
0	BCC_WD_TIMER_ DISABLE	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer. 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

7.7.10 I2C Control 1

表 7-22. I2C_CONTROL1 (Address 0x09)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	LCL_WRITE_ DISABLE	R/W	0x0	Disable Remote Writes to Local Registers. Setting this bit to a 1 prevents remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C controller attached to the deserializer. Setting this bit does not affect remote access to I2C targets at the Serializer.
6:4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time. This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xE	I2C Glitch Filter Depth. This field configures the maximum width of glitch pulses on the SCL and SDA inputs that are rejected. Units are 5 nanoseconds.

7.7.11 I2C Control 2

表 7-23. I2C_CONTROL2 (Address 0x0A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	SDA_OUTPUT_ SETUP	R/W	0x1	Remote Ack SDA Output Setup. When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value increases setup time in units of 640 ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80 ns.
3:2	SDA_OUTPUT_DELA Y	R/W	0x0	SDA Output Delay. This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value increases output delay in units of 40 ns. Nominal output delay values for SCL to SDA are: 00 : 240 ns 01: 280 ns 10: 320 ns 11: 360 ns
1	I2C_BUS_TIMER_ SPEEDUP	R/W	0x0	Speed up I2C Bus Watchdog Timer. 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER_ DISABLE	R/W	0x0	Disable I2C Bus Watchdog Timer. When the I2C Bus Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus is assumed free. If SDA is low and no signaling occurs, the device attempts to clear the bus by driving 9 clocks on SCL.

7.7.12 SCL High Time

表 7-24. SCL_HIGH_TIME (Address 0x0B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SCL_HIGH_TIME	R/W	0x7F	I2C Controller SCL High Time. This field configures the high pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. Units are 38.1 ns for the nominal oscillator clock frequency of 26.25 MHz. The default value is set to provide a minimum 5-µs SCL high time with the internal oscillator clock running at 26.25 MHz. Delay includes 5 additional oscillator clock periods. Min_delay = 38.0952 ns × (SCL_HIGH_TIME + 5)

7.7.13 SCL Low Time

表 7-25. SCL_LOW_TIME (Address 0x0C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SCL_LOW_TIME	R/W	0x7F	I2C SCL Low Time. This field configures the low pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 38.1 ns for the nominal oscillator clock frequency of 26.25 MHz. The default value is set to provide a minimum 5-µs SCL low time with the internal oscillator clock running at 26.25 MHz. Delay includes 5 additional clock periods. Min_delay = 38.0952 ns × (SCL_LOW_TIME + 5)

7.7.14 Local GPIO DATA

表 7-26. LOCAL_GPIO_DATA (Address 0x0D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	GPIO_RMTEN	R/W	0xF	Enable remote deserializer GPIO data on local GPIO. Bit 7: Enable remote GPIO3 when this bit is set to 1 Bit 6: Enable remote GPIO2 when this bit is set to 1 Bit 5: Enable remote GPIO1 when this bit is set to 1 Bit 4: Enable remote GPIO0 when this bit is set to 1
3:0	GPIO_OUT_SRC	R/W	0x0	GPIO Output Source. This register sets the logical output of 4 GPIOs, GPIO_RMTEN must be disabled and GPIOx_OUT_EN must be enabled. Bit 3: write 0/1 on GPIO3 Bit 2: write 0/1 on GPIO2 Bit 1: write 0/1 on GPIO1 Bit 0: write 0/1 on GPIO0

7.7.15 GPIO Input Control

表 7-27. GPIO_INPUT_CTRL (Address 0x0E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	GPIO3_OUT_EN	R/W	0x0	GPIO3 Output Enable. 0: Disabled 1: Enabled
6	GPIO2_OUT_EN	R/W	0x0	GPIO2 Output Enable. 0: Disabled 1: Enabled
5	GPIO1_OUT_EN	R/W	0x0	GPIO1 Output Enable. 0: Disabled 1: Enabled
4	GPIO0_OUT_EN	R/W	0x0	GPIO0 Output Enable. 0: Disabled 1: Enabled

表 7-27. GPIO_INPUT_CTRL (Address 0x0E) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable. 0: Disabled 1: Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable. 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable. 0: Disabled 1: Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable. 0: Disabled 1: Enabled

7.7.16 DVP_CFG

表 7-28. DVP_CFG (Address 0x10)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R/W	0x0	Reserved.
4	DVP_DT_ANY_EN	R/W	0x0	When asserted, allows any packet with a Long data type (DT) packet through DVP.
3	DVP_DT_MATCH_EN	R/W	0x0	When asserted, allows data type matching based on the value in the DVP_DT register. Note: When this bit is asserted, writes to the DVP_DT register are blocked.
2	DVP_DT_YUV_EN	R/W	0x0	When asserted, allows YUV 10-bit DTs through DVP when mode_100m is also asserted (YUV 10-bit DTs are 0x19, 0x1d, and 0x1f).
1	DVP_FV_IN	R/W	0x0	Invert Frame Valid Polarity.
0	DVP_LV_INV	R/W	0x0	Invert Line Valid Polarity.

7.7.17 DVP_DT

表 7-29. DVP_DT (Address 0x11)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R/W	0x0	Reserved.
5:0	DVP_DT_MATCH_VAL	R/W	0x0	When the DVP_DT_MATCH_EN bit in register DVP_CFG (0x10) is asserted, the DVP block will allow packets with this DT through regardless of the mode_75m or mode_100m setting. The DT value must be a Long DT value (either bit 5 or 4 must be set) for a match to occur.

7.7.18 Force BIST Error

表 7-30. FORCE_BIST_ERR (Address 0x13)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	FORCE_FC_ERR	SC	0x0	FORCE_ERR_CNT allows forcing a number of forward channel parity errors based on the value in FORCE_FC_CNT. When in BIST mode, the parity errors will be generated automatically upon entering BIST mode. When in normal operation this bit must be set to one to inject the parity errors. 0: Force Disabled 1: Force Enabled
6:0	FORCE_FC_CNT	R/W	0x00	Force Error Count. Set this value to the desired number of forced parity errors.

7.7.19 Remote BIST Control

表 7-31. REMOTE_BIST_CTRL (Address 0x14)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	FORCE_ERR_CNT	R/W	0x0	Set to force FC error based on the FORCE_ERR_CNT. 0: Force Disabled 1: Force Enabled
3	LOCAL_BIST_EN	R/W	0x0	Force DS90UB635-Q1 to Enter BIST Mode.
2:1	BIST_CLOCK	R/W	0x0	BIST clock source selection. 00: External/System clock 01: 50 MHz internal clock 1X: 25 MHz internal clock
0	REMOTE_BIST_EN	R/W	0x0	Backward-Compatible Remote BIST Enable Register.

7.7.20 Sensor Voltage Gain

表 7-32. SENSOR_VGAIN (Address 0x15)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:0	VOLT_GAIN	R/W	0x20	Voltage Sensor Gain Setting. VOLT_GAIN = (128 / REG_VALUE). 0x40 = Gain of 2 0x20 = Gain of 4 0x10 = Gain of 8

7.7.21 Sensor Temp Gain

表 7-33. SENSOR_TGAIN (Address 0x16)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:0	TEMP_GAIN	R/W	0x18	Temperature Sensor Gain Setting. 128/TEMP_GAIN

7.7.22 Sensor Control 0

表 7-34. SENSOR_CTRL0 (Address 0x17)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	R/W	0x3	Reserved.
3:2	SENSOR_ENABLE	R/W	0x3	Temperature and Voltage Sensor Enable. 00: Disabled 11: Enabled
1:0	SENSE_V_GPIO	R/W	0x0	Enable GPIO 0/1 for input Voltage Sensor 0/1 measurement. 00: No voltage sensing 01: GPIO0 Voltage Sensing 10: GPIO1 Voltage Sensing 11: GPIO0 and GPIO1 Voltage Sensing

7.7.23 Sensor Control 1

表 7-35. SENSOR_CTRL1 (Address 0x18)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	SENSE_GAIN_EN	R/W	0x1	Enable Gain Setting of the Sensor.
6:0	RESERVED	R/W	0x00	Reserved.

7.7.24 Voltage Sensor 0 Thresholds

表 7-36. SENSOR_V0_THRESH (Address 0x19)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:4	SENSE_V0_HI	R/W	0x6	GPIO0/V0 sensor upper limit. When the GPIO0 is configured as a voltage sensor, and the voltage measured is above the SENSE_V0_HI, it triggers the V0_SENSOR_HI alarm in the SENSOR_STATUS register. The max reading can be read from VOLTAGE_SENSOR_V0_MAX.
3	RESERVED	R/W	0x0	Reserved.
2:0	SENSE_V0_LO	R/W	0x2	GPIO0/V0 sensor lower limit. When the GPIO0 is configured as a voltage sensor, and the voltage measured is below the SENSE_V0_LO, it triggers the V0_SENSOR_LOW alarm in the SENSOR_STATUS register. The min reading can be read from VOLTAGE_SENSOR_V0_MIN.

7.7.25 Voltage Sensor 1 Thresholds

表 7-37. SENSOR_V1_THRESH (Address 0x1A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:4	SENSE_V1_HI	R/W	0x6	GPIO1/V1 alarm upper limit. When the GPIO1 is configured as a voltage sensor, V1_MAX sets the upper limit for V1_SENSOR_HI status to be triggered.
3	RESERVED	R/W	0x0	Reserved.
2:0	SENSE_V1_LO	R/W	0x2	GPIO1/V1 alarm lower limit. When the GPIO1 is configured as a voltage sensor, V1_MIN sets the lower limit for V1_SENSOR_LOW status to be triggered.

7.7.26 Temperature Sensor Thresholds

表 7-38. SENSOR_T_THRESH (Address 0x1B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:4	SENSE_T_HI	R/W	0x6	Temp sensor upper threshold. When the Temp sensor is enabled, and the temperature measured above the SENSE_T_HI limit, it triggers the T_SENSOR_HI alarm in SENSOR_STATUS.
3	RESERVED	R/W	0x0	Reserved.
2:0	SENSE_T_LO	R/W	0x2	Temp sensor lower threshold. When the Temp sensor is enabled, and the temperature measured below the SENSE_T_LO limit, it triggers the T_SENSOR_LOW alarm in SENSOR_STATUS.

7.7.27 CSI-2 Alarm Enable

表 7-39. ALARM_CSI_EN (Address 0x1C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R/W	0x0	Reserved.
5	CSI_NO_FV_EN	R/W	0x1	CSI-2 No Frame Valid Alarm Enable. 1: Enabled 0: Disabled
4	DPHY_SYNC_ERR_EN	R/W	0x1	DPHY_SYNC_ERR Alarm Enable. 1: Enabled 0: Disabled
3	DPHY_CTRL_ERR_EN	R/W	0x1	DPHY_CTRL_ERR Alarm Enable. 1: Enabled 0: Disabled

表 7-39. ALARM_CSI_EN (Address 0x1C) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
2	CSI_ECC_2_EN	R/W	0x1	CSI_ECC2 Alarm Enable. 1: Enabled 0: Disabled
1	CSI_CHKSUM_ERR_EN	R/W	0x1	CSI-2 Checksum Error Alarm Enable. 1: Enabled 0: Disabled
0	CSI_LENGTH_ERR_EN	R/W	0x1	CSI-2 Length Error Alarm Enable. 1: Enabled 0: Disabled

7.7.28 Alarm Sense Enable

表 7-40. ALARM_SENSE_EN (Address 0x1D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R/W	0x0	Reserved.
5	T_OVER	R/W	0x0	Enable Temp Sensor over the high limit alarm.
4	T_UNDER	R/W	0x0	Enable Temp Sensor under the low limit alarm.
3	V1_OVER	R/W	0x0	Enable Voltage1 Sensor over the high limit alarm.
2	V1_UNDER	R/W	0x0	Enable Voltage1 Sensor under the low limit alarm.
1	V0_OVER	R/W	0x0	Enable Voltage0 Sensor over the high limit alarm.
0	V0_UNDER	R/W	0x0	Enable Voltage0 Sensor under the low limit alarm.

7.7.29 Back Channel Alarm Enable

表 7-41. ALARM_BC_EN (Address 0x1E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
1	CRC_ERR_EN	R/W	0x0	Enable CRC_ERR alarm.
0	LINK_DETECT_EN	R/W	0x0	Enable LINK_DETECT alarm.

7.7.30 CSI-2 Polarity Select

The CSI-2 Polarity Select register allows for changing P/N input polarity for each data lane.

表 7-42. CSI_POL_SEL (Address 0x20)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R	0x0	Reserved.
4	POLARITY_CLK0	R/W	0x0	CSI-2 CLK lane 0 Polarity.
3	POLARITY_D3	R/W	0x0	CSI-2 Data lane 3 Polarity.
2	POLARITY_D2	R/W	0x0	CSI-2 Data lane 2 Polarity.
1	POLARITY_D1	R/W	0x0	CSI-2 Data lane 1 Polarity.
0	POLARITY_D0	R/W	0x0	CSI-2 Data lane 0 Polarity.

7.7.31 CSI-2 LP Mode Polarity

The CSI-2 LP Mode Polarity register allows for changing polarity for all clocks and data lanes in Low power mode.

表 7-43. CSI_LP_POLARITY (Address 0x21)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R/W	0x0	Reserved.
4	POL_LP_CLK0	R/W	0x0	LP CSI-2 Clock lane Polarity.

表 7-43. CSI_LP_POLARITY (Address 0x21) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3:0	POL_LP_DATA	R/W	0x0	LP CSI-2 Data lane Polarity.

7.7.32 CSI-2 High-Speed RX Enable

The CSI-2 High Speed RX Enable register is intended for system debugging and should be set to 0x00 for normal operation.

表 7-44. CSI_EN_HSRX (Address 0x22)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved.
6:0	RESERVED	R/W	0x00	Reserved.

7.7.33 CSI-2 Low Power Enable

The CSI-2 Low Power Enable register is intended for system debugging.

表 7-45. CSI_EN_LPRX (Address 0x23)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved.
6:0	RESERVED	R/W	0x00	Reserved.

7.7.34 CSI-2 Termination Enable

The CSI-2 Termination Enable register is intended for system debugging.

表 7-46. CSI_EN_RXTERM (Address 0x24)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	R/W	0x0	Reserved.
3	EN_RXTERM_D3	R/W	0x0	Reserved.
2	EN_RXTERM_D2	R/W	0x0	Reserved.
1	EN_RXTERM_D1	R/W	0x0	Reserved.
0	EN_RXTERM_D0	R/W	0x0	Reserved.

7.7.35 CSI-2 Packet Header Control

表 7-47. CSI_PKT_HDR_TINIT_CTRL (Address 0x31)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	PKT_HDR_SEL_VC	R/W	0x0	For interleaved VC packet select the VC ID to display the packet header. This is effective only if bit4 is set high (PKT_HDR_VCI_ENABLE).
5	PKT_HDR_CORRECTED	R/W	0x1	1: Displays the corrected CSI-2 packet header (in case of error) sent to the receiver 0: Displays the received CSI-2 packet header from imager
4	PKT_HDR_VCI_ENABLE	R/W	0x0	Enable the CSI-2 packet header selection based on VC for interleaved mode. For interleaved VC packet set this bit to record the packet headers for each VC. For regular data packet ignore this bit.
3	RESERVED	R/W	0x0	Reserved.
2:0	TINIT_TIME	R/W	0x0	CSI-2 Initial Time after power up. Any LP control data are ignored during this time for all CSI-2 lanes. 000 = 100 µs 001 = 200 µs 010 = 300 µs 111 = 800 µs and so forth.

7.7.36 Back Channel Configuration

表 7-48. BCC_CONFIG (Address 0x32)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	I2C_PASS_THROUGH_ALL	R/W	0x0	I2C Pass-Through All Transactions. 0: Disabled 1: Enabled
6	I2C_PASS_THROUGH	R/W	0x0	I2C Pass-Through to Deserializer if decode matches. 0: Pass-Through Disabled 1: Pass-Through Enabled
5	AUTO_ACK_ALL	R/W	0x0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge. 1: Enable 0: Disable
4	RESERVED	R/W	0x0	Reserved.
3	RX_PARITY_CHECKER_ENABLE	R/W	0x1	Parity Checker Enable. 0: Disable 1: Enable
2	RESERVED	R/W	0x0	Reserved.
1	RESERVED	R/W	0x0	Reserved.
0	RESERVED	R/W	0x1	Reserved.

7.7.37 Datapath Control 1

表 7-49. DATAPATH_CTL1 (Address 0x33)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R/W	0x00	Reserved.
2	DCA_CRC_EN	R/W	0x1	DCA CRC Enable. If set to a 1, the Forward Channel sends a CRC as part of the DCA sequence. The DCA CRC protects the first 8 bytes of the DCA sequence. The CRC is sent as the 9th byte.
1:0	FC_GPIO_EN	R/W	0x0	Forward Channel GPIO Enable. Configures the number of enabled forward channel GPIOs. 00: GPIOs disabled 01: One GPIO 10: Two GPIOs 11: Four GPIOs

7.7.38 Remote Partner Capabilities 1

表 7-50. REMOTE_PAR_CAP1 (Address 0x35)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	FREEZE_DES_CAP	R/W	0x0	Freeze Partner Capabilities. Prevent auto-loading of the Partner Capabilities by the Bidirectional Control Channel. The Capabilities are frozen at the values written in registers 0x1E and 0x1F.
6	RESERVED	R/W	0x0	Reserved.
5	BIST_EN	R/W	0x0	Link BIST Enable. This bit indicates the remote partner is requesting BIST operation over the FPD-Link III interface. This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE_DES_CAP bit to prevent overwriting by the Bidirectional Control Channel.

表 7-50. REMOTE_PAR_CAP1 (Address 0x35) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
4	MPORT	R/W	0x0	Remote Partner Multi-Port capable. 0 : Remote partner is a single-port deserializer device 1 : Remote partner is a multi-port deserializer device This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE_DES_CAP bit to prevent overwriting by the Bidirectional Control Channel.
3:0	PORT_NUM	R/W	0x0	Remote Partner port number. When connected to a multi-port device, this field indicates the port number to which the Serializer is connected. This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE_DES_CAP bit to prevent overwriting by the Bidirectional Control Channel.

7.7.39 Partner Deserializer ID

表 7-51. DES_ID (Address 0x37)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	DES_ID	R/W	0x3D	Remote Deserializer ID. This field is normally loaded automatically from the remote Deserializer.
0	FREEZE_ DEVICE_ID	R/W	0x0	Freeze Deserializer Device ID. Prevent auto-loading of the Deserializer Device ID from the back channel. The ID is frozen at the value written.

7.7.40 Target 0 ID

表 7-52. TARGET_ID_0 (Address 0x39)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_0	R/W	0x00	7-bit Remote Target Device ID 0. Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID0, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	Reserved.

7.7.41 Target 1 ID

表 7-53. TARGET_ID_1 (Address 0x3A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_1	R/W	0x00	7-bit Remote Target Device ID 1. Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID1, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	Reserved.

7.7.42 Target 2 ID

表 7-54. TARGET_ID_2 (Address 0x3B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_2	R/W	0x00	7-bit Remote Target Device ID 2. Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID2, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	Reserved.

7.7.43 Target 3 ID

表 7-55. TARGET_ID_3 (Address 0x3C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_3	R/W	0x00	7-bit Remote Target Device ID 3. Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID3, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	Reserved.

7.7.44 Target 4 ID

表 7-56. TARGET_ID_4 (Address 0x3D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_4	R/W	0x00	7-bit Remote Target Device ID 4. Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID4, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	Reserved.

7.7.45 Target 5 ID

表 7-57. TARGET_ID_5 (Address 0x3E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_5	R/W	0x00	7-bit Remote Target Device ID 5. Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID5, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	Reserved.

7.7.46 Target 6 ID

表 7-58. TARGET_ID_6 (Address 0x3F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_6	R/W	0x00	7-bit Remote Target Device ID 6. Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID6, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	Reserved.

7.7.47 Target 7 ID

表 7-59. TARGET_ID_7 (Address 0x40)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_7	R/W	0x00	7-bit Remote Target Device ID 7. Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID7, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	Reserved.

7.7.48 Target 0 Alias

表 7-60. TARGET_ID_ALIAS_0 (Address 0x41)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_ALIAS_0	R/W	0x00	7-bit Remote Target Device Alias ID 0. Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_0	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 0 independent of the forward channel lock state or status of the remote Deserializer Acknowledge. 1: Enable 0: Disable This is intended for debugging only and not recommended for normal operation.

7.7.49 Target 1 Alias

表 7-61. TARGET_ID_ALIAS_1 (Address 0x42)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_ALIAS_1	R/W	0x00	7-bit Remote Target Device Alias ID 1. Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID1 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_1	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 1 independent of the forward channel lock state or status of the remote Deserializer Acknowledge. 1: Enable 0: Disable This is intended for debugging only and not recommended for normal operation.

7.7.50 Target 2 Alias

表 7-62. TARGET_ID_ALIAS_2 (Address 0x43)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_ALIAS_2	R/W	0x00	7-bit Remote Target Device Alias ID 2. Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID2 register. A value of 0 in this field disables access to the remote I2C Target.

表 7-62. TARGET_ID_ALIAS_2 (Address 0x43) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	TARGET_AUTO_ACK_2	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 2 independent of the forward channel lock state or status of the remote Deserializer Acknowledge. 1: Enable 0: Disable This is intended for debugging only and not recommended for normal operation.

7.7.51 Target 3 Alias

表 7-63. TARGET_ID_ALIAS_3 (Address 0x44)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_ALIAS_3	R/W	0x00	7-bit Remote Target Device Alias ID 3. Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID3 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_3	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 3 independent of the forward channel lock state or status of the remote Deserializer Acknowledge. 1: Enable 0: Disable This is intended for debugging only and not recommended for normal operation.

7.7.52 Target 4 Alias

表 7-64. TARGET_ID_ALIAS_4 (Address 0x45)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_ALIAS_4	R/W	0x00	7-bit Remote Target Device Alias ID 4. Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID4 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_4	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 4 independent of the forward channel lock state or status of the remote Deserializer Acknowledge. 1: Enable 0: Disable This is intended for debugging only and not recommended for normal operation.

7.7.53 Target 5 Alias

表 7-65. TARGET_ID_ALIAS_5 (Address 0x46)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_ALIAS_5	R/W	0x00	7-bit Remote Target Device Alias ID 5. Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID5 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_5	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 5 independent of the forward channel lock state or status of the remote Deserializer Acknowledge. 1: Enable 0: Disable This is intended for debugging only and not recommended for normal operation.

7.7.54 Target 6 Alias

表 7-66. TARGET_ID_ALIAS_6 (Address 0x47)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_ALIAS_6	R/W	0x00	7-bit Remote Target Device Alias ID 6. Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID6 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_6	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 6 independent of the forward channel lock state or status of the remote Deserializer Acknowledge. 1: Enable 0: Disable This is intended for debugging only and not recommended for normal operation.

7.7.55 Target 7 Alias

表 7-67. TARGET_ID_ALIAS_7 (Address 0x48)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID_ALIAS_7	R/W	0x00	7-bit Remote Target Device Alias ID 7. Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID7 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_7	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 7 independent of the forward channel lock state or status of the remote Deserializer Acknowledge. 1: Enable 0: Disable This is intended for debugging only and not recommended for normal operation.

7.7.56 Back Channel Control

表 7-68. BC_CTRL (Address 0x49)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R	0x0	Reserved.
5	BIST_CRC_ERR_CLR	(R/W)/SC	0x0	Clear BIST CRC error counter. 0: Disable clear 1: Enable Clear
4	RESERVED	R/W	0x0	Reserved.
3	CRC_ERR_CLR	(R/W)/SC	0x0	Clear CRC error. 0: Disable clear 1: Enable clear
2:0	LINK_DET_TIMER	R/W	0x0	TX-RX link detect timer val.

7.7.57 Revision ID

表 7-69. REV_MASK_ID (Address 0x50)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	REVISION_ID	R	0x2	Revision ID.
3:0	MASK_ID	R	0x0	Mask ID.

7.7.58 Device Status

表 7-70. Device STS (Address 0x51)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	CFG_CKSUM_STS	R	0x0	Config Checksum Passed. This bit is set following initialization if the Configuration data in the eFuse ROM had a valid checksum.
6	CFG_INIT_DONE	R	0x0	Power-up initialization complete. This bit is set after Initialization is complete. Configuration from eFuse ROM has completed.
5:0	RESERVED	R	0x00	Reserved.

7.7.59 General Status

表 7-71. GENERAL_STATUS (Address 0x52)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved.
6	RX_LOCK_DETECT	R	0x0	Deserializer LOCK status This bit indicates the LOCK status of the Deserializer.
5	RESERVED	R	0x0	Reserved.
4	LINK_LOST_FLAG	R	0x0	Back Channel Link lost Status changed. This bit is set if a change in BC LINK DET lost status has been detected. This bit is cleared upon read of CRC ERR CLR register or HS PLL loses lock.
3	BIST_CRC_ERR	R	0x0	BIST Error is detected. The BIST_ERR_CNT register contain the number of Back Channel BIST errors.
2	HS_PLL_LOCK	R	0x1	Forward Channel High speed PLL lock flag.
1	CRC_ERR	R	0x0	Back Channel CRC error detected. This bit is set when the back channel errors detected when BC LINK DET is asserted. This bit is cleared upon read of CRC_ERR_CLR register.
0	LINK_DET	R	0x1	Back Channel Link detect. This bit is set when BC link is valid.

7.7.60 GPIO Pin Status

表 7-72. GPIO_PIN_STS For Input State Only (Address 0x53)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	R	0x0	Reserved.
3:0	GPIO_STS	R	0x0	GPIO Pin Status. This register reads the current values on GPIO pins. Bit 3 reads the GPIO3 pin status. Bit 2 reads the GPIO2 pin status. Bit 1 reads the GPIO1 pin status. Bit 0 reads the GPIO0 pin status.

7.7.61 BIST Error Count

表 7-73. BIST_ERR_CNT (Address 0x54)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	BIST_BC_ERRCNT	R	0x00	CRC error count in BIST mode.

7.7.62 CRC Error Count 1

表 7-74. CRC_ERR_CNT1 (Address 0x55)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CRC_ERR_CNT1	R	0x00	CRC Error count (LSB).

7.7.63 CRC Error Count 2

表 7-75. CRC_ERR_CNT2 (Address 0x56)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CRC_ERR_CNT2	R	0x00	CRC Error count (MSB).

7.7.64 Sensor Status

表 7-76. SENSOR_STATUS (Address 0x57)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R	0x0	Reserved.
5	T_SENSOR_HI	R	0x0	When set, this bit indicates that Internal Temperature Sensor is above SENSE_T_HI limit. This bit is cleared upon read.
4	T_SENSOR_LOW	R	0x0	When set, this bit indicates that Internal Temperature Sensor is below SENSE_T_LO limit. This bit is cleared upon read.
3	V1_SENSOR_HI	R	0x0	When set, this bit indicates that GPIO1 input is above SENSE_V1_HI limit. This bit is cleared upon read.
2	V1_SENSOR_LOW	R	0x0	When set, this bit indicates that GPIO1 input is below SENSO_V1_LO limit. This bit is cleared upon read.
1	V0_SENSOR_HI	R	0x0	When set, this bit indicates that GPIO0 input is above SENSE_V0_HI limit. This bit will be cleared upon read.
0	V0_SENSOR_LOW	R	0x0	When set, this bit indicates that GPIO0 input is below SENSO_V0_LO limit. This bit will be cleared upon read.

7.7.65 Sensor V0

表 7-77. SENSOR_V0 (Address 0x58)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:4	VOLTAGE_SENSOR_V0_MAX	RC	0x0	GPIO0 Voltage sensor max reading when the GPIO0 voltage is above SENSE_V0_HI limit. This bit is cleared upon read. 0 indicates alarm has not been triggered.
3	RESERVED	R/W	0x0	Reserved.
2:0	VOLTAGE_SENSOR_V0_MIN	RC	0x7	GPIO0 Voltage sensor min reading when GPIO0 voltage is below SENSE_V0_LO limit. This bit is cleared upon read. 7 indicates alarm has not been triggered.

7.7.66 Sensor V1

表 7-78. SENSOR_V1 (Address 0x59)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:4	VOLTAGE_SENSOR_V1_MAX	RC	0x0	GPIO1 Voltage sensor max reading when the GPIO1 voltage is above SENSE_V1_HI limit. This bit is cleared upon read. 0 indicates alarm has not been triggered.
3	RESERVED	R/W	0x0	Reserved.
2:0	VOLTAGE_SENSOR_V1_MIN	RC	0x7	GPIO1 Voltage sensor min reading when GPIO1 voltage is below SENSE_V1_LO limit. This bit is cleared upon read. 7 indicates alarm has not been triggered.

7.7.67 Sensor T

表 7-79. SENSOR_T (Address 0x5A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved.
6:4	TEMP_MAX	RC	0x0	Internal Temperature sensor maximum reading when temperature is above SENSE_T_HI limit. This bit is cleared upon read. 0 indicates alarm has not been triggered.
3	RESERVED	R/W	0x0	Reserved
2:0	TEMP_MIN	RC	0x7	Internal Temperature sensor minimum reading when temperature is below SENSE_T_LO limit. This bit is cleared upon read. 7 indicates alarm has not been triggered.

7.7.68 CSI-2 Error Count

表 7-80. CSI_ERR_CNT (Address 0x5C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_ERR_CNT	RC	0x00	CSI-2 Error Counter Register. This register counts the number of CSI-2 packets received with errors since the last read of the counter.

7.7.69 CSI-2 Error Status

表 7-81. CSI_ERR_STATUS (Address 0x5D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	R	0x0	Reserved.
3	LINE_LEN_ MISMATCH	R/RC	0x0	Indicates Line length less than the received Packet header Word count.
2	CHKSUM_ERR	R/RC	0x0	Indicates a checksum error detected in the incoming data (uncorrectable).
1	ECC_2BIT_ERR	R/RC	0x0	Indicates a 2-Bit Ecc error (uncorrectable) in the Packet header.
0	ECC_1BIT_ERR	R/RC	0x0	Indicates a 1-Bit Ecc error detected in the Packet header.

7.7.70 CSI-2 Errors Data Lanes 0 and 1

表 7-82. CSI_ERR_DLANE01 (Address 0x5E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	SOT_ERROR_1	R	0x0	Lane 1: Single-bit Error in SYNC Sequence - Correctable.
6	SOT_SYNC_ ERROR_1	R	0x0	Lane 1: Multi-bit Error in SYNC Sequence - Uncorrectable.
5	CNTRL_ERR_ HSRQST_1	R	0x0	Lane 1: Control Error in HS Request Mode.
4	RESERVED	R	0x0	Reserved.
3	SOT_ERROR_0	R	0x0	Lane 0: Single-bit Error in SYNC Sequence - Correctable.
2	SOT_SYNC_ ERROR_0	R	0x0	Lane 0: Multi-bit Error in SYNC Sequence - Uncorrectable.
1	CNTRL_ERR_ HSRQST_0	R	0x0	Lane 0: Control Error in HS Request Mode.
0	RESERVED	R	0x0	Reserved.

7.7.71 CSI-2 Errors Data Lanes 2 and 3

表 7-83. CSI_ERR_DLANE23 (Address 0x5F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	SOT_ERROR_3	R	0x0	Lane 3: Single-bit Error in SYNC Sequence - Correctable.

表 7-83. CSI_ERR_DLANE23 (Address 0x5F) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
6	SOT_SYNC_ERROR_3	R	0x0	Lane 3: Multi-bit Error in SYNC Sequence - Uncorrectable.
5	CNTRL_ERR_HSRQST_3	R	0x0	Lane 3: Control Error in HS Request Mode.
4	RESERVED	R	0x0	Reserved.
3	SOT_ERROR_2	R	0x0	Lane 2: Single-bit Error in SYNC Sequence - Correctable.
2	SOT_SYNC_ERROR_2	R	0x0	Lane 2: Multi-bit Error in SYNC Sequence - Uncorrectable.
1	CNTRL_ERR_HSRQST_2	R	0x0	Lane 2: Control Error in HS Request Mode.
0	RESERVED	R	0x0	Reserved.

7.7.72 CSI-2 Errors Clock Lane

表 7-84. CSI_ERR_CLK_LANE (Address 0x60)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:2	RESERVED	R	0x00	Reserved.
1	CNTRL_ERR_HSRQST_CK0	R	0x0	Clk Lane: Control Error in HS Request Mode.
0	RESERVED	R	0x0	Reserved.

7.7.73 CSI-2 Packet Header Data

表 7-85. CSI_PKT_HDR_VC_ID (Address 0x61)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	LONG_PKT_VCHNL_ID	R	0x0	Virtual Channel ID from CSI-2 Packet header.
5:0	LONG_PKT_DATA_ID	R	0x00	Data ID from CSI-2 Packet header.

7.7.74 Packet Header Word Count 0

表 7-86. PKT_HDR_WC_LSB (Address 0x62)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LONG_PKT_WRD_CNT_LSB	R	0x00	Payload count lower byte from CSI-2 Packet header.

7.7.75 Packet Header Word Count 1

表 7-87. PKT_HDR_WC_MSB (Address 0x63)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LONG_PKT_WRD_CNT_MSB	R	0x00	Payload count upper byte from CSI-2 Packet header.

7.7.76 CSI-2 ECC

表 7-88. CSI_ECC (Address 0x64)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	LINE_LENGTH_CHANGE	R	0x0	Indicates Line length change detected per frame.

表 7-88. CSI_ECC (Address 0x64) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
6	RESERVED	R	0x0	Reserved.
5:0	CSI-2_ECC	R	0x00	CSI-2 ECC byte from packet header.

7.7.77 IND_ACC_CTL

表 7-89. IND_ACC_CTL (Address 0xB0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R	0x0	Reserved.
4:2	IA_SEL	R/W	0x0	Indirect Register Select: Selects target for register access 000 : PATGEN 001 : FPD3 TX Registers 010: DIE ID Data
1	IA_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address is automatically incremented by 1.
0	IA_READ	R/W	0x0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes are also asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data.

7.7.78 IND_ACC_ADDR

表 7-90. IND_ACC_ADDR (Address 0xB1)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	IND_ACC_ADDR	R/W	0x00	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

7.7.79 IND_ACC_DATA

表 7-91. IND_ACC_DATA (Address 0xB2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	IND_ACC_DATA	R/W	0x00	Indirect Access Register Data: Writing this register causes an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register returns the value of the selected analog block register.

7.7.80 FPD3_TX_ID0

表 7-92. FPD3_TX_ID0 (Address 0xF0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_TX_ID0	R	0x5F	FPD3_TX_ID0: First byte ID code: '_'.

7.7.81 FPD3_TX_ID1

表 7-93. FPD3_TX_ID1 (Address 0xF1)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_TX_ID1	R	0x55	FPD3_TX_ID1: 2nd byte of ID code: 'U'.

7.7.82 FPD3_TX_ID2

表 7-94. FPD3_TX_ID2 (Address 0xF2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_TX_ID2	R	0x42	FPD3_TX_ID2: 3rd byte of ID code: ‘B’.

7.7.83 FPD3_TX_ID3

表 7-95. FPD3_TX_ID3 (Address 0xF3)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_TX_ID3	R	0x39	FPD3_TX_ID3: 4th byte of ID code: ‘9’.

7.7.84 FPD3_TX_ID4

表 7-96. FPD3_TX_ID4 (Address 0xF4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_TX_ID4	R	0x35	FPD3_TX_ID4: 5th byte of ID code: '5'.

7.7.85 FPD3_TX_ID5

表 7-97. FPD3_TX_ID5 (Address 0xF5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_TX_ID5	R	0x33	FPD3_TX_ID5: 6th byte of ID code: '3'.

7.7.86 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map (表 7-98); that is, Pattern Generator, and Analog controls. Register access is provided through an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0xB0-0xB2 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:
1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Write the data value to the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 writes additional data bytes to subsequent register offset locations.

For reads, the process is as follows:
1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Read from the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 reads additional data bytes from subsequent register offset locations.

表 7-98. Indirect Register Map Description

IA SELECT 0xB0[4:2]	PAGE/BLOCK	INDIRECT REGISTERS	ADDRESS RANGE	DESCRIPTION
000	0	Digital Page 0 Indirect Registers	0x01 - 0x1F	Pattern Gen Registers.
010	2	Indirect Registers: Die ID Data	0x00 - 0x0F	Hold 16 bytes that correspond to Die ID data.

7.7.86.1 PGEN_CTL

表 7-99. PGEN_CTL (Address 0x01)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RESERVED	R/W	0x0	Reserved.
0	PGEN_ ENABLE	R/W	0x0	Pattern Generator Enable. 1: Enable Pattern Generator 0: Disable Pattern Generator

7.7.86.2 PGEN_CFG

表 7-100. PGEN_CFG (Address 0x02)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	PGEN_ FIXED_EN	R/W	0x0	Fixed Pattern Enable. Setting this bit enables Fixed Color Patterns. 0 : Send Color Bar Pattern 1 : Send Fixed Color Pattern
6	RESERVED	R/W	0x0	Reserved.
5:4	NUM_ CBARS	R/W	0x3	Number of Color Bars. 00 : 1 Color Bar 01 : 2 Color Bars 10 : 4 Color Bars 11 : 8 Color Bars

表 7-100. PGEN_CFG (Address 0x02) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3:0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.

7.7.86.3 PGEN_CSI_DI

表 7-101. PGEN_CSI_DI (Address 0x03)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	PGEN_CSI_VC	R/W	0x0	CSI-2 Virtual Channel Identifier. This field controls the value sent in the CSI-2 packet for the Virtual Channel Identifier.
5:0	PGEN_CSI_DT	R/W	0x24	CSI-2 Data Type. This field controls the value sent in the CSI-2 packet for the Data Type. The default value (0x24) indicates RGB888.

7.7.86.4 PGEN_LINE_SIZE1

表 7-102. PGEN_LINE_SIZE1 (Address 0x04)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x07	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640-pixel line width.

7.7.86.5 PGEN_LINE_SIZE0

表 7-103. PGEN_LINE_SIZE0 (Address 0x05)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640-pixel line width.

7.7.86.6 PGEN_BAR_SIZE1

表 7-104. PGEN_BAR_SIZE1 (Address 0x06)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x00	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

7.7.86.7 PGEN_BAR_SIZE0

表 7-105. PGEN_BAR_SIZE0 (Address 0x07)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

7.7.86.8 PGEN_ACT_LPF1

表 7-106. PGEN_ACT_LPF1 (Address 0x08)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ACT_LPF[15:8]	R/W	0x01	Active Lines Per Frame. Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

7.7.86.9 PGEN_ACT_LPF0

表 7-107. PGEN_ACT_LPF0 (Address 0x09)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame. Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

7.7.86.10 PGEN_TOT_LPF1

表 7-108. PGEN_TOT_LPF1 (Address 0x0A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_TOT_LPF[15:8]	R/W	0x02	Total Lines Per Frame. Most significant byte of the number of total lines per frame including vertical blanking.

7.7.86.11 PGEN_TOT_LPF0

表 7-109. PGEN_TOT_LPF0 (Address 0x0B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_TOT_LPF[7:0]	R/W	0x0D	Total Lines Per Frame. Least significant byte of the number of total lines per frame including vertical blanking.

7.7.86.12 PGEN_LINE_PD1

表 7-110. PGEN_LINE_PD1 (Address 0x0C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_PD[15:8]	R/W	0x0C	Line Period. Most significant byte of the line period in 10-ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

7.7.86.13 PGEN_LINE_PD0

表 7-111. PGEN_LINE_PD0 (Address 0x0D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period. Least significant byte of the line period in 10-ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

7.7.86.14 PGEN_VBP

表 7-112. PGEN_VBP (Address 0x0E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch. This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

7.7.86.15 PGEN_VFP

表 7-113. PGEN_VFP (Address 0x0F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_VFP	R/W	0x0A	Vertical Front Porch. This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

7.7.86.16 PGEN_COLOR0

表 7-114. PGEN_COLOR0 (Address 0x10)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR0	R/W	0xAA	Pattern Generator Color 0. For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

7.7.86.17 PGEN_COLOR1

表 7-115. PGEN_COLOR1 (Address 0x11)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR1	R/W	0x33	Pattern Generator Color 1. For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

7.7.86.18 PGEN_COLOR2

表 7-116. PGEN_COLOR2 (Address 0x12)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR2	R/W	0xF0	Pattern Generator Color 2. For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

7.7.86.19 PGEN_COLOR3

表 7-117. PGEN_COLOR3 (Address 0x13)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR3	R/W	0x7F	Pattern Generator Color 3. For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

7.7.86.20 PGEN_COLOR4

表 7-118. PGEN_COLOR4 (Address 0x14)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR4	R/W	0x55	Pattern Generator Color 4. For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

7.7.86.21 PGEN_COLOR5

表 7-119. PGEN_COLOR5 (Address 0x15)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR5	R/W	0xCC	Pattern Generator Color 5. For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

7.7.86.22 PGEN_COLOR6

表 7-120. PGEN_COLOR6 (Address 0x16)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR6	R/W	0x0F	Pattern Generator Color 6. For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

7.7.86.23 PGEN_COLOR7

表 7-121. PGEN_COLOR7 (Address 0x17)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR7	R/W	0x80	Pattern Generator Color 7. For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

7.7.86.24 PGEN_COLOR8

表 7-122. PGEN_COLOR8 (Address 0x18)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR8	R/W	0x00	Pattern Generator Color 8. For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

7.7.86.25 PGEN_COLOR9

表 7-123. PGEN_COLOR9 (Address 0x19)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR9	R/W	0x00	Pattern Generator Color 9. For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

7.7.86.26 PGEN_COLOR10

表 7-124. PGEN_COLOR10 (Address 0x1A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR10	R/W	0x00	Pattern Generator Color 10. For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

7.7.86.27 PGEN_COLOR11

表 7-125. PGEN_COLOR11 (Address 0x1B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR11	R/W	0x00	Pattern Generator Color 11. For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

7.7.86.28 PGEN_COLOR12

表 7-126. PGEN_COLOR12 (Address 0x1C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR12	R/W	0x00	Pattern Generator Color 12. For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

7.7.86.29 PGEN_COLOR13

表 7-127. PGEN_COLOR13 (Address 0x1D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR13	R/W	0x00	Pattern Generator Color 13. For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

7.7.86.30 PGEN_COLOR14

表 7-128. PGEN_COLOR14 (Address 0x1E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR14	R/W	0x00	Pattern Generator Color 14. For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

7.7.86.31 PGEN_COLOR15

表 7-129. PGEN_COLOR15 (Address 0x1F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ COLOR15	R/W	0x00	Pattern Generator Color 15. For Fixed Color Patterns, this register controls the sixteenth byte of the fixed color pattern.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The link between the DS90UB635-Q1 and the companion deserializer has two distinct data paths. The first path is a forward channel which is nominally running at up to 4.16 Gbps and is encoded such that the channel occupies a bandwidth from 20 MHz to 2.1 GHz. The second path is a back channel from the deserializer to the serializer which occupies a frequency range nominally from 10 MHz to 50 MHz.

For these two communications links to operate properly, the circuit between the serializer and the deserializer must present a characteristic impedance of 50 Ω. Deviations from this 50-Ω characteristic will lead to signal reflections either at the serializer or deserializer, which will result in bit errors.

8.1.1 Power-over-Coax

The DS90UB635-Q1 is designed to support the Power-over-Coax (PoC) method of powering remote sensor systems. With this method, the power is delivered over the same medium (a coaxial cable) used for high-speed digital video data, bidirectional control, and diagnostics data transmission. This method uses passive networks or filters that isolate the transmission line from the loading of the DC-DC regulator circuits and their connecting power traces on both sides of the link as shown in 図 8-1.

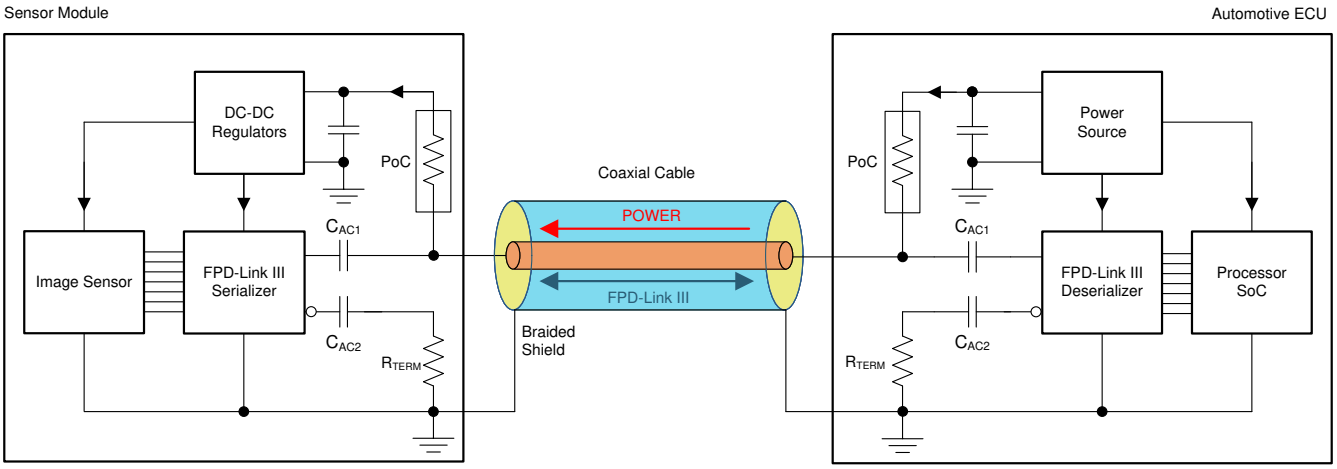

図 8-1. Power-over-Coax (PoC) System Diagram

The PoC networks' impedance of ≥ 1 kΩ over a specific frequency band is recommended to isolate the transmission line from the loading of the regulator circuits. Higher PoC network impedance will contribute to favorable insertion loss and return loss characteristics in the high-speed channel. The lower limit of the frequency band is defined as ½ of the frequency of the back channel, f_{BC}. The upper limit of the frequency band is the frequency of the forward high-speed channel, f_{FC}. However, the main criteria that need to be met in the high-speed channel, which consists of a serializer PCB, a deserializer PCB, and a cable, are the insertion loss and return loss limits defined in the Total Channel Requirements(1) over the entire system, while the system is under maximum current load and extreme temperature conditions (2).

1. Contact TI for more information on the required Channel Specifications defined for each individual FPD-Link device.

2. The PoC network and any components along the high-speed trace on the PCB will contribute to the PCB loss budget. TI has recommendations for the loss budget allocation for each individual PCB and cable component in the overall high-speed channel, but the loss limits defined for the total channel in the Channel Specifications must be met.

図 8-2 shows an example PoC network suitable for a "4G" FPD-Link III consisting of DS90UB635-Q1 and DS90UB638-Q1 or DS90UB662-Q1 pair with the bidirectional channel operating at 50 Mbps (½ f_{BCC} = 25 MHz) and the forward channel operating at 4.16 Gbps (f_{FC} ≈ 2.1 GHz). Other PoC networks are possible and may be different on the serializer and the deserializer boards as long as the printed-circuit board return loss requirements listed in 表 8-2 are met.

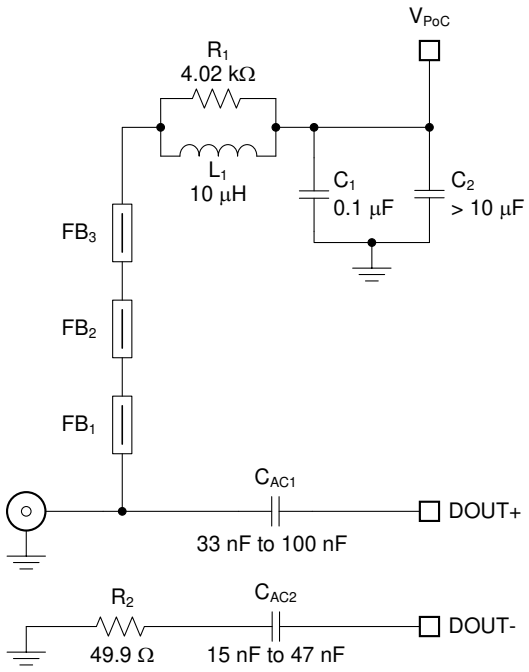

図 8-2. Typical PoC Network for a "4G" FPD-Link III

表 8-1 lists essential components for this particular PoC network. Note that the impedance characteristic of the ferrite beads deviates with the bias current. Therefore, keeping the current going through the network below 150 mA is recommended.

表 8-1. Suggested Components for a "4G" FPD-Link III PoC Network

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	L1	Inductor, 10 µH, 0.288 Ω maximum, 530 mA minimum (Isat, Itemp) 30 MHz SRF minimum, 3 mm × 3 mm, General-Purpose	LQH3NPN100MJR	Murata
		Inductor, 10 µH, 0.288 Ω maximum, 530 mA minimum (Isat, Itemp) 30 MHz SRF minimum, 3 mm × 3 mm, AEC-Q200	LQH3NPZ100MJR	Murata
		Inductor, 10 µH, 0.360 Ω maximum, 450 mA minimum (Isat, Itemp) 30 MHz SRF minimum, 3.2 mm × 2.5 mm, AEC-Q200	NLCV32T-100K-EFD	TDK
		Inductor, 10 µH, 0.400 Ω typical, 550 mA minimum (Isat, Itemp) 39 MHz SRF typical, 3 mm × 3 mm, AEC-Q200	TYS3010100M-10	Laird
		Inductor, 10 µH, 0.325 Ω maximum, 725 mA minimum (Isat, Itemp) 41 MHz SRF typical, 3 mm × 3 mm, AEC-Q200	TYS3015100M-10	Laird
3	FB1-FB3	Ferrite Bead, 1.5 kΩ at 1 GHz, 0.5 Ω maximum at DC 500 mA at 85°C, 0603 SMD , General-Purpose	BLM18HE152SN1	Murata
		Ferrite Bead, 1.5 kΩ at 1 GHz, 0.5 Ω maximum at DC 500 mA at 85°C, 0603 SMD , AEC-Q200	BLM18HE152SZ1	Murata

In addition to the selection of PoC network components, their placement and layout play a critical role as well.

- Place the smallest component, typically a ferrite bead or a chip inductor, as close to the connector as possible. Route the high-speed trace through one of its pads to avoid stubs.
- Use the smallest component pads as allowed by manufacturer's design rules. Add anti-pads in the inner planes below the component pads to minimize impedance drop.
- Consult with the connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impact of the through-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.
- Use coupled 100-Ω differential signal traces from the device pins to the AC-coupling caps. Use 50-Ω single-ended traces from the AC-coupling capacitors to the connector.
- Terminate the inverting signal traces close to the connectors with standard 49.9-Ω resistors.

The suggested characteristics for single-ended PCB traces (microstrips or striplines) for serializer or deserializer boards are listed in 表 8-2. The effects of the PoC networks must be accounted for when testing the traces for compliance to the suggested limits.

表 8-2. Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks

PARAMETER		MIN	TYP	MAX	UNIT
L_{trace}	Single-ended PCB trace length from the device pin to the connector pin			5	cm
Z_{trace}	Single-ended PCB trace characteristic impedance	45	50	55	Ω
Z_{con}	Connector (mounted) characteristic impedance	40	50	60	Ω

The V_{POC} fluctuations on the serializer side, caused by the transient current draw of the sensor, the DC resistance of cables, and PoC components, must be kept to a minimum as well. Increasing the V_{POC} voltage and adding extra decoupling capacitance (> 10 µF) help reduce the amplitude and slew rate of the V_{POC} fluctuations.

8.2 Typical Applications

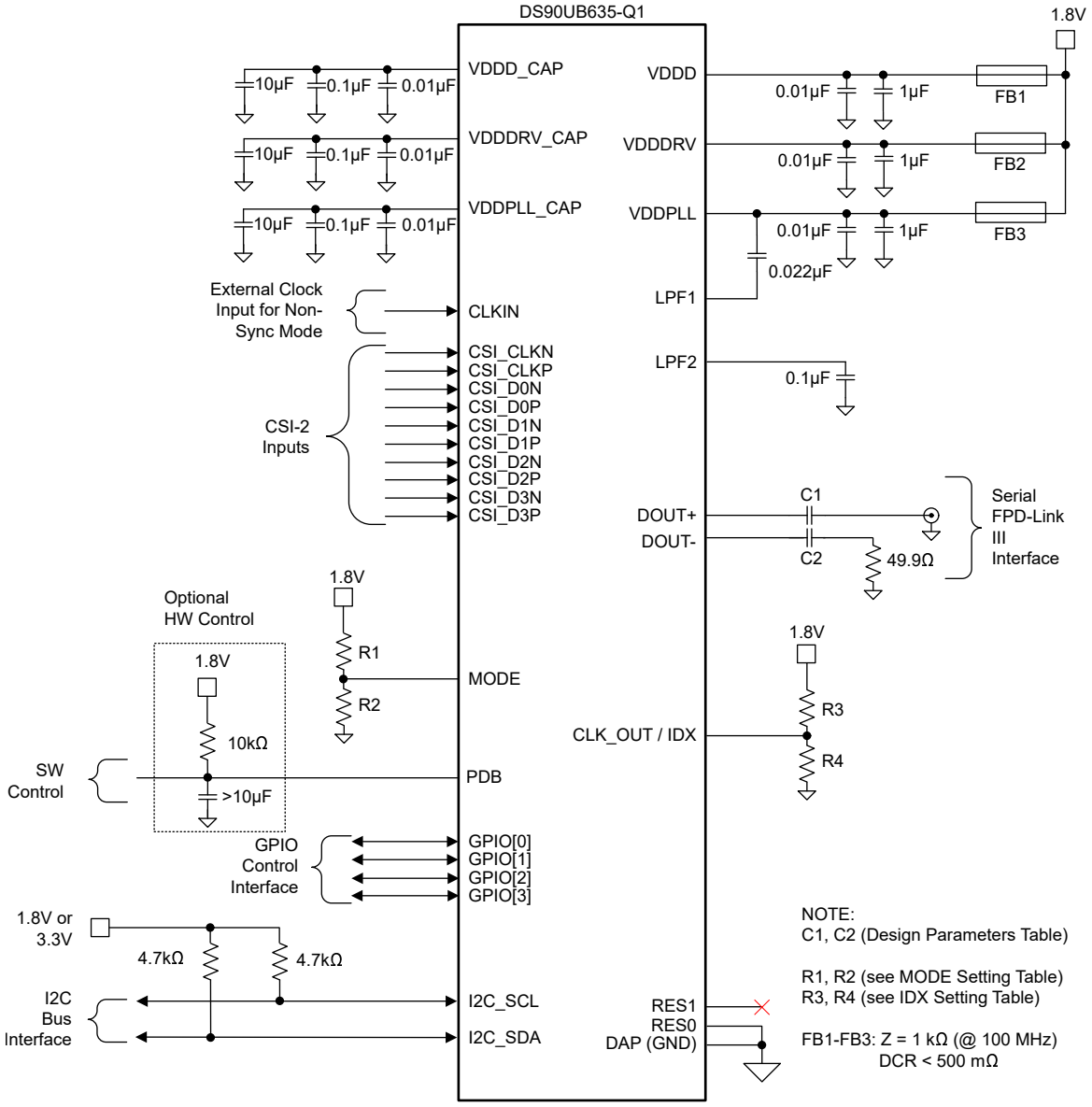

図 8-3. Typical Connection Diagram Coaxial

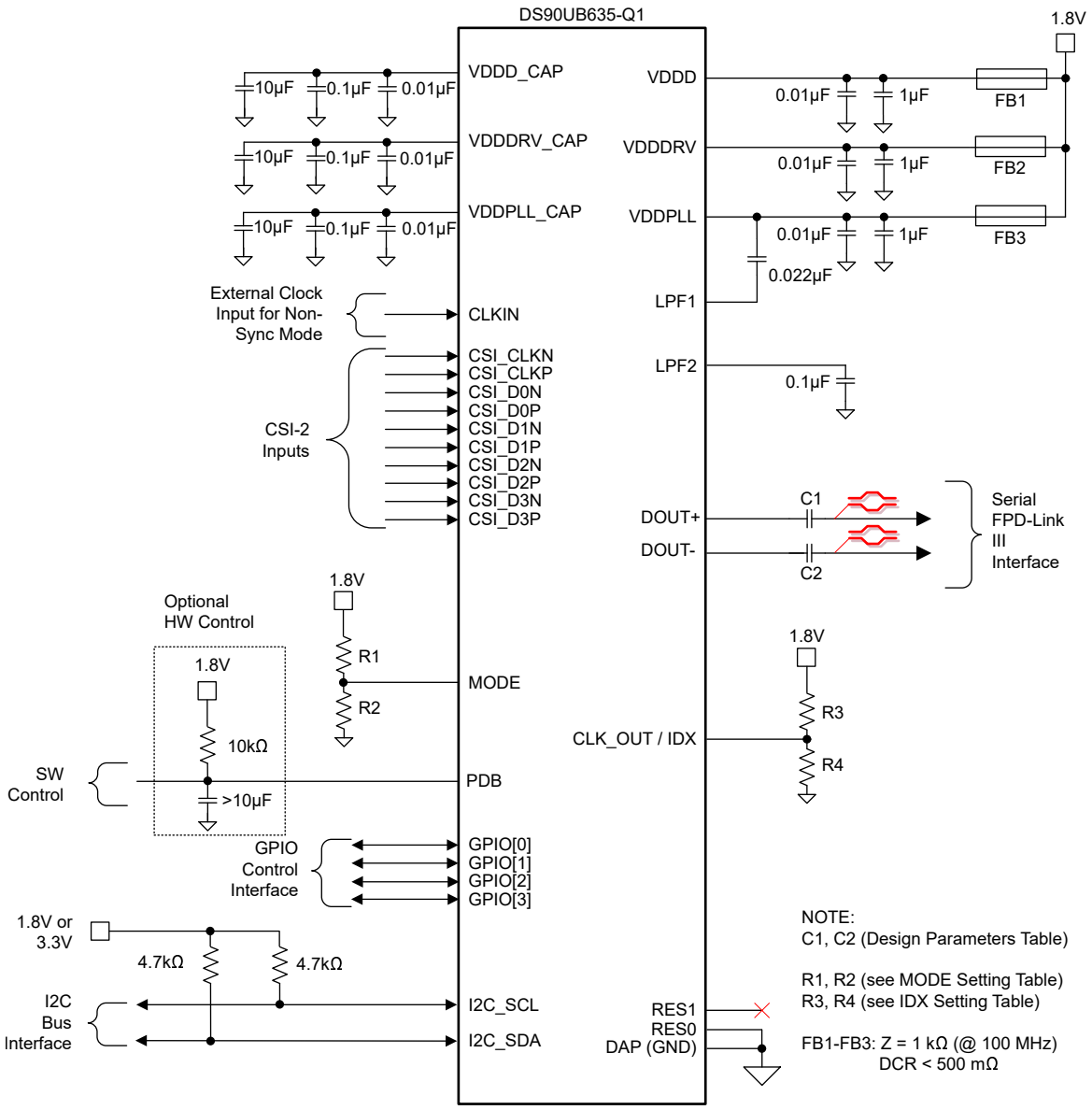

図 8-4. Typical Connection Diagram STP

8.2.1 Design Requirements

For a typical design application, use the parameters listed in 表 8-3.

表 8-3. Design Parameters

DESIGN PARAMETER	PIN(S)	VALUE
$V_{(VDD)}$	VDDD, VDDDRV, VDDPLL	1.8 V
AC-Coupling Capacitor for Synchronous Modes, Coaxial Connection	DOUT+	33nF – 100 nF (50 V / X7R / 0402)
	DOUT–	15nF – 47 nF (50 V / X7R / 0402)
AC-Coupling Capacitor for Synchronous Modes, STP Connection	DOUT+, DOUT–	33 – 100 nF (50 V / X7R / 0402)
AC-Coupling Capacitor for Non-Synchronous and DVP Backwards Compatible Modes, Coaxial Connection	DOUT+	100 nF (50 V / X7R / 0402)
	DOUT–	47 nF (50 V / X7R / 0402)
AC-Coupling Capacitor for Non-Synchronous and DVP Backwards Compatible Modes, STP Connection	DOUT+, DOUT–	100 nF (50 V / X7R / 0402)

The SER/DES only supports AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in 図 8-5 and 図 8-6. For applications using single-ended 50-Ω coaxial cable, terminate the unused data pins (DOUT+, DOUT–) with an AC-coupling capacitor and a 50-Ω resistor.

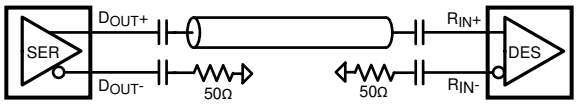

図 8-5. AC-Coupled Connection (Coaxial)

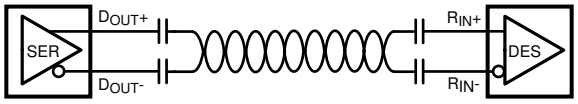

図 8-6. AC-Coupled Connection (STP)

For high-speed FPD–Link III transmissions, use the smallest available package for the AC-coupling capacitor to help minimize degradation of signal quality due to package parasitics.

8.2.2 Detailed Design Procedure

セクション 8.2 shows a typical application circuit of the DS90UB635-Q1. The next sections highlight recommendations for the critical device pins.

8.2.2.1 CSI-2 Interface

The CSI-2 input port on the DS90UB635-Q1 is compliant with the MIPI D-PHY v1.2 and CSI-2 v1.3 specifications. The CSI-2 interface consists of a clock and an option of one, two, or four data lanes. The clock and each of the data lanes are differential lines. The DS90UB635-Q1 CSI-2 input must be DC-coupled to a compatible CSI-2 transmitter. Follow the PCB layout guidelines given in *セクション 10.1.1*.

8.2.2.2 FPD-Link III Input / Output

The DS90UB635-Q1 serial data out signal operates at different data rates depending upon the mode in which the device is operating. In synchronous mode, where the reference clock is provided by the deserializer, the serial data rate is up to 4.16 Gbps.

The signals at DOUT+ and DOUT– must be AC-coupled. The AC-coupling capacitor values used on DOUT+ and DOUT– depends on the mode and cable used as shown in 表 8-3. When connecting to a coax cable, the AC-coupling capacitor on the negative terminal (DOUT–) should be approximately ½ of the AC-coupling capacitor value on DOUT+ and be terminated to a 50-Ω load. Make sure to follow the critical PCB layout guidelines given in *セクション 10.2*.

8.2.2.3 Internal Regulator Bypassing

The DS90UB635-Q1 features three internal regulators that must be bypassed to GND. The VDDD_CAP, VDDDRV_CAP, and VDDPLL_CAP are the pins that expose the outputs of the internal regulators for bypassing. TI recommends that each pin has a 10-µF, 0.1-µF, and a 0.01-µF capacitor to GND. The 0.01-µF caps must be placed as close as practical to the bypass pins.

8.2.2.4 Loop Filter Decoupling

The LPF1 and LPF2 pins are for connecting filter capacitors to the internal PLL circuits. LPF1 should have a 0.022-µF capacitor connected to the VDD_PLL pin (pin 11). The capacitor connected between LPF1 and VDDPLL must enclose as small of a loop as possible. LPF2 must have a 0.1-µF capacitor connecting the pin to GND. One of these PLLs generates the high-speed clock used in the serialization of the output, while the other PLL is used in the CSI-2 receive port. Noise coupled into these pins degrades the performance of the PLLs in the DS90UB635-Q1, so the caps must be placed close to the pins they are connected to, and the area of the loop enclosed must be minimized.

8.2.3 Application Curve

The falling edge of the blue trace indicates that the device should shift from LP to HS mode – the rise that comes about one division later is when the DS90UB635-Q1 turns on the internal termination so the device is ready to receive HS data. The transitions are the CSI-2 data, and then the drop of the blue trace indicates that the termination has been turned off.

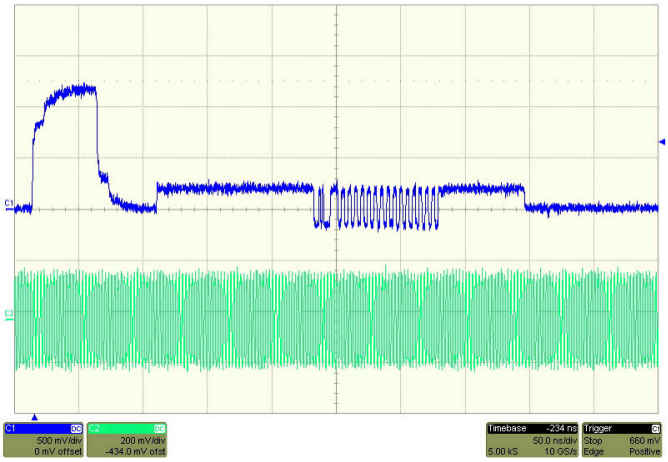

図 8-7. CSI-2 LP to HS Mode Transition

9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The *Pin Configuration and Functions* section provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

9.1 Power-Up Sequencing

The power-up sequence for the DS90UB635-Q1 is as follows:

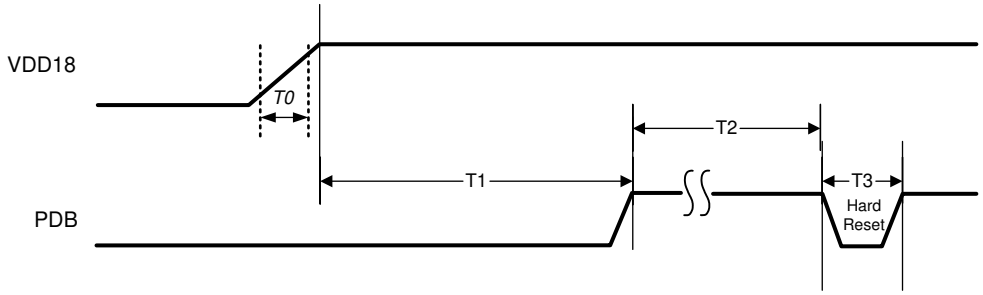

図 9-1. Power Supply Sequencing

表 9-1. Timing Diagram for the Power Supply Start-Up and Initialization Sequences

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
T0	VDD18 rise time	0.05			ms	at 10/90%
T1	VDD18 to PDB	0			ms	After VDD18 is stable
T2	PDB high time before PDB hard reset	1			ms	
T3	PDB high to low pulse width	3			ms	Hard reset (optional)
T4	PDB to I2C Ready	2			ms	See Initialization Sequence: Synchronous Clocking Mode

9.1.1 System Initialization

When initializing the communications link between a deserializer hub and a DS90UB635-Q1 serializer, the system timing will depend on the mode selected for generating the serializer reference clock. When synchronous clocking mode is selected, the serializer will relock onto the extracted back channel reference clock when available, so there is no need for local crystal oscillator at the sensor module. The initialization sequence follows the illustration given in the Initialization Sequence: Synchronous Clocking Mode.

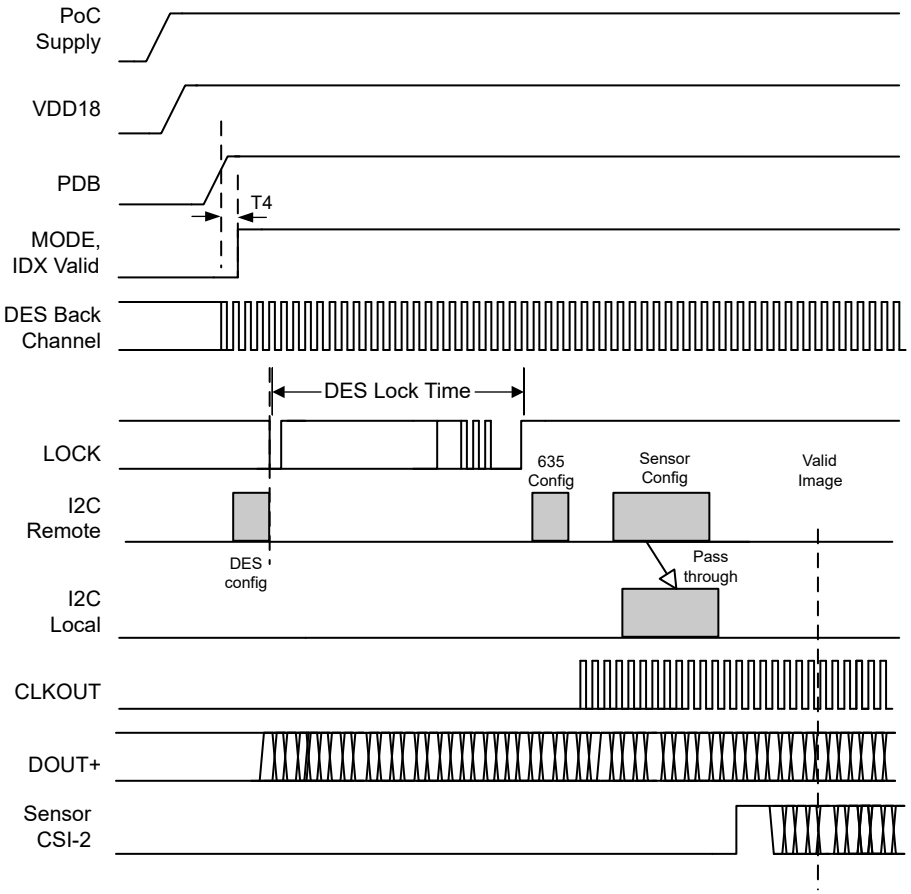

図 9-2. Initialization Sequence: Synchronous Clocking Mode

To allow for a quicker system bringup time, it is recommended to program the I2C watchdog timer speedup, by setting 0x0A = 0x12, before trying to access remote I2C target devices attached to the SER through the back channel from the deserializer. This will ensure a faster remote sensor access time even if the serializer I2C bus experiences unexpected noise during power up of the sensor module.

9.2 Power Down (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through VDD where VDD = 1.71 V to 1.89 V. PDB should be brought high after all power supplies on the board have stabilized.

When PDB is driven low, ensure that the pin is driven to 0 V for at least 3 ms before releasing or driving high. In the case where PDB is pulled up to VDD directly, a 10-kΩ pullup resistor and a > 10-µF capacitor to ground are required.

Toggling PDB low powers down the device and resets all control registers to default. After power up, if there are any errors seen, TI recommends clearing the registers to reset the errors.

Make sure to power up the VDDDRV before or at the same time as the VDDPLL.

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. External bypassing should be low-ESR ceramic capacitors with high-quality dielectric. The voltage rating of the ceramic capacitors must be at least 2× the power supply voltage being used.

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closest to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 47-µF to 100-µF range, which smooths low-frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane. TI also recommends that the user place a via on both ends of the capacitors. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin description tables typically provide guidance on which circuit blocks are connected to which power pin pairs (see *Pin Configuration and Functions* for more information). In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a dedicated ground plane. Place CSI-2 signals away from the single-ended or differential FPD-Link III RX input traces to prevent coupling from the CSI-2 lines to the Rx input lines. A single-ended impedance of 50 Ω is typically recommended for coaxial interconnect, and a differential impedance of 100 Ω is typically recommended for STP interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

10.1.1 CSI-2 Guidelines

1. Route CSI0_D*P/N pairs with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Keep the length difference between a differential pair to 5 mils of each other.
4. Make sure that length matching is near the location of mismatch.
5. Match trace lengths between the clock pair and each data pair to be < 25 mils.
6. Separate each pair by at least 3 times the signal trace width.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on the same layer to help match trace impedance characteristics.
9. Keep the number of VIAS to a minimum—TI recommends keeping the VIA count to two or fewer.
10. Keep traces on layers adjacent to ground plane.
11. Do NOT route differential pairs over any plane split.

注

Adding test points can cause impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

10.2 Layout Examples

Figures below 図 10-1, 図 10-2, and 図 10-3 are examples are taken from the layout of an FPD-Link EVM board. All EVM layers are included in *DS90UB953-Q1EVM user's guide* (SNLU224). Note that the DS90UB953-Q1 shares this user guide with other related products such as the DS90UB635-Q1.

Routing the FPD-Link III signal traces between the DOUT pins and the connector, as well as connecting the PoC filter to these traces, are the most critical pieces of a successful DS90UB635-Q1 PCB layout. The following list provides essential recommendations for routing the FPD-Link III signal traces between the driver output pins and the FAKRA connector, as well as connecting the PoC filter.

- The routing of the FPD-Link III traces may be all on the top layer or partially embedded in middle layers if EMI is a concern.
- The AC-coupling capacitors should be on the top layer and very close to the receiver input pins to minimize the length of coupled differential trace pair between the pins and the capacitors.
- Route the DOUT+ trace between the AC-coupling capacitor and the FAKRA connector as a 50-Ω single-ended micro-strip with tight impedance control (±10%). Calculate the proper width of the trace for a 50-Ω impedance based on the PCB stack-up. Ensure that the trace can carry the PoC current for the maximum load presented by the remote sensor module.
- The PoC filter should be connected to the DOUT+ trace through the ferrite bead or an RF inductor. The ferrite bead should be touching the high-speed trace to minimize the stub length seen by the transmission line. Create an anti-pad or a moat under the ferrite bead pad that touches the trace. The anti-pad should be a plane cutout of the ground plane directly underneath the top layer without cutting out the ground reference under the trace. The purpose of the anti-pad is to maintain the impedance as close to 50 Ω as possible.
- When routing DOUT+ on inner layers, length matching for single-ended traces does not provide a significant benefit. If the user wants to route the DOUT+ on the top or bottom layer, route the DOUT– trace loosely coupled to the DOUT+ trace for the length similar to the DOUT+ trace length. This may help the differential nature of the receiver to cancel out any common-mode noise that may be present in the environment that may couple on to the signal traces.

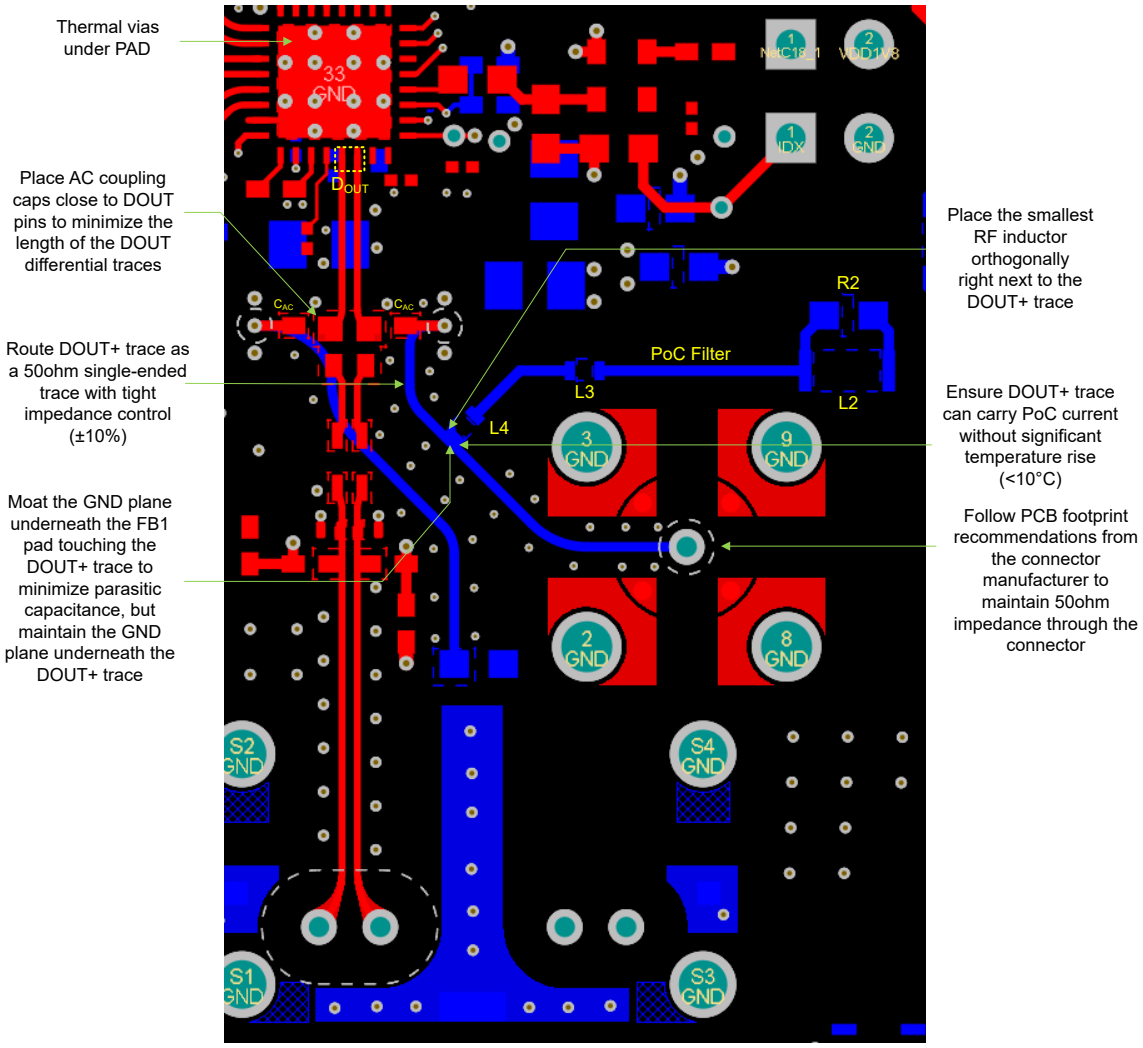

図 10-1. DS90UB635-Q1 Serializer DOUT+ Signal Traces and PoC Filter PCB Layout Example

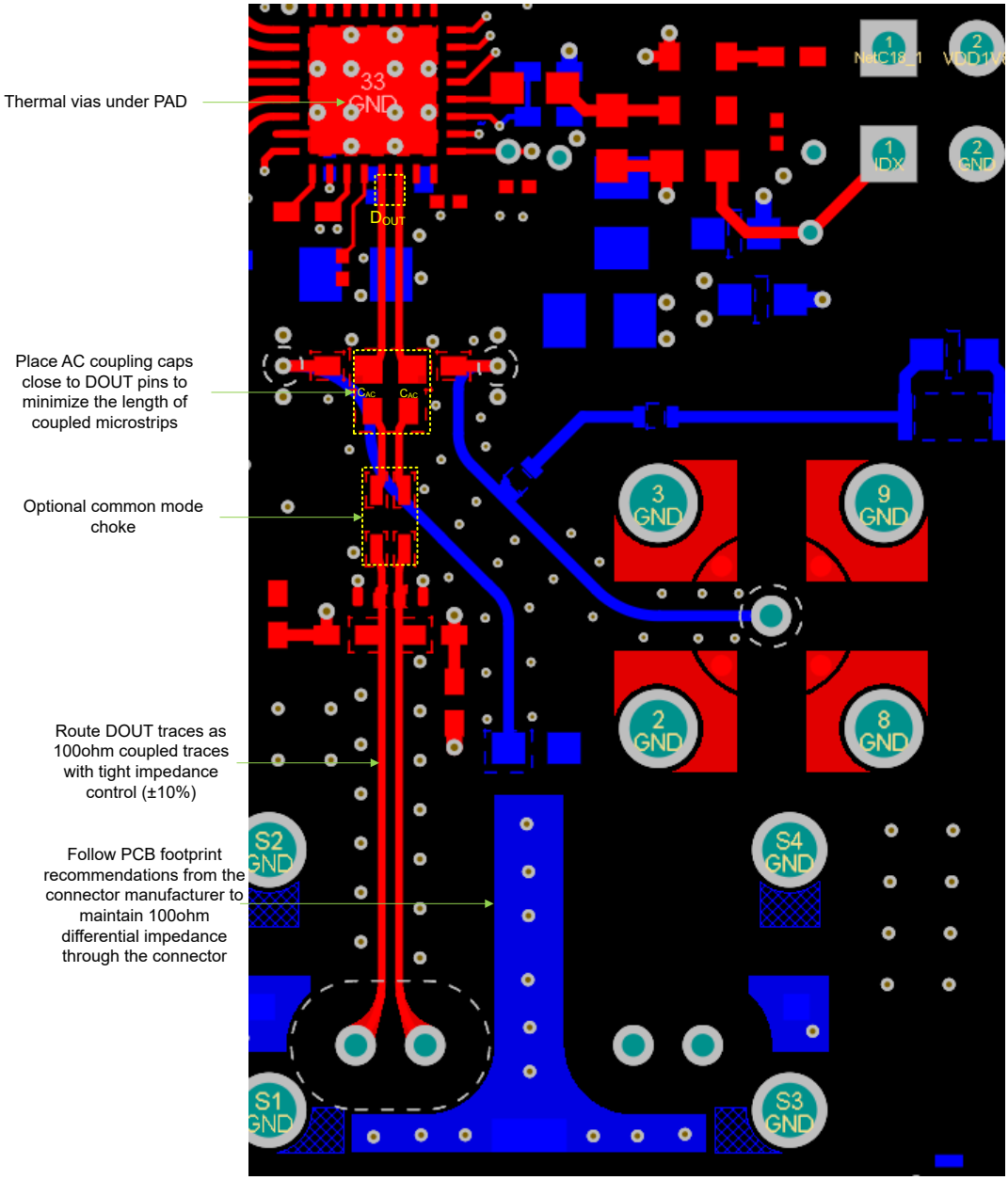

図 10-2. DS90UB635-Q1 Serializer Differential Signal Traces PCB Layout Example

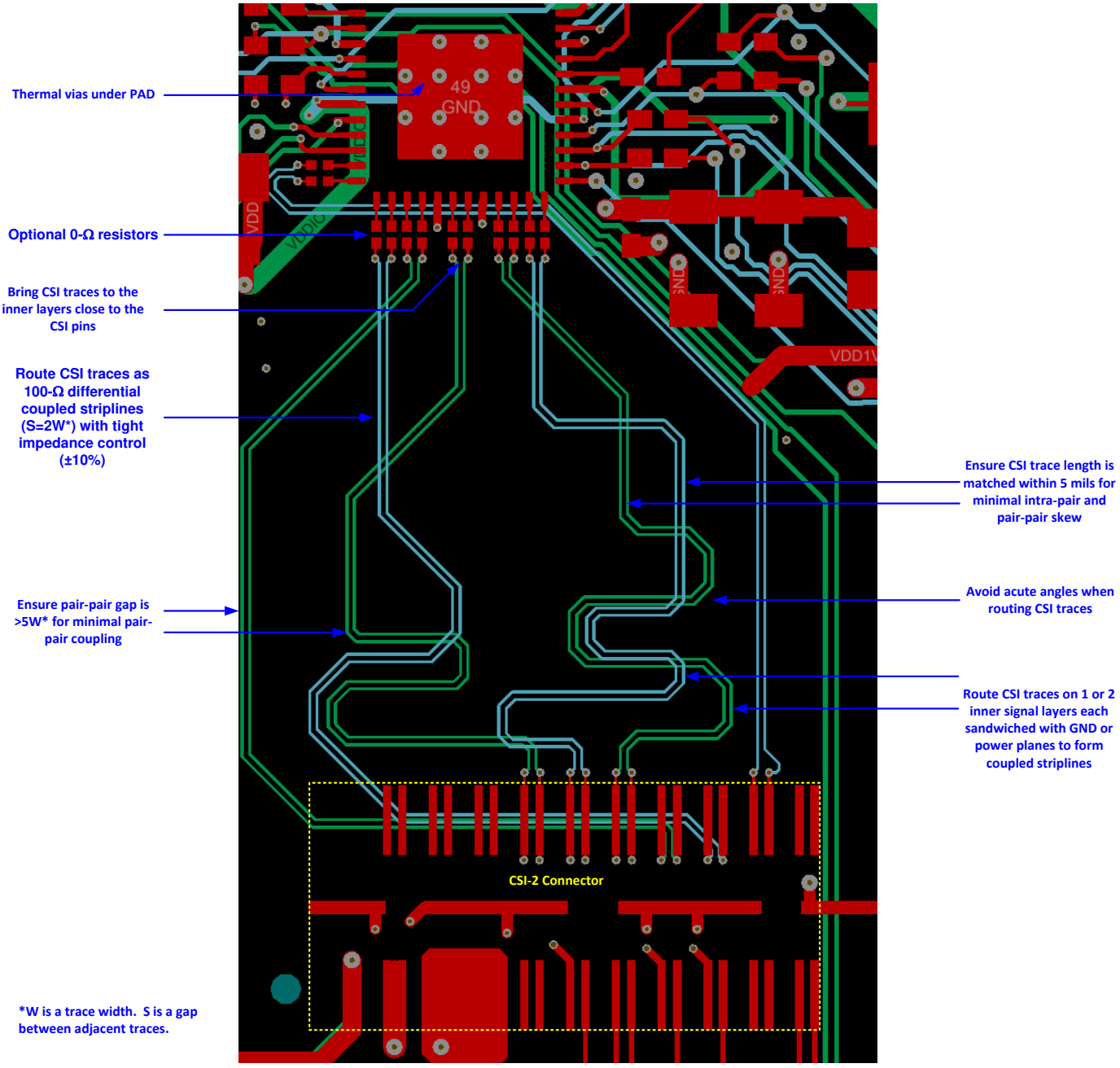

図 10-3. DS90UB635-Q1 Serializer CSI-2 Traces PCB Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *How to design a FPD-Link III system* (SNLA267)
- *I2C communication over FPD-Link III with bidirectional control channel* (SNLA131)
- *I2C bus pullup resistor calculation* (SLVA689)
- *I2C over DS90UB913/4 FPD-Link III with bidirectional control channel* (SNLA222)
- *Sending Power-over-Coax in DS90UB913A designs* (SNLA224)
- FPD-Link learning center training material
- *An EMC/EMI system-design and testing methodology for FPD-Link III SerDes* (SLYT719)
- *Ten tips for successfully designing with automotive EMC/EMI requirements* (SLYT636)
- *Backwards compatibility modes for operation with parallel output deserializers* (SNLA270)
- *Power-over-Coax design guidelines* (SNLA272)
- *AN-1108 Channel-link PCB and interconnect design-in guidelines* (SNLA008)
- *DS90UB953-Q1EVM user's guide* (SNLU224)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB635TRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 105	UB635	Samples
DS90UB635TRHBTQ1	ACTIVE	VQFN	RHB	32	250	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 105	UB635	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

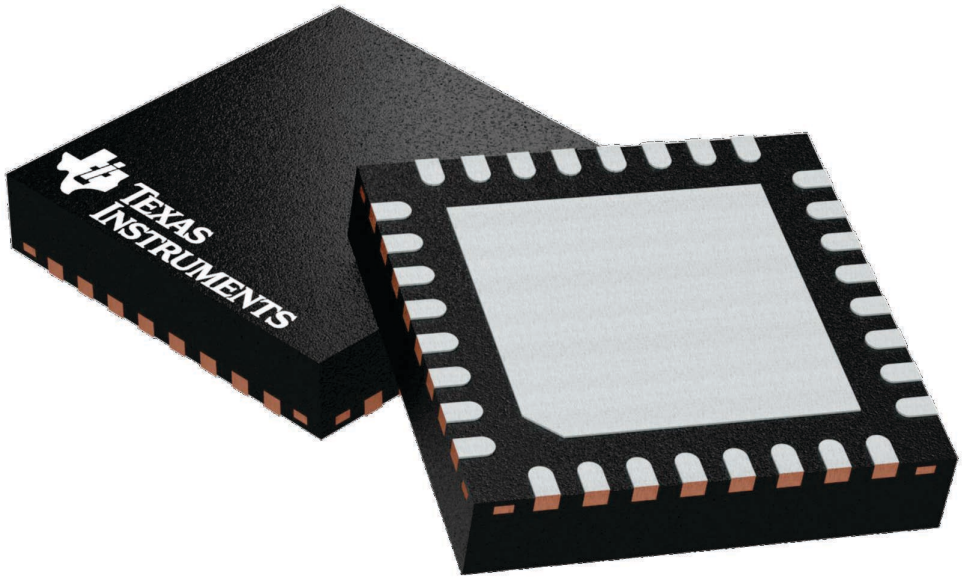
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

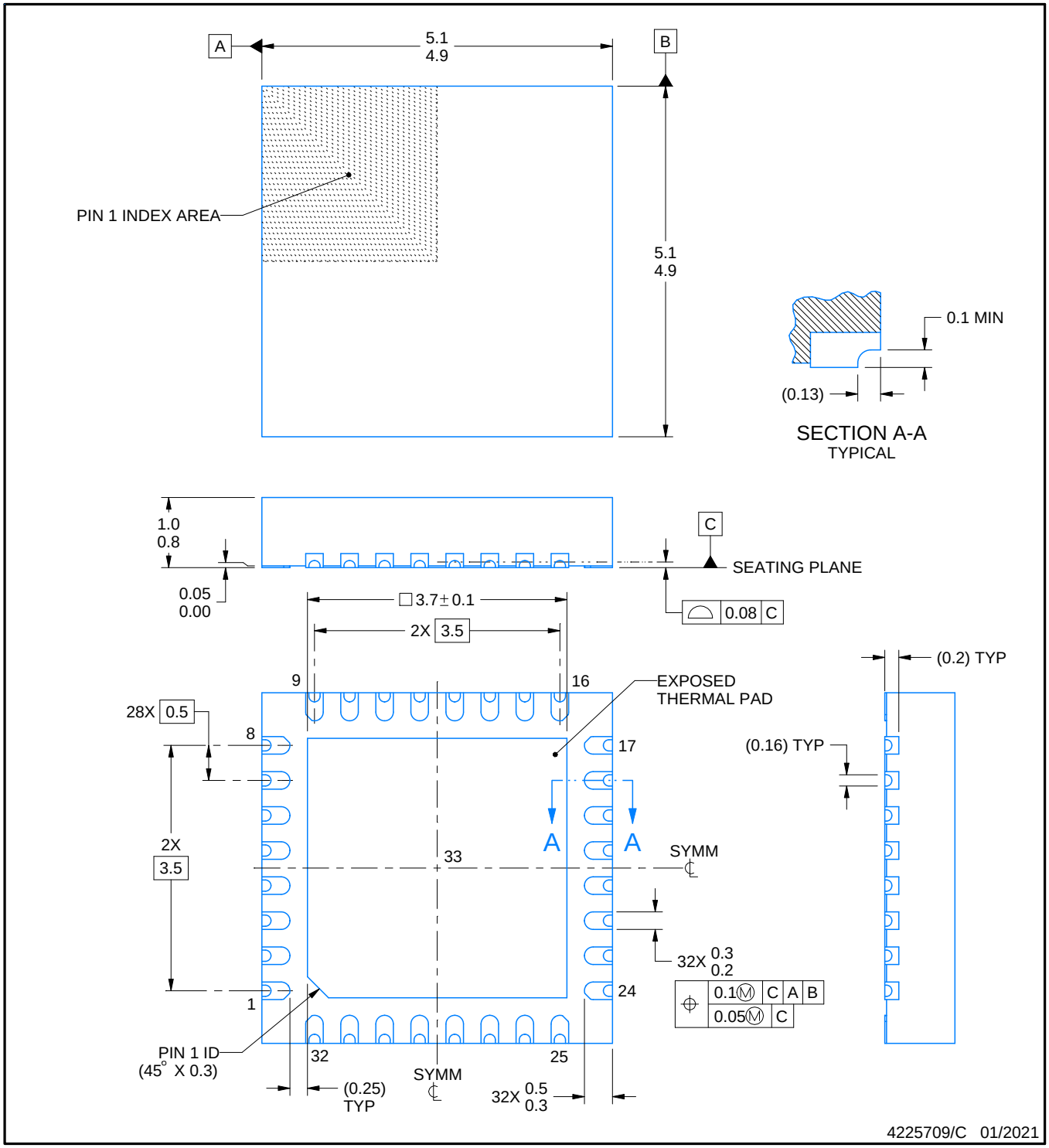
4224745/A

RHB0032U

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

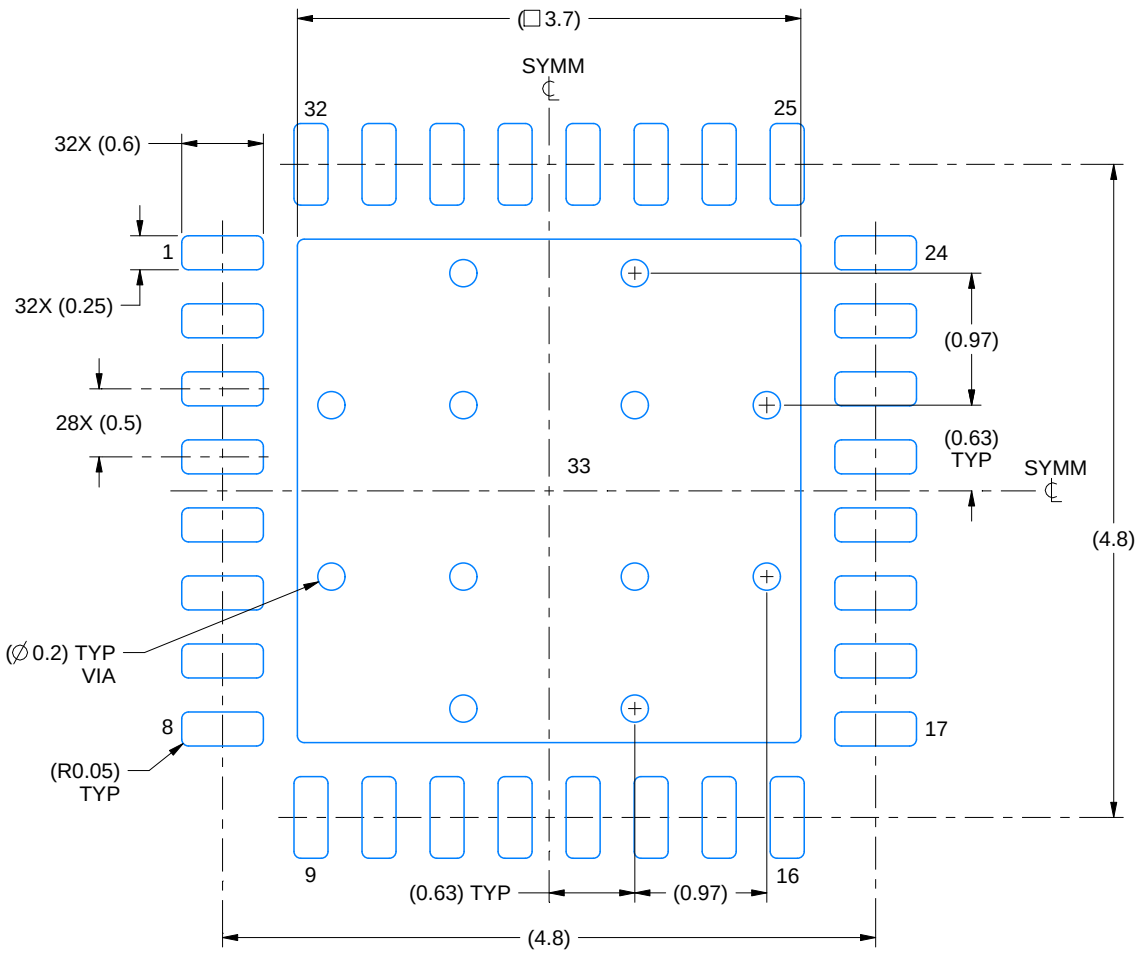
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

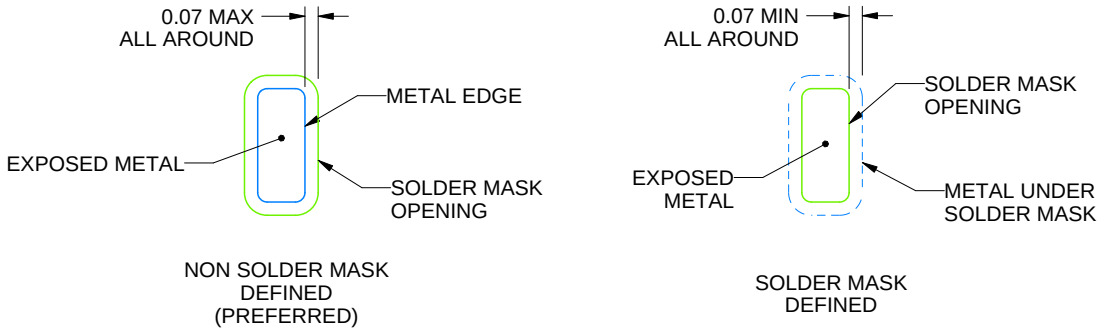
RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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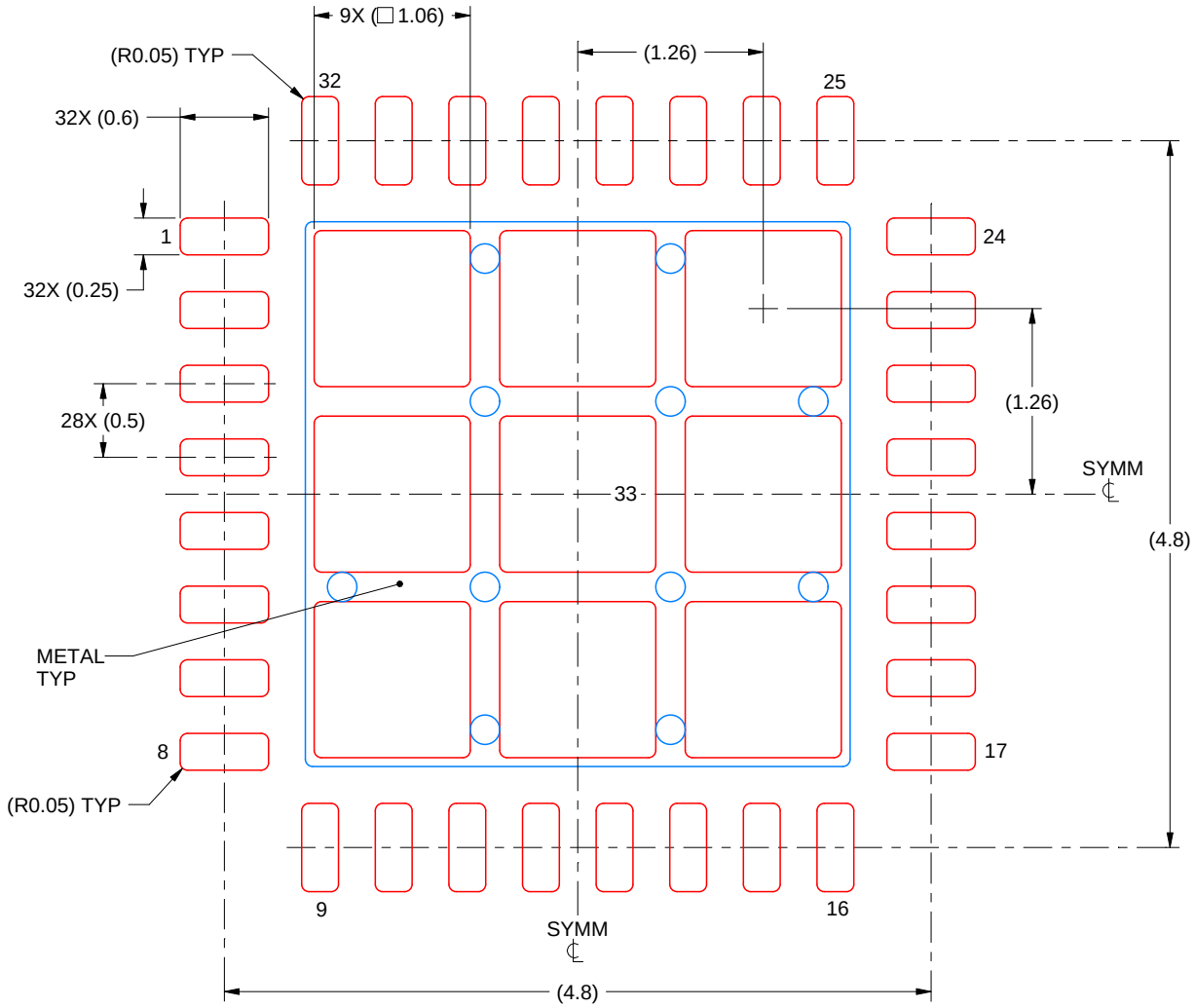
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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