DS90LVRA2 LVDS デュアル差動ライン・レシーバ

1 特長

- 600Mbps (300MHz) を超えるスイッチング速度
- 差動スキュー:50ps (標準値)
- チャネル間スキュー:0.1ns (標準値)
- 1.8V 電源
- フロースルーのピン配置
- 電源オフ時に高インピーダンスになる LVDS 入力
- 出力スルーレート制御
- LVDS 入力は LVDS/CML/LVPECL 信号に対応
- ANSI/TIA/EIA-644 規格に準拠
- DS90LV028A-Q1 とピン互換
- OPN バリアント
  - 標準:0℃～70℃
  - 産業用:–40℃～+85℃

2 アプリケーション

- 通信機器
- エンタープライズ・システム
- 産業用
- パーソナル・エレクトロニクス

3 概要

DS90LVRA2 は、デュアル CMOS 差動ライン・レシーバであり、広い入力同相範囲、高いデータ・レート、スルーレート制御付き CMOS 出力を必要とするアプリケーション向けに設計されています。このデバイスは、低電圧差動信号 (LVDS) テクノロジを活用して、600Mbps (300MHz) のデータ速度をサポートするよう設計されています。

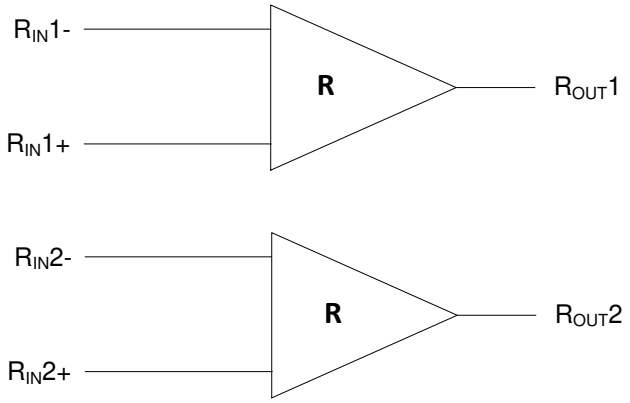
DS90LVRA2 は、低電圧 (標準値 350mV) の差動入力信号を受信し、1.8V CMOS 出力レベルへ変換します。DS90LVRA2 は、フロースルー設計を採用しており、PCB レイアウトが容易です。

DS90LVRA2 およびこれと対になる LVDS ライン・ドライバ DS90LV027AQ は、消費電力の大きい PECL/ECL デバイスの新しい代替品として、高速のポイント・ツー・ポイント・インターフェイス・アプリケーションに使用できます。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DS90LVRA2	DEM (WSON、8)	2.00mm × 2.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ダイアグラム

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4 Revision History

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Pin Configuration and Functions

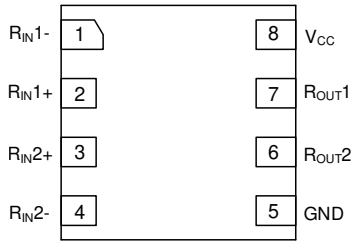


図 5-1. DEM Package, WSON 8 Pin (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	5	G	Ground pin
$R_{IN}1-$	1	I	Inverting receiver input pin
$R_{IN}2-$	4	I	
$R_{IN}1+$	2	I	Non-inverting receiver input pin
$R_{IN}2+$	3	I	
$R_{OUT}2$	6	O	Receiver output pin
$R_{OUT}1$	7	O	
V_{CC}	8	P	Power supply pin

(1) I = input, O = output, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply Voltage (V_{CC})		–0.3	4	V
Input Voltage (R_{IN}+, R_{IN}−)		–5	6	V
Differential Voltage (R_{IN}+ - R_{IN}−) for LVDS		0	3	V
Output Voltage (R_{OUT})		–0.3	1.98	V
Lead Temperature Range Soldering	(4 sec.)		260	°C
Maximum Junction Temperature			135	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended* Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, and performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±5000	V
		Charged-device model (CDM), per JEDEC specification JS-002[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (1.8 V mode)	1.62	1.80	1.98	V
V_R	Receiver input voltage (LVDS)	0		3.0	V
T_A	Operating free-air temperature (Standard)	0		70	°C
T_A	Operating free-air temperature (Industrial)	–40		85	°C
T_{PCB}	PCB temperature (Standard)			80	°C
T_{PCB}	PCB temperature (Industrial)			95	°C
T_J	Junction temperature (Standard)			95	°C
T_J	Junction temperature (Industrial)			110	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		DEM (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	143.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ITH}	Positive-going differential input voltage threshold	V_{IB} = -1 V or 2 V, VCC = 1.62 V to 1.98 V			100	mV
V_{ITL}	Negative-going differential input voltage threshold		-100			
V_{HYS}	Differential input voltage hysteresis, $V_{IT1} – V_{IT2}$	VCC = 1.62 V to 1.98 V	20	40	90	mV
V_{CM_RANGE}	Input common mode voltage range	VCC = 1.62 - 1.98 V	-1	1.2	2	V
V_{OH_1V8}	High-level output voltage	I_{OH} = –4 mA, VCC=1.8 V ±10%	1.3			V
V_{OL_1V8}	Low-level output voltage	I_{OL} = 4 mA, VCC=1.8 V ±10%			0.2	V
I_{CC_ACTIVE}	Supply current	V_{CC} = 1.98 V, No load, Steady-state, VID=200 mV/-200 mV			25	mA
I_I	Input current (A or B inputs)	V_I = -1.0 V, Other input open			±35	µA
I_I	Input current (A or B inputs)	V_I = 2.0 V, Other input open			±20	µA
$I_{I(OFF)}$	Power-off output current (Y or Z outputs)	V_Y or V_Z = 1.98 V, V_{CC} = 0 V			±20	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_A or V_B = -1 V or 2.0 V, V_{CC} = 0 V			±35	µA

(1) All typical values are at 25°C and with a 1.8 V supply.

6.6 Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(2) (3) (4)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
t_{PHLD_1p8}	Differential Propagation Delay High to Low	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC 1.8 V ±10%	2.7	4.3	7.7	ns
$t_{PHLD\_1p8\_5}$	Differential Propagation Delay High to Low	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC 1.8 V ±5%	2.8	4.3	7.1	ns
t_{PLHD_1p8}	Differential Propagation Delay Low to High	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC 1.8 V ±10%	2.7	4.4	7.7	ns
$t_{PLHD\_1p8\_5}$	Differential Propagation Delay Low to High	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC 1.8 V ±5%	2.8	4.4	7.1	ns
$t_{SKD1\_1p8\_S}$	Differential Pulse Skew ($t_{PHLD} – t_{PLHD}$)((7))	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC=1.8 V±10%	-500		500	ps
$t_{SKD1\_1p8\_5\_S}$	Differential Pulse Skew ($t_{PHLD} – t_{PLHD}$)((7))	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC=1.8 V±5%	-400		400	ps
$t_{SKD1\_1p8\_S\_400M}$	Differential Pulse Skew ($t_{PHLD} – t_{PLHD}$) ((7))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns DR=400M, VCC=1.8 V±10%	-500		500	ps
$t_{SKD1\_1p8\_5\_S\_400M}$	Differential Pulse Skew ($t_{PHLD} – t_{PLHD}$) ((7))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns DR=400M,VCC=1.8 V±5%	-400		400	ps
t_{SKD2_1p8}	Differential Channel-to-Channel Skew-same device (6)	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±10%			0.5	ns

6.6 Switching Characteristics (continued)

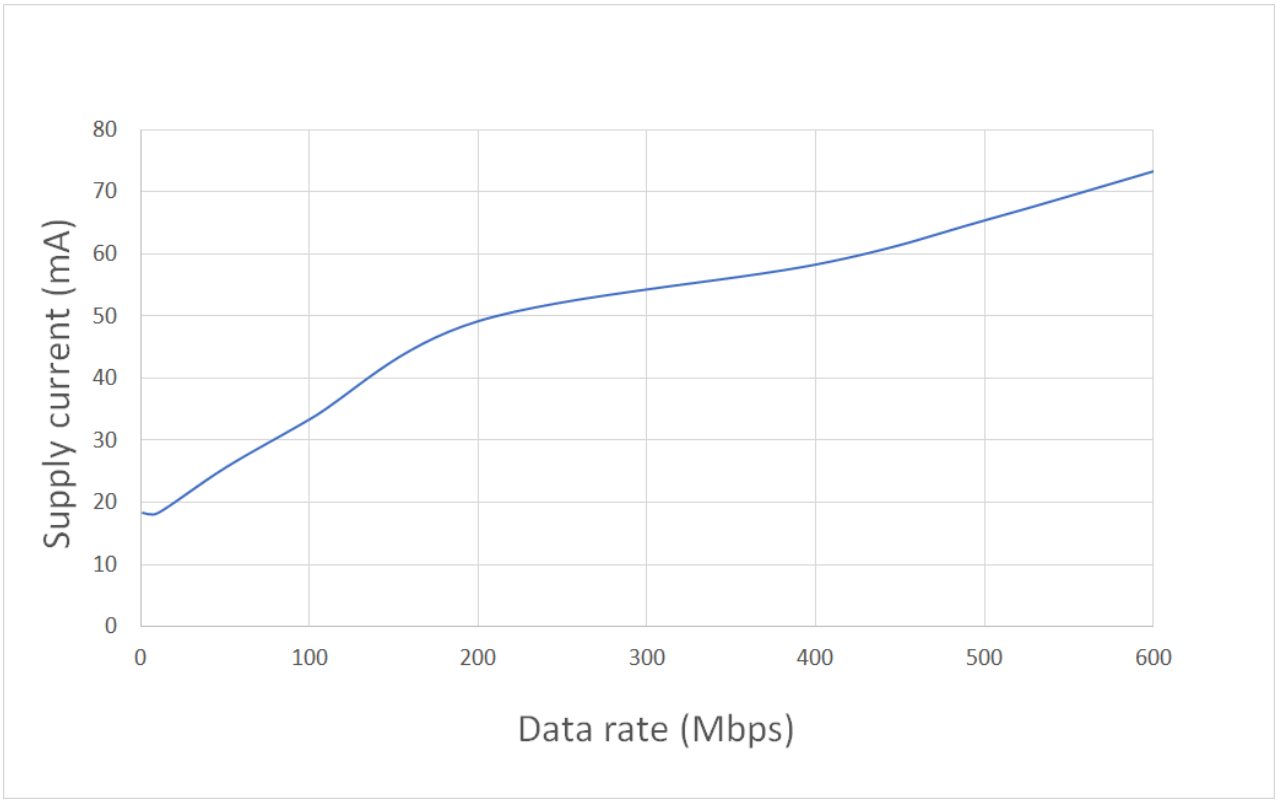
Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(2) (3) (4)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$t_{SKD2\_1p8\_5}$	Differential Channel-to-Channel Skew-same device ((8))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5%			0.4	ns
$t_{SKD3\_1p8\_5}$	Differential Part to Part Skew ((9))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5% at same temperature			2.7	ns
$t_{SKD3\_1p8\_5\_25C}$	Differential Part to Part Skew ((9))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5% at TJ =25℃			2.6	ns
$t_{SKD3\_1p8\_5\_70C}$	Differential Part to Part Skew ((9))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5% at TJ =70℃			2.7	ns
$t_{SKD3\_1p8\_5\_125C}$	Differential Part to Part Skew ((9))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5% at TJ= 125℃			2.7	ns
t_{TLH_1p8}	Rise Time		250	500	720	ps
t_{THL_1p8}	Fall Time		250	500	720	ps
f_{MAX}	Maximum Operating Frequency ((11))		300			MHz

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
(2) All typicals are given for: V_{CC} = 1.8V and T_A = +25°C.
(3) C_L includes probe and jig capacitance.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
(5) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(6) t_{SKD2} is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(7) t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(8) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max), V_{OH} (min), load = 15 pF (stray plus probes).

6.7 Typical Characteristics

Typical power supply current -vs- data rate (VCC 1.8 V, 5 pF output load, 2 channels)



7 Parameter Measurement Information

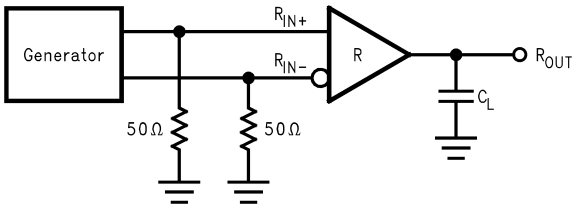


図 7-1. Receiver Propagation Delay and Transition Time Test Circuit

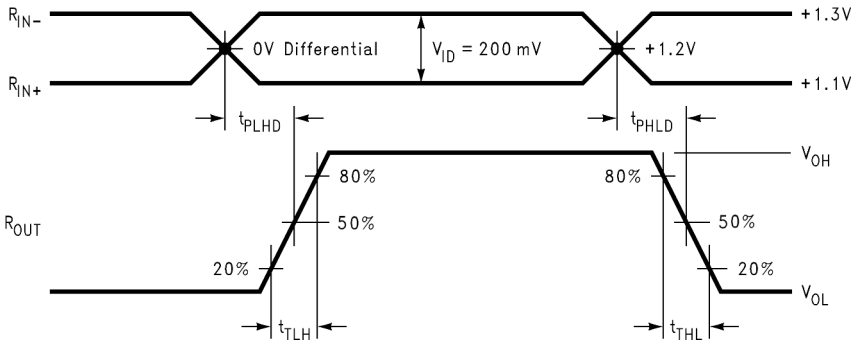


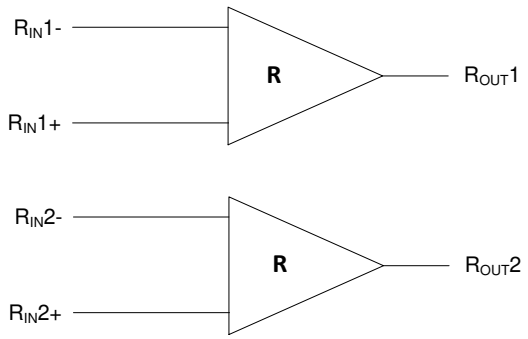
図 7-2. Receiver Propagation Delay and Transition Time Waveforms

8 Detailed Description

8.1 Overview

図 9-1 shows how LVDS drivers and receivers are intended to be primarily used in a simple point-to-point configuration. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the source through a impedance controlled 100 Ω differential PCB traces. A termination resistor of 100 Ω should be used, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver.

8.2 Functional Block Diagram



8.3 Feature Description

The DS90LVRA2 differential line receiver is capable of detecting signals as low as 100 mV, over a common-mode range of −1 V to 2 V (V_{CC} at 1.8 V). This is related to the driver offset voltage which is typically +1.2 V. The driven signal is centered around this voltage and may shift around this center point. The shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of +0 V to +3 V (measured from each pin to ground).

8.4 Device Functional Modes

表 8-1. Truth Table

INPUTS	OUTPUT
$[R_{IN}+] - [R_{IN}-]$	R_{OUT}
$V_{ID} \geq 0.1$ V	H
$V_{ID} \leq -0.1$ V	L
-0.1 V $\leq V_{ID} \leq 0.1$ V	?(1)

(1) ? indicates state is indeterminate

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

For general application guidelines and hints about LVDS drivers and receivers, refer to the *LVDS application notes and design guides*.

9.2 Typical Application

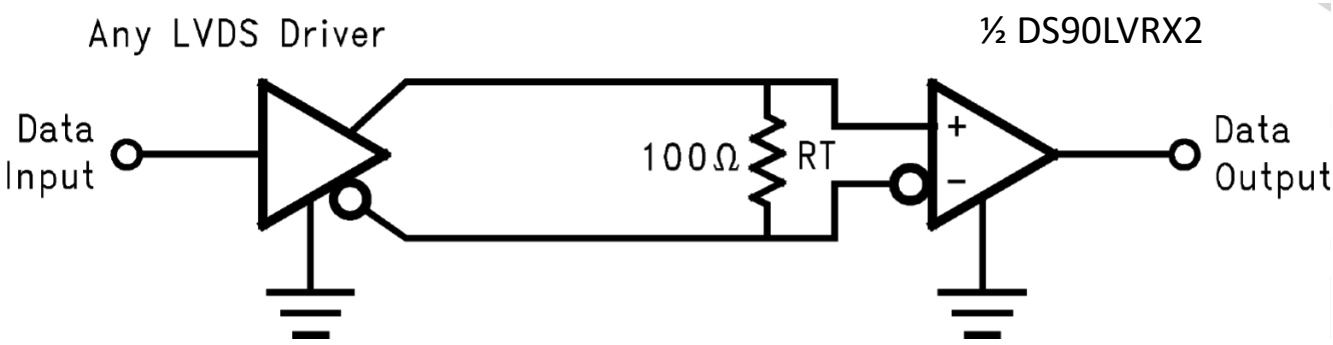


図 9-1. Balanced System Point-to-Point Application

9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces. All components of the transmission media must have a matched differential impedance of 100 Ω. They must not introduce major impedance discontinuities.

9.2.2 Detailed Design Procedure

9.2.2.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1 µF and 0.01 µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10 µF (35 V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

9.2.2.2 Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90 Ω and 110 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10 mm (12 mm maximum).

9.2.2.3 Input Failsafe Biasing

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5 kΩ to 15 kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2 V to be compatible with the internal circuitry. For more information, refer to application note AN-1194 *Failsafe Biasing of LVDS Interfaces*.

9.2.2.4 Probing LVDS Transmission Lines

Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

9.3 Application Curves

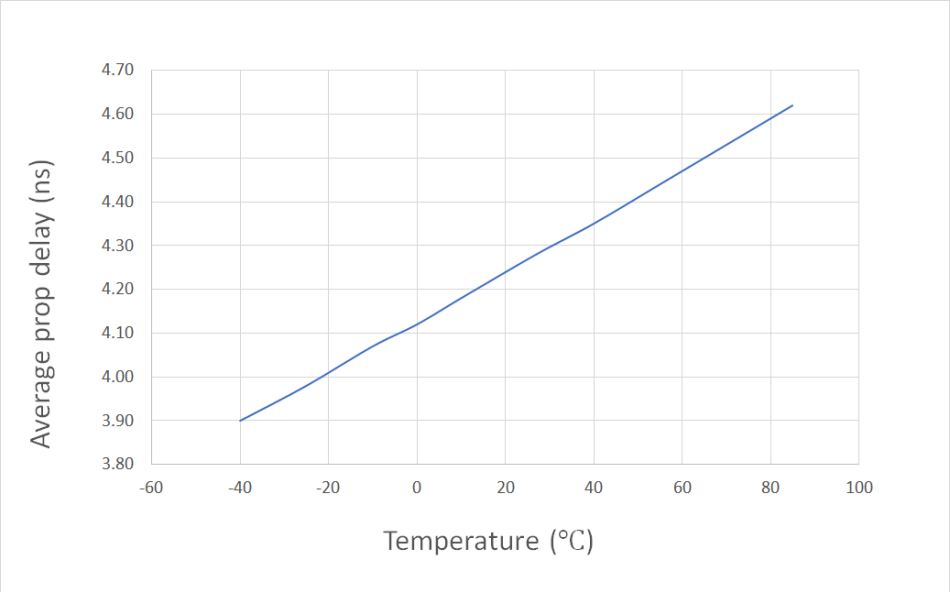


図 9-2. Typical Propagation Delay -vs- Temperature (VCC 1.8 V, 10 pF Output Load, Average of 2 Channels)

10 Power Supply Recommendations

Bypass capacitors must be used on power pins. TI recommends using high-frequency, ceramic, 0.1-µF and 0.01-µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-µF bulk capacitor, 35-V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.

11 Layout

11.1 Layout Guidelines

11.1.1 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission trace and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10 mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. It is important to note: skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note that the velocity of propagation, v = c/E $_r$ where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

11.1.2 PC Board Considerations

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, and TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by one or more power or ground planes.

11.2 Layout Examples

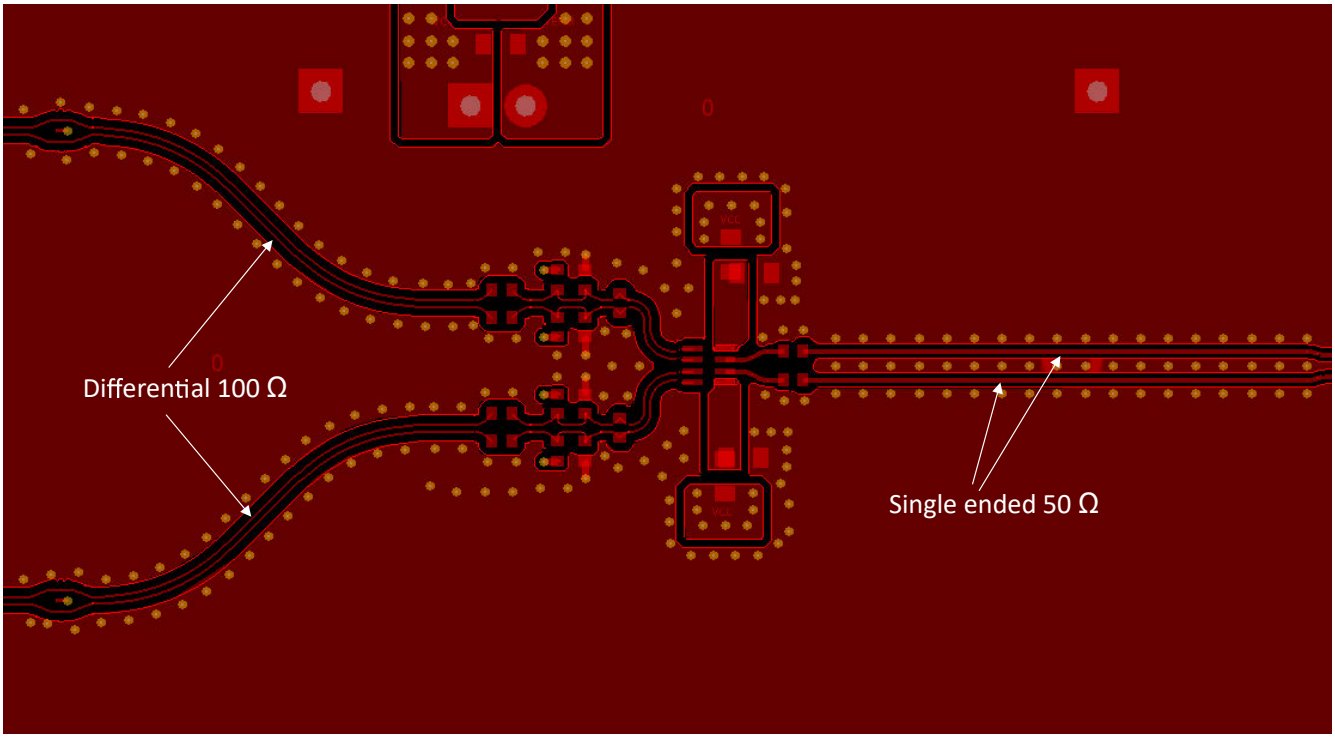


図 11-1. EVM Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Failsafe Biasing of LVDS Interfaces* application note

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.4 Trademarks

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12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
D9LVRA2DEMR	ACTIVE	WSON	DEM	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LR2	Samples
D9LVRA2DEMT	ACTIVE	WSON	DEM	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LR2	Samples
D9LVRA2IDEMR	ACTIVE	WSON	DEM	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LR2	Samples
D9LVRA2IDEMT	ACTIVE	WSON	DEM	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LR2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

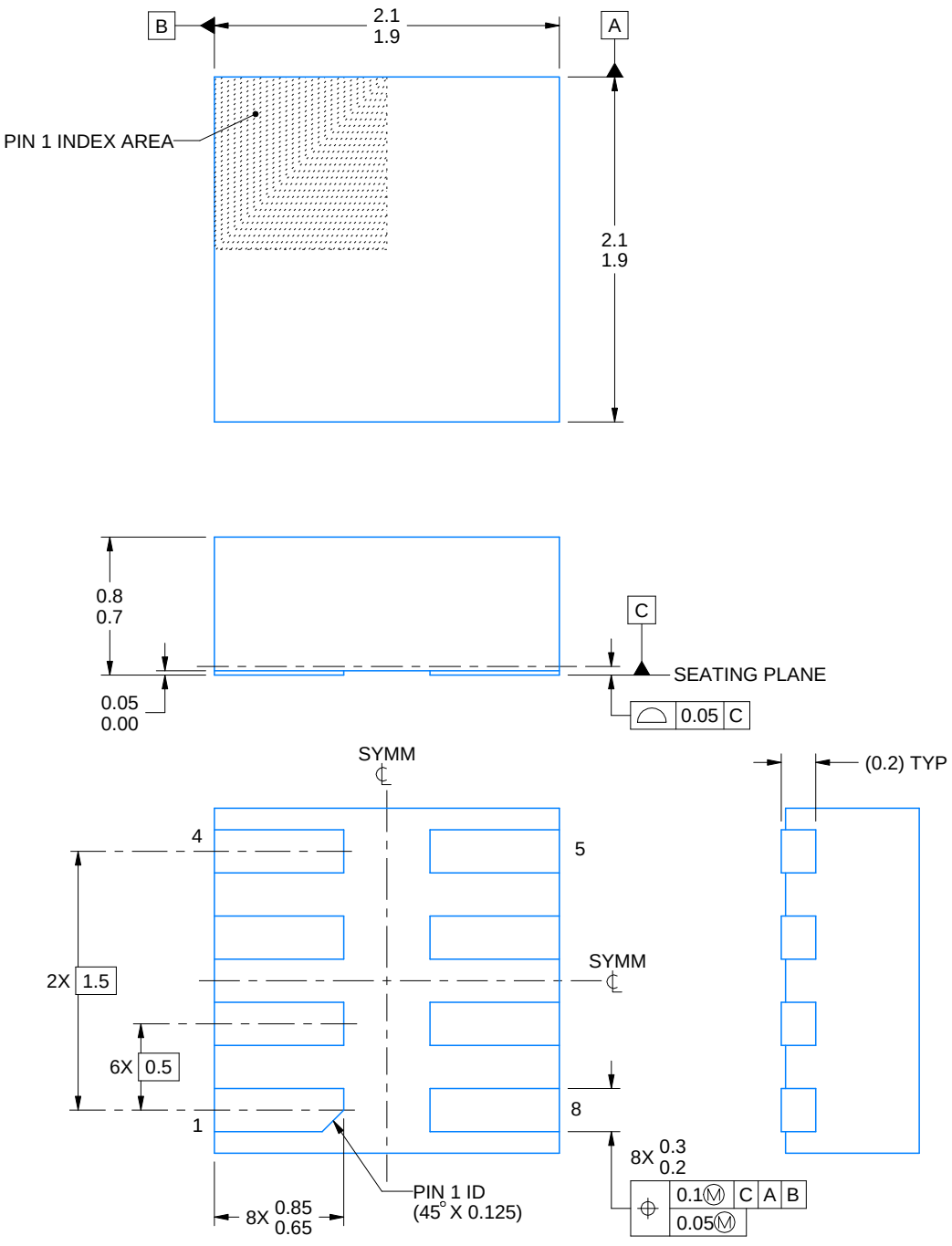
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DEM0008A

PACKAGE OUTLINE

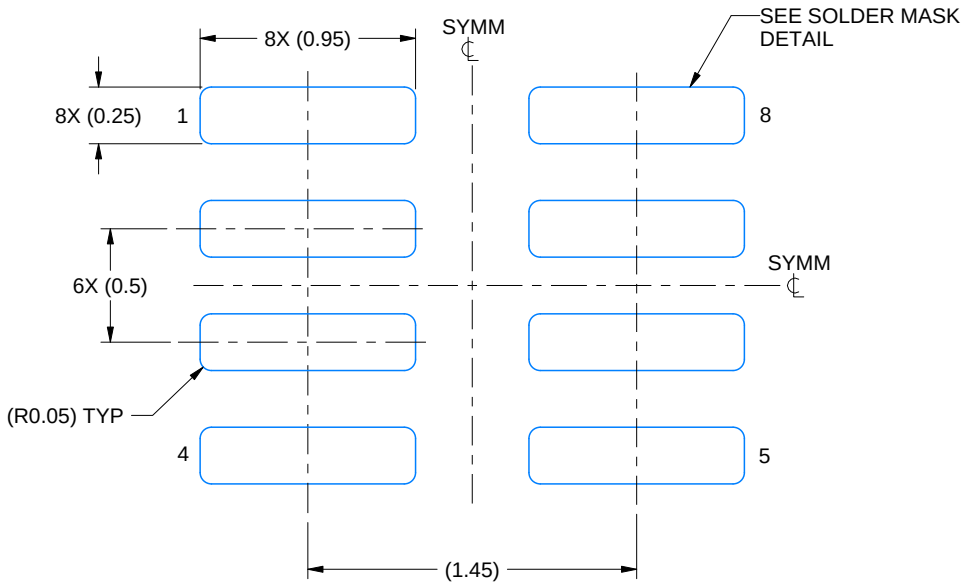
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

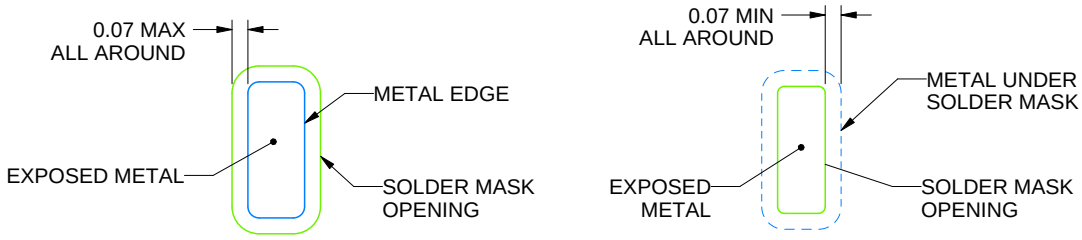


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

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NOTES: (continued)

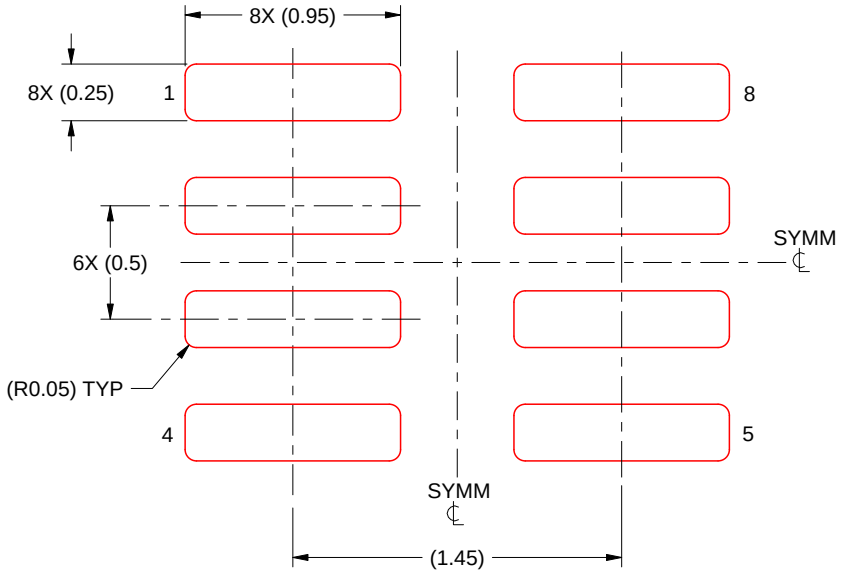
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DEM0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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