TEXAS INSTRUMENTS

DRV8770：100V ブラシ付き DC ゲート・ドライバ

1 特長

- 100V H ブリッジ・ゲート・ドライバ
  - N チャネル MOSFET (NMOS) を駆動
  - ゲート・ドライバ電源 (GVDD)：5～20V
  - MOSFET 電源 (SHx) をサポート：最大 100V
- ブートストラップ・ダイオードを内蔵
- 反転および非反転 INLx 入力をサポート (QFN パッケージ)
- ブートストラップ・ゲート駆動アーキテクチャ
  - 750mA のソース電流
  - 1.5A のシンク電流
- 最大 15S のバッテリ駆動アプリケーションをサポート
- SHx ピンの低リーク電流 (55µA 未満)
- BSTx 電圧の絶対最大定格：115V
- SHx ピンで -22V までの負過渡電圧をサポート
- DT ピンでデッドタイムを調整可能 (QFN パッケージ)
- 200ns の固定デッドタイム挿入 (TSSOP パッケージ)
- 3.3V および 5V ロジック入力 (絶対最大定格 20V) をサポート
- 4ns (代表値) の伝搬遅延マッチング
- 小型の QFN および TSSOP パッケージおよびフットプリント
- パワー・ブロックによる効率的なシステム設計
- 保護機能内蔵
  - BST 低電圧誤動作防止 (BSTUV)
  - GVDD 低電圧 (GVDDUV)

2 アプリケーション

- 電動アシスト自転車、電動スクーター、E モビリティ
- コードレス園芸用器具および電動工具、芝刈り機
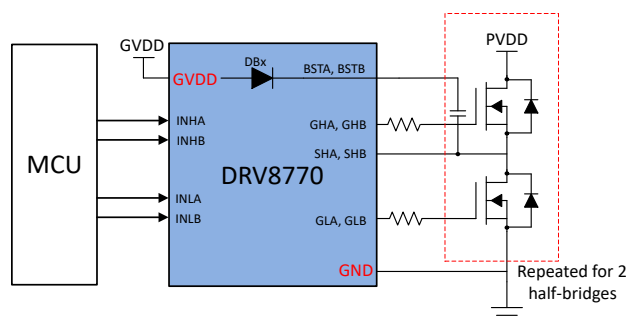- コードレス掃除機
- ドローン、ロボティクス、ラジコン玩具
- 産業用および物流用ロボット
- 電動工具

3 概要

DRV8770 デバイスは 2 個のハーフブリッジ・ゲート・ドライバを搭載しており、それぞれがハイサイドとローサイドの各 N チャネル・パワー MOSFET を駆動する能力があります。GVDD がローサイド MOSFET のゲートを駆動する一方、内蔵ブートストラップ・ダイオードと外付けコンデンサはハイサイド MOSFET のための適切なゲート駆動電圧を生成します。このゲート駆動アーキテクチャは最大でソース 750mA、シンク 1.5A のゲート駆動電流をサポートしています。

ゲート駆動ピンの高い許容電圧はシステムの堅牢性を高めます。SHx 位相ピンは大きな負電圧過渡に耐えます。一方、ハイサイド・ゲート・ドライバ電源は BSTx および GHx ピンのさらに大きな正電圧過渡 (絶対最大定格電圧 115V) に対応できます。伝搬遅延が短く、遅延マッチング仕様によりデッドタイムの要件が最小化されるため、さらに効率が向上します。GVDD と BST の低電圧誤動作防止による低電圧保護機能がローサイドとハイサイドの両方に備わっています。

製品情報[1]

部品番号	パッケージ	本体サイズ (公称)
DRV8770PW	TSSOP (20)	6.40mm × 4.40mm
DRV8770RGE	VQFN (24)	4.00mm × 4.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図 (DRV8770)

English Data Sheet: SLVSFL8

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
July 2021	*	Initial Release

Product Folder Links: *DRV8770*
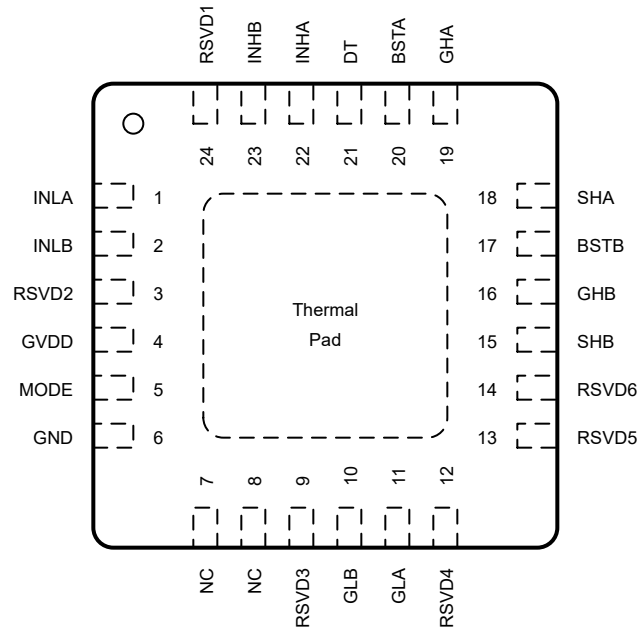
5 Pin Configuration and Functions

図 **5-1. DRV8770 RGE Package 24-Pin VQFN With Exposed Thermal Pad Top View**

表 **5-1. Pin Functions—24-Pin DRV8770 Device**

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BSTA	20	O	Bootstrap output pin. Connect capacitor between BSTA and SHA
BSTB	17	O	Bootstrap output pin. Connect capacitor between BSTB and SHB
DT	21	I	Deadtime input pin. Connect resistor to ground for variable deadtime, fixed deadtime when left it floating
GHA	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	11	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GND	6	PWR	Device ground.
GVDD	4	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.
INHA	22	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	23	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	1	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	2	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	5	I	Mode Input controls polarity of GLx compared to INLx inputs. Mode pin floating: GLx output polarity same(Non-Inverted) as INLx input Mode pin to GVDD: GLx output polarity inverted compared to INLx input
NC	7, 8	NC	No internal connection. This pin can be left floating or connected to system ground.
RSVD1, RSVD2, RSVD3, RSVD5, RSVD6	3, 9, 13, 14, 24	I	TI reserved pin. Leave pin floating.
RSVD4	12	I	TI reserved pin. Connect to GND
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.

(1)   PWR = power, I = input, O = output, NC = no connection

Product Folder Links: *DRV8770*

図 5-2. DRV8770 PW Package 20-Pin TSSOP Top View

表 5-2. Pin Functions—20-Pin DRV8770 Device

PIN NAME	PIN NO.	TYPE[1]	DESCRIPTION
BSTA	20	O	Bootstrap output pin. Connect capacitor between BSTA and SHA
BSTB	17	O	Bootstrap output pin. Connect capacitor between BSTB and SHB
GHA	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	11	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GND	8	PWR	Device ground.
GVDD	7	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.
INHA	1	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	2	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	4	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	5	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
RSVD1, RSVD2, RSVD3, RSVD5, RSVD6	3, 6, 9, 13, 14	I	TI reserved pin. Leave pin floating.
RSVD4	12	I	TI reserved pin. Connect to GND
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.

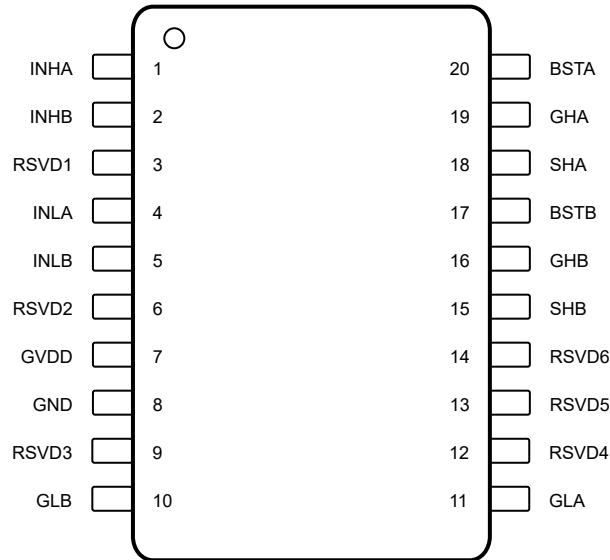(1)   PWR = power, I = input, O = output, NC = no connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Gate driver regulator pin voltage	GVDD	-0.3	21.5	V
Bootstrap pin voltage	BSTx	-0.3	115	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	21.5	V
Logic pin voltage	INHx, INLx, MODE, DT	-0.3	V_{GVDD}+0.3	V
High-side gate drive pin voltage	GHx	-22	115	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	22	V
Transient 500-ns high-side gate drive pin voltage	GHx with respect to SHx	-5	22	V
Low-side gate drive pin voltage	GLx	-0.3	V_{GVDD}+0.3	V
Transient 500-ns low-side gate drive pin voltage	GLx	-5	V_{GVDD}+0.3	V
High-side source pin voltage	SHx	-22	100	V
Ambient temperature, T_A		−40	125	°C
Junction temperature, T_J		−40	150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings Comm

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{GVDD}	Power supply voltage	GVDD	5		20	V
V_{SHx}	High-side source pin voltage	SHx	-2		85	V
V_{SHx}	Transient 2µs high-side source pin voltage	SHx	-22		85	V
V_{BST}	Bootstrap pin voltage	BSTx	5		105	V
V_{BST}	Bootstrap pin voltage	BSTx with respect to SHx	5		20	V
V_{IN}	Logic input voltage	INHx, INLx, MODE, DT	0		GVDD	V
f_{PWM}	PWM frequency	INHx, INLx	0		200	kHz
V_{SHSL}	Slew rate on SHx pin				2	V/ns
C_{BOOT} [1]	Capacitor between BSTx and SHx				1	µF
T_A	Operating ambient temperature		−40		125	°C
T_J	Operating junction temperature		−40		150	°C

(1) Current flowing through boot diode (D_{BOOT}) needs to be limited for C_{BOOT} > 1µF

Product Folder Links: *DRV8770*

6.4 Thermal Information

	THERMAL METRIC[1]	DRV8770		UNIT
		PW (TSSOP)	RGE (VQFN)	
		20 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.4	49.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	42.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.8	26.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	48.4	26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

$4.8 \text{ V} \leq V_{GVDD} \leq 20 \text{ V}$, $-40°C \leq T_J \leq 150°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (GVDD, BSTx)						
I_{GVDD}	GVDD standby mode current	INHx = INLX = 0; $V_{BSTx} = V_{GVDD}$	400	800	1400	µA
	GVDD active mode current	INHx = INLX = Switching @20kHz; $V_{BSTx} = V_{GVDD}$; NO FETs connected	400	825	1400	µA
IL_{BSx}	Bootstrap pin leakage current	$V_{BSTx} = V_{SHx} = 85V$; $V_{GVDD} = 0V$	2	4	7	µA
IL_{BS_TRAN}	Bootstrap pin active mode transient leakage current	INHx = Switching@20kHz	30	105	220	µA
IL_{BS_DC}	Bootstrap pin active mode leakage static current	INHx = High	30	85	150	µA
IL_{SHx}	High-side source pin leakage current	INHx = INLX = 0; $V_{BSTx} - V_{SHx} = 12V$; $V_{SHx} = 0$ to 85V	30	55	80	µA
LOGIC-LEVEL INPUTS (INHx, INLx, MODE)						
V_{IL_MODE}	Input logic low voltage	Mode pin			0.6	V
V_{IL}	Input logic low voltage	INLx, INHx pins			0.8	V
V_{IH_MODE}	Input logic high voltage	Mode pin	3.7			V
V_{IH}	Input logic high voltage	INLx, INHx pins	2.0			V
V_{HYS_MODE}	Input hysteresis	Mode pin	1600	2000	2400	mV
V_{HYS}	Input hysteresis	INLx, INHx pins	40	100	260	mV
I_{IL_INLx}	INLx Input logic low current	V_{PIN} (Pin Voltage) = 0 V; INLx in non-inverting mode	-1	0	1	µA
		V_{PIN} (Pin Voltage) = 0 V; INLx in inverting mode	5	20	30	µA
I_{IH_INLx}	INLx Input logic high current	V_{PIN} (Pin Voltage) = 5 V; INLx in non-inverting mode	5	20	30	µA
		V_{PIN} (Pin Voltage) = 5 V; INLx in inverting mode	0	0.5	1.5	µA
I_{IL}	INHx, MODE Input logic low current	V_{PIN} (Pin Voltage) = 0 V;	-1	0	1	µA
I_{IH}	INHx, MODE Input logic high current	V_{PIN} (Pin Voltage) = 5 V;	5	20	30	µA
R_{PD_INHx}	INHx Input pulldown resistance	To GND	120	200	280	kΩ
R_{PD_INLx}	INLx Input pulldown resistance	To GND, INLx in non-inverting mode	120	200	280	kΩ
R_{PU_INLx}	INLx Input pullup resistance	To INT_5V, INLx in inverting mode	120	200	280	kΩ
R_{PD_MODE}	MODE Input pulldown resistance	To GND	120	200	280	kΩ
GATE DRIVERS (GHx, GLx, SHx, SLx)						

Product Folder Links: DRV8770

4.8 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GHx_LO}	High-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V_{GHx_HI}	High-side gate drive high level voltage (V_{BSTx} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
V_{GLx_LO}	Low-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V_{GLx_HI}	Low-side gate drive high level voltage (V_{GVDD} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
I_{DRIVEP_HS}	High-side peak source gate current	GHx-SHx = 12V	400	750	1200	mA
I_{DRIVEN_HS}	High-side peak sink gate current	GHx-SHx = 0V	850	1500	2100	mA
I_{DRIVEP_LS}	Low-side peak source gate current	GLx = 12V	400	750	1200	mA
I_{DRIVEN_LS}	Low-side peak sink gate current	GLx = 0V	850	1500	2100	mA
t_{PD}	Input to output propagation delay	INHx, INLx to GHx, GLx; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	70	125	180	ns
t_{PD_match}	Matching propagation delay per phase	GHx turning OFF to GLx turning ON, GLx turning OFF to GHx turning ON; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	-30	±4	30	ns
t_{PD_match}	Matching propagation delay phase to phase	GHx/GLx turning ON to GHy/GLy turning ON, GHx/GLx turning OFF to GHy/GLy turning OFF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	-30	±4	30	ns
t_{R_GLx}	GLx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t_{R_GHx}	GHx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t_{F_GLx}	GLx fall time (90% to 10%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	5	12	30	ns
t_{F_GHx}	GHx fall time (90% to 10%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	5	12	30	ns
t_{DEAD}	Gate drive dead time	DT pin connected to GND	150	215	280	ns
		40 kΩ between DT pin and GND	150	200	260	ns
		400 kΩ between DT pin and GND	1500	2000	2600	ns
t_{PW_MIN}	Minimum input pulse width on INHx, INLx that changes the output on GHx, GLx		40	70	150	ns
BOOTSTRAP DIODES						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA	0.45	0.7	0.85	V
		I_{BOOT} = 100 mA	2	2.3	3.1	V
R_{BOOTD}	Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$)	I_{BOOT} = 100 mA and 80 mA	11	15	25	Ω
PROTECTION CIRCUITS						
V_{GVDDUV}	Gate Driver Supply undervoltage lockout (GVDDUV)	Supply rising	4.45	4.6	4.7	V
		Supply falling	4.2	4.35	4.4	V
V_{GVDDUV_HYS}	Gate Driver Supply UV hysteresis	Rising to falling threshold	250	280	310	mV
t_{GVDDUV}	Gate Driver Supply undervoltage deglitch time		5	10	13	µs
V_{BSTUV}	Boot Strap undervoltage lockout (V_{BSTx} - V_{SHx})	Supply rising	3.6	4.2	4.8	V
	Boot Strap undervoltage lockout (V_{BSTx} - V_{SHx})	Supply falling	3.5	4	4.5	V

Product Folder Links: *DRV8770*

4.8 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

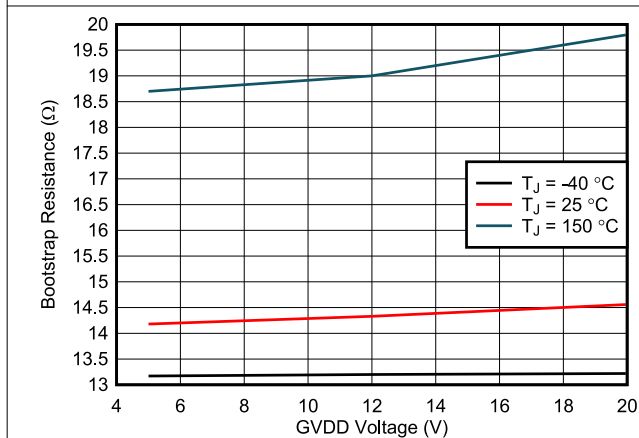| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BSTUV_HYS}	Bootstrap UV hysteresis	Rising to falling threshold		200		mV
t_{BSTUV}	Bootstrap undervoltage deglitch time		6	10	22	µs

6.6 Typical Characteristics
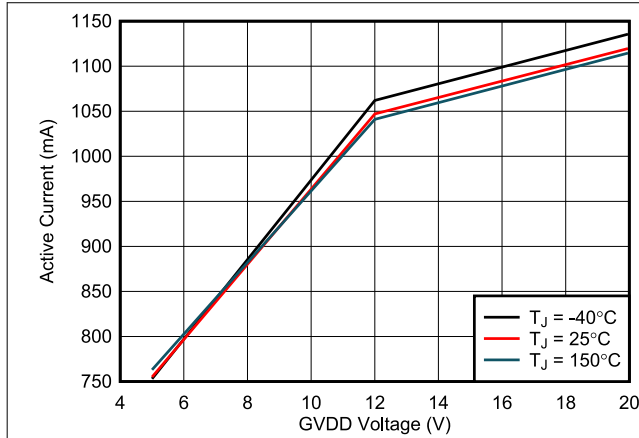
図 **6-1. Supply Current Over GVDD Voltage**
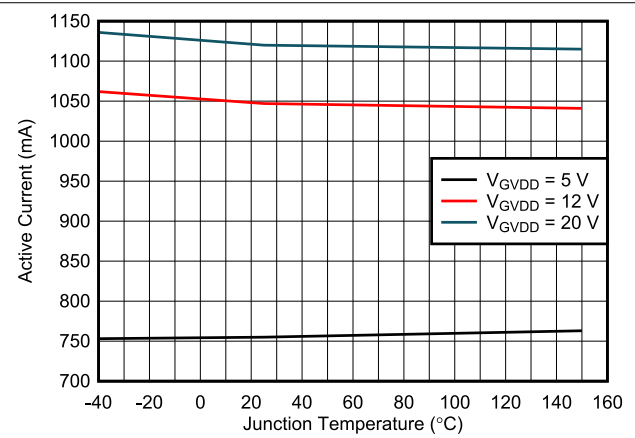
図 **6-2. Supply Current Over Temperature**

図 **6-3. Bootstrap Resistance Over GVDD Voltage**
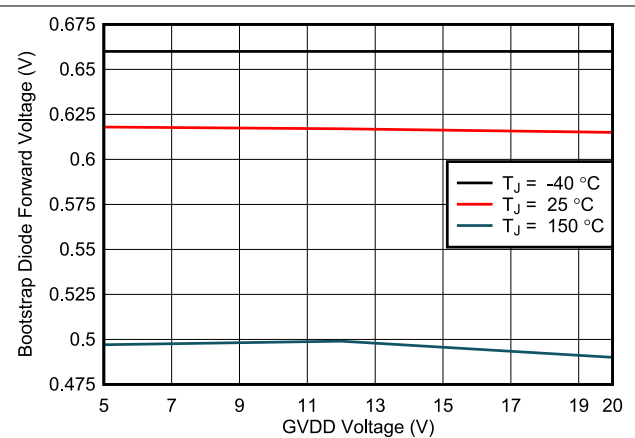
図 **6-4. Bootstrap Diode Forward Voltage over GVDD Voltage**

Product Folder Links: *DRV8770*

7 Detailed Description

7.1 Overview

The DRV8770 device is a gate driver for brushed DC motor drive applications. This device decreases system component count, reduces PCB area, and saves cost by integrating two independent half-bridge gate drivers and bootstrap diodes.

DRV8770 device integrates bootstrap diode used along with boot capacitor to generate voltage to drive high side N-channel MOSFET. The high-side and low-side gate drivers and can drive 750-mA source, 1.5-A sink currents with total 30-mA average output current. DRV8770 is available in 0.5-mm pitch QFN and 0.65 TSSOP surface-mount packages. The QFN size is 4 × 4 mm (0.5-mm pin pitch) for the 24-pin package, and TSSOP size is 6.5 × 6.4 mm (0.65-mm pin pitch) for the 20-pin package.

7.2 Functional Block Diagram
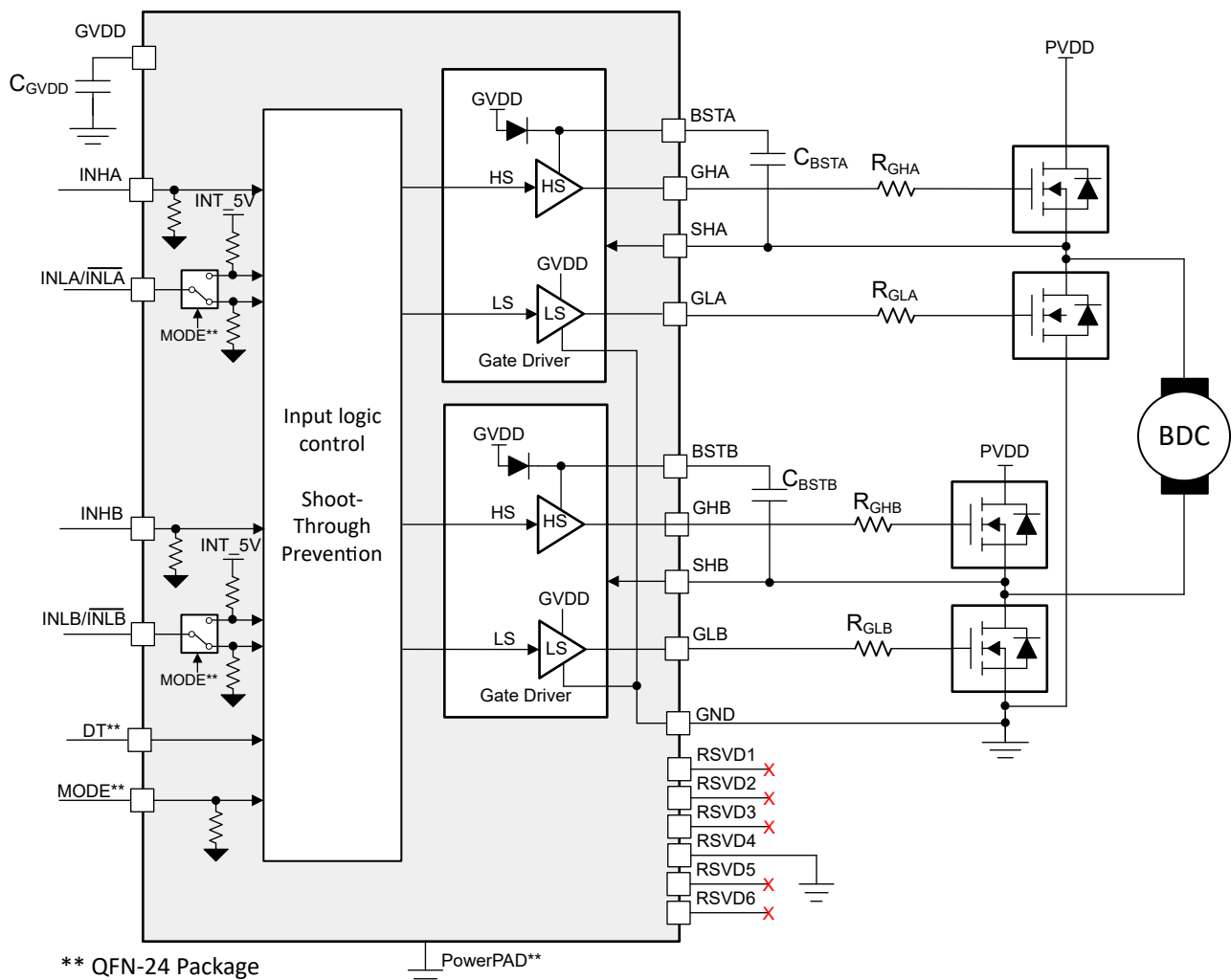
図 **7-1. Block Diagram for DRV8770**

7.3 Feature Description

7.3.1 Gate Drivers

The DRV8770 integrates two half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. Input on GVDD provides the gate bias voltage for the low-side MOSFETs. The high voltage is generated using a bootstrap capacitor and GVDD supply. DRV8770 device integrates the bootstrap diode. The

half-bridge gate drivers can be used in combination to drive a brushed DC motor or separately to drive other types of loads.

7.3.1.1 Gate Drive Timings

7.3.1.1.1 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the input deglitcher delay and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. The analog gate drivers have a small delay that contributes to the overall propagation delay of the device.
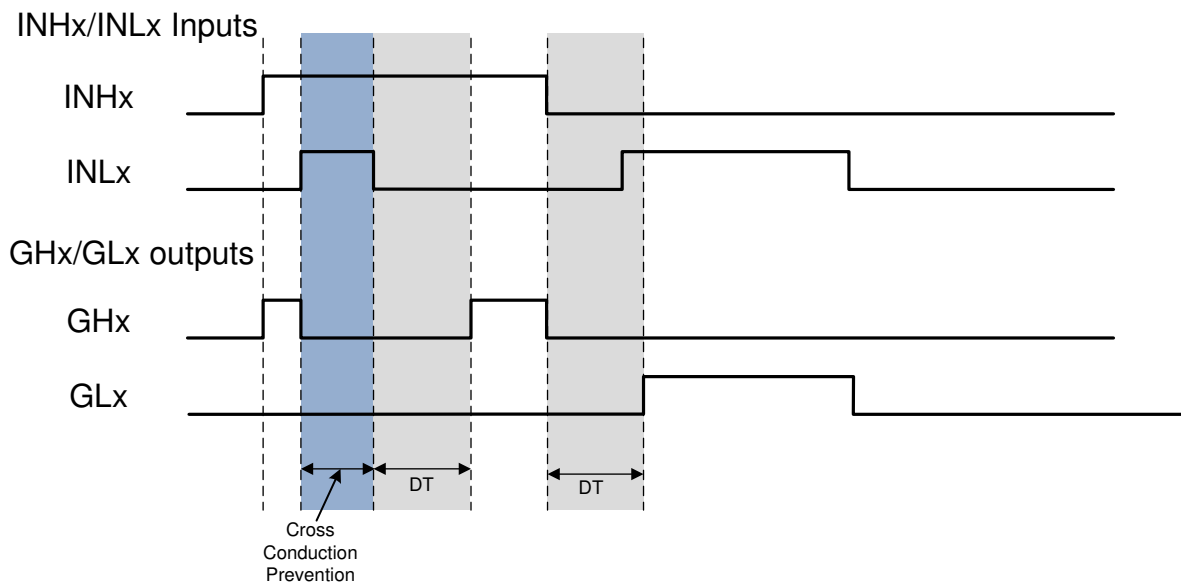
7.3.1.1.2 Deadtime and Cross-Conduction Prevention

In the DRV8770, high- and low-side inputs operate independently, with an exception to prevent cross conduction when high and low side are turned ON at same time. The DRV8770 turns OFF high- and low- side output to prevent shoot through when high- and low-side inputs are logic high at same time.

The DRV8770 also provides deadtime insertion to prevents both external MOSFETs of each power-stage from switching on at the same time. In devices with DT pin (QFN package device), deadtime can be linearly adjusted between 200 ns to 2000 ns by connecting resistor between DT and ground. When DT pin is connected to ground, fixed deadtime of 200 ns (typical value) is inserted. The value of resistor can be caculated using 式 1.

$$R_{DT}(k\Omega) = \frac{Deadtime\ (ns)}{5}$$

(1)

In device without DT pin (TSSOP package device), fixed deadtime of 200 ns (Typical value) is inserted to prevent high and low side gate output turning on at same time.

図 7-2. Cross Conduction Prevention and Deadtime Insertion

7.3.1.2 Mode (Inverting and non-inverting INLx)

The DRV8770 has flexibility of accepting different kind of inputs on INLx. In the QFN (RGE) package variant, the MODE pin provides option of GLx output inverted or non-inverted compared to polarity of signal on INLx pin. When the MODE pin is left floating, INLx is configured to be in non-inverting mode and GLx output is in phase

Product Folder Links: *DRV8770*

with INLx (see 図 7-3). When MODE pin is connected to GVDD, GLx output is out of phase with inputs (see 図 7-4). The TSSOP (PW) package variant does not have a MODE pin, so the INLx pins are inverted by default.
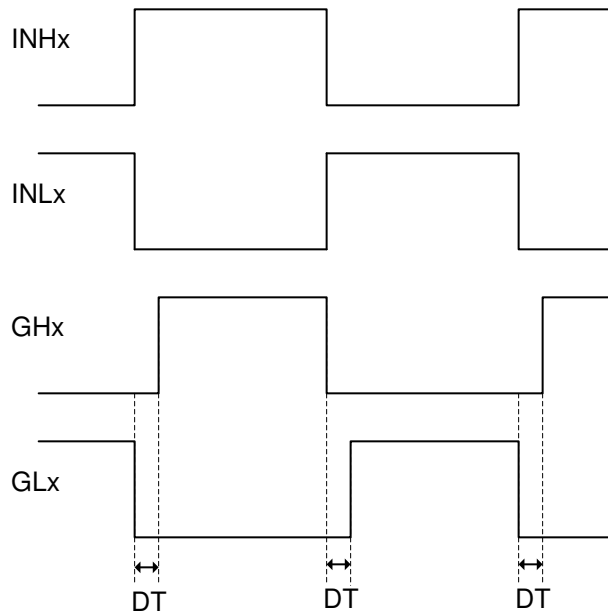

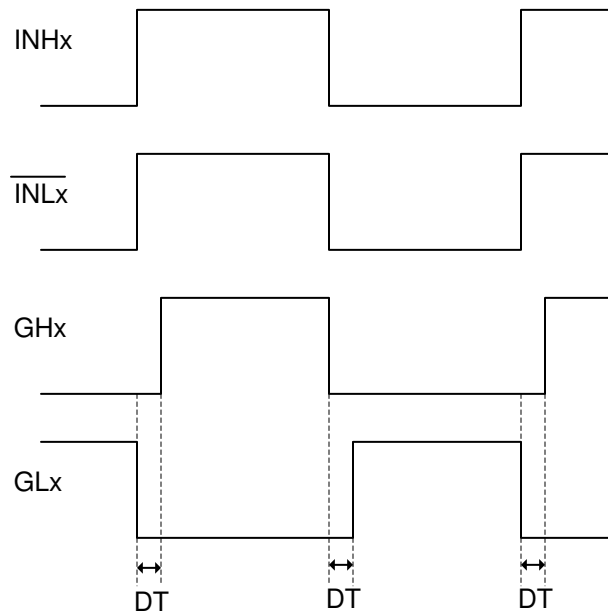**図 7-3. Non-Inverted INLx inputs (MODE = floating)**

図 7-4. Inverted INLx inputs (MODE = GVDD or TSSOP package variant)

表 7-1 shows the states of the gate drivers and FET half bridge when MODE = floating.

表 7-1. Logic table when MODE = floating

INHx	INLx	GHx	GLx	Half Bridge State
0	0	L	L	Z, FETs disabled
0	1	L	H	L, low-side FET enabled
1	0	H	L	H, high-side FET enabled
1	1	L	L	Z, invalid state

Product Folder Links: *DRV8770*

表 7-2 shows the states of the gate drivers and FET half bridge for the inverted mode (MODE = GVDD or the default mode of the TSSOP package). In this mode, the INHx and INLx pins can be tied together to reduce the number of control signals from a microcontroller, as shown in 表 7-3. In this configuration, the device controls the deadtime as described in セクション 7.3.1.1.2.

**表 7-2. Logic table when MODE = GVDD or TSSOP package variant**

INHx	INLx	GHx	GLx	Half Bridge State
0	0	L	H	L, low-side FET enabled
0	1	L	L	Z, FETs disabled
1	0	L	L	Z, invalid state
1	1	H	L	H, high-side FET enabled

表 7-3. Logic table when INHx = INLx for MODE = GVDD or TSSOP package variant

INHx = INLx	GHx	GLx	Half Bridge State
0	L	H	L, low-side FET enabled
1	H	L	H, high-side FET enabled

7.3.2 Pin Diagrams

図 7-5 shows the input structure for the logic level pins INHx, INLx. INHx and INLx has passive pull down, so when inputs are floating the output of gate driver will be pulled low. 図 7-6 shows the input structure for the logic level pin inverted INLx. INLx in inverted mode has passive pull up, so when inputs are floating the output of gate driver will be pulled low.

図 7-5. INHx and Non-Inverted INLx Logic-Level Input Pin Structure

図 7-6. Inverted INLx Logic-Level Input Pin Structure
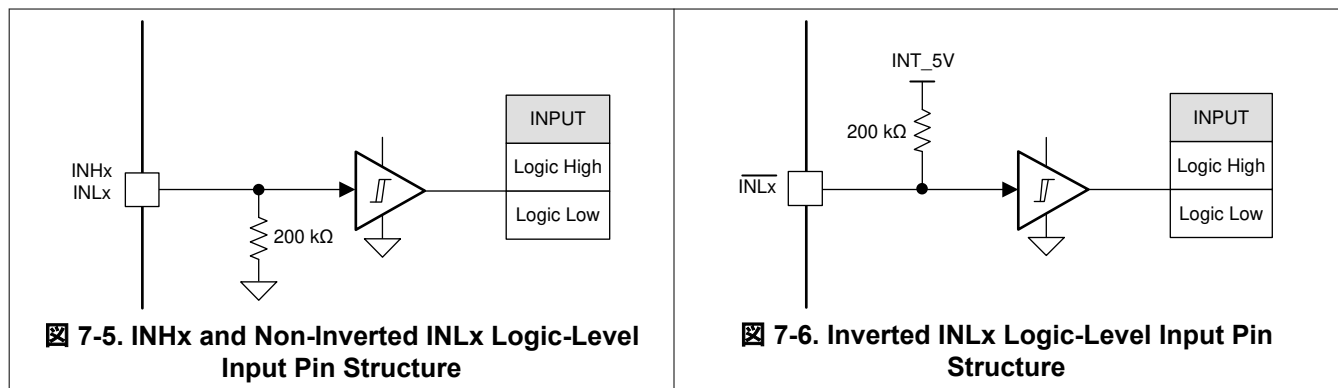
7.3.3 Gate Driver Protective Circuits

The DRV8770 is protected against BSTx undervoltage and GVDD undervoltage events.

表 7-4. Fault Action and Response

FAULT	CONDITION	GATE DRIVER	RECOVERY
V_{BSTx} undervoltage (BSTUV)	$V_{BSTx} < V_{BSTUV}$	GHx - Hi-Z	Automatic: $V_{BSTx} > V_{BSTUV}$ and low to high PWM edge detected on INHx pin
GVDD undervoltage (GVDDUV)	$V_{GVDD} < V_{GVDDUV}$	Hi-Z	Automatic: $V_{GVDD} > V_{GVDDUV}$

7.3.3.1 V_{BSTx} Undervoltage Lockout (BSTUV)

The DRV8770 has separate voltage comparator to detect undervoltage condition for each phase. If at any time the supply voltage on the BSTx pin falls lower than the VBSTUV threshold, high side external MOSFETs of that particular phase is disabled by disabling (Hi-Z) GHx pin. Normal operation starts again when the BSTUV condition clears and low to high PWM edge is detected on INHx input on the same phase BSTUV was detected. BSTUV protection ensures that high side gate driver are not switched when BSTx pin has lower value.

Product Folder Links: *DRV8770*

7.3.3.2 GVDD Undervoltage Lockout (GVDDUV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDDUV} threshold voltage, all of the external MOSFETs are disabled. Normal operation starts again GVDDUV condition clears. GVDDUV protection ensures that gate driver are not switched when GVDD input is at lower value.

7.4 Device Functional Modes

Whenever the GVDD > V_{GVDDUV} and V_{BSTX} > V_{BSTUV} the device is in operating (active) mode, in this condition gate driver output GHx and GLX will follow respective inputs INHx and INLx.

Product Folder Links: *DRV8770*

8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8770 is primarily used for brushed DC motor control. The design procedures in the *セクション 8.2* section highlight how to use and configure the DRV8770.

8.2 Typical Application
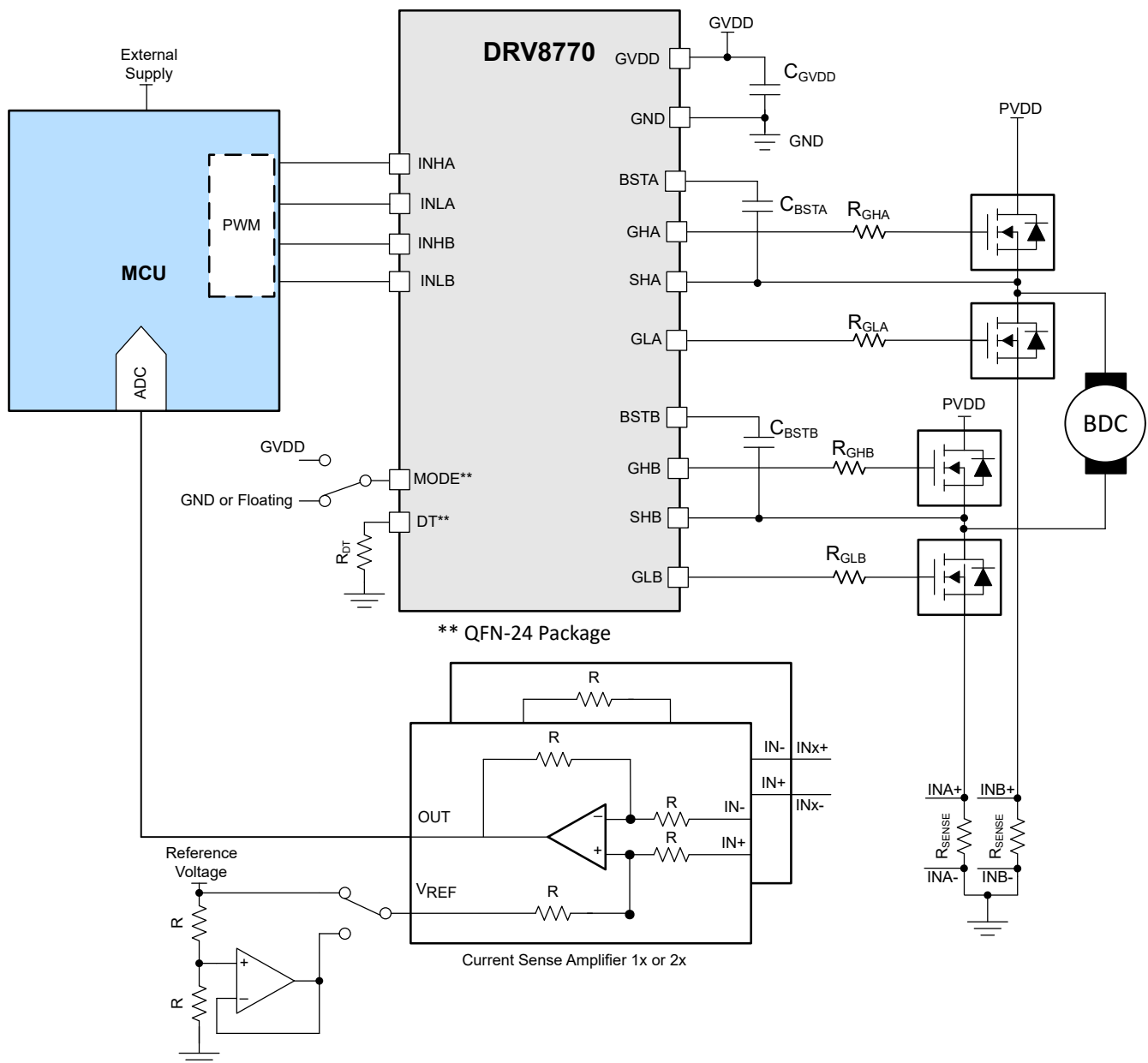
図 8-1. Application Schematic

Product Folder Links: *DRV8770*

8.2.1 Design Requirements

表 8-1 lists the example design input parameters for system design.

表 8-1. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
MOSFET	-	CSD19532Q5B
Gate Supply Voltage	V_{GVDD}	12 V
Gate Charge	Q_G	48 nC

8.2.2 Detailed Design Procedure

Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. 式 2 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \tag{2}$$

= 12 V – 0.85 V – 4.5 V = 6.65 V

where
- V_{GVDD} is the supply voltage of the gate drive
- V_{BOOTD} is the forward voltage drop of the bootstrap diode
- V_{BSTUV} is the threshold of the bootstrap undervoltage lockout

In this example the allowed voltage drop across bootstrap capacitor is 6.65 V. It is generally recommended that ripple voltage on both the bootstrap capacitor and GVDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value between 0.5 V to 1 V.

The total charge needed per switching cycle can be estimated with 式 3:

$$Q_{TOT} = Q_G + \frac{IL_{BS\_TRANS}}{f_{SW}} \tag{3}$$

= 48 nC + 220 µA/20 kHz = 50 nC + 11 nC = 59 nC

where
- Q_G is the total MOSFET gate charge
- I_{LBS_TRAN} is the bootstrap pin leakage current
- f_{SW} is the is the PWM frequency

The minimum bootstrap capacitor an then be estimated as below assuming 1-V ΔV_{BSTx}:

$$C_{BST\_MIN} = {Q_{TOT}}/{\Delta V_{BSTX}} \tag{4}$$

= 59 nC / 1 V = 59 nF

The calculated value of minimum bootstrap capacitor is 59 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100 nF bootstrap capacitor in this example. It is also recommended to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

Note

If the bootstrap capacitor value (C_{BSTx}) is above 1 μF, then current flowing through internal bootstrap diode needs to be limited.

The local GVDD bypass capacitor must be greater than the value of bootstrap capacitor value (generally 10 times the bootstrap capacitor value).

$$C_{GVDD} \geq 10 \times C_{BSTX}$$

(5)

= 10*100 nF = 1 μF

For this example application, choose 1-μF C_{GVDD} capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system.

Gate Resistance Selection

The slew rate of the SHx connection will be dependent on the rate at which the gate of the external MOSFETs is controlled. The pull-up/pull-down strength of the DRV8770 is fixed internally, hence slew rate of gate voltage can be controlled with an external series gate resistor. In some applications the gate charge, which is load on gate driver device, is significantly larger than gate driver peak output current capability. In such applications external gate resistors can limit the peak output current of the gate driver. External gate resistors are also used to damp ringing and noise.

The specific parameters of the MOSFET, system voltage, and board parasitics will all affect the final slew rate, so generally selecting an optimal value or configuration of external gate resistor is an iterative process.

8.2.3 Application Curves

図 8-2. Gate voltages, SHx rising with 15 ohm gate resistor and CSD19532Q5B MOSFET

図 8-3. Gate voltages, SHx falling with 15 ohm gate resistor and CSD19532Q5B MOSFET
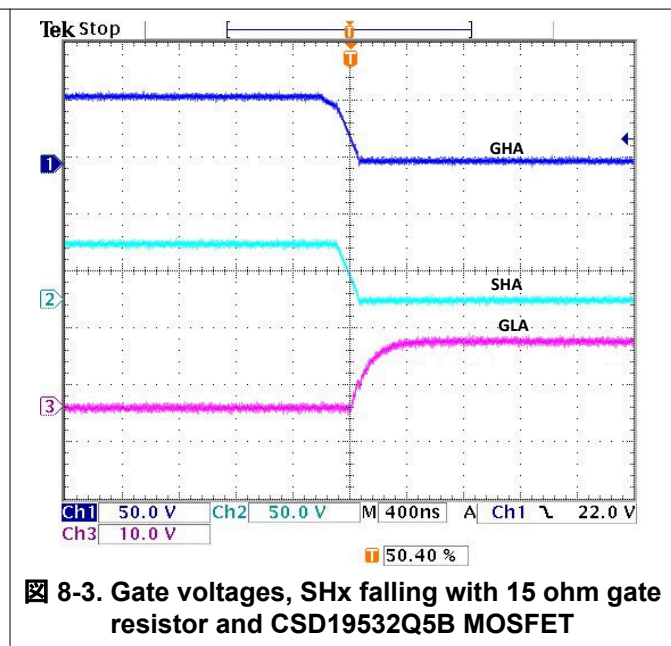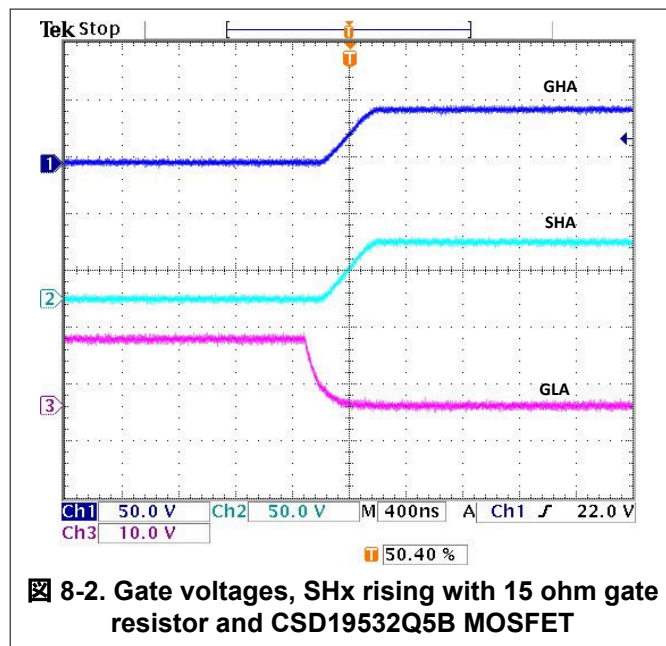
9 Power Supply Recommendations

The DRV8770 is designed to operate from an input voltage supply (GVDD) range from 4.8 V to 20 V. A local bypass capacitor should be placed between the GVDD and GND pins. This capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is recommended to use two capacitors across GVDD and GND: a low capacitance ceramic surface-mount capacitor for high frequency filtering placed very close to GVDD and GND pin, and another high capacitance value surfacemount capacitor for device bias requirements. In a similar manner, the current pulses delivered by the GHx pins are sourced from the BSTx pins. Therefore, capacitor across the BSTx to SHx is recommended, it should be high enough capacitance value capacitor to deliver GHx pulses.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.
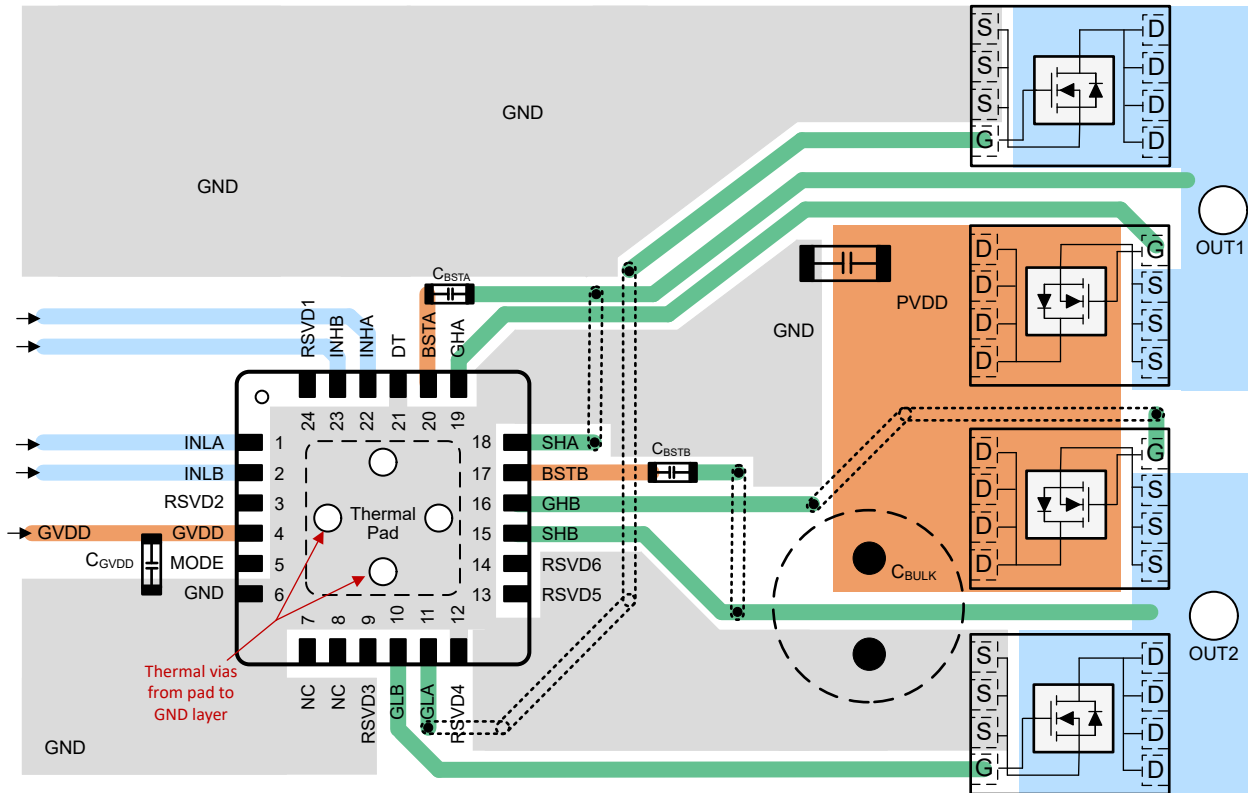
The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.
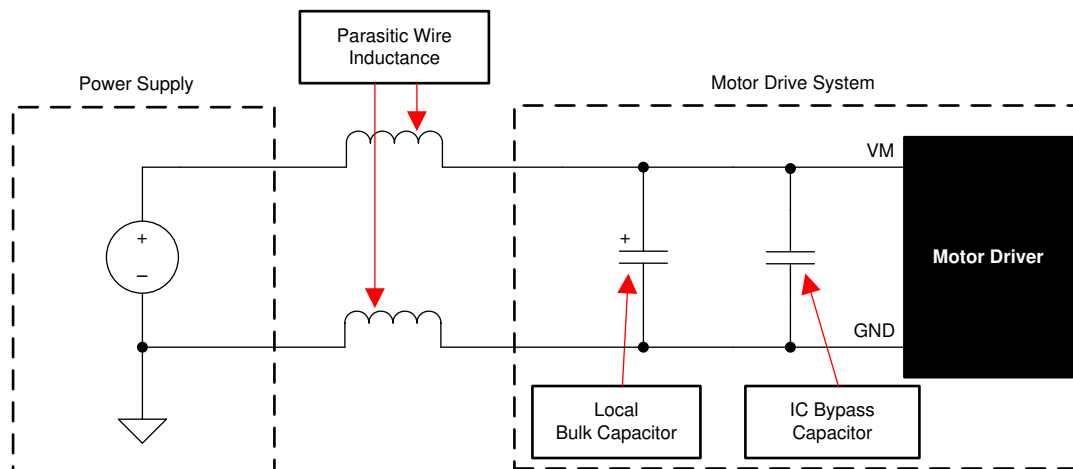
図 9-1. Motor Drive Supply Parasitics Example

10 Layout

10.1 Layout Example

10.2 Layout Guidelines

- Low ESR/ESL capacitors must be connected close to the device between GVDD and GND and between BSTx and SHx pins to support high peak currents drawn from GVDD and BSTx pins during the turn-on of the external MOSFETs.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground.
- In order to avoid large negative transients on the switch node (SHx) pin, the parasitic inductances between the source of the high-side MOSFET and the source of the low-side MOSFET must be minimized.
- In order to avoid unexpected transients, the parasitic inductance of the GHx, SHx, and GLx connections must be minimized. Minimize the trace length and number of vias wherever possible. Minimum 10 mil and typical 15 mil trace width is recommended.
- Resistance between DT and GND must be place as close as possible to device
- Place the gate driver as close to the MOSFETs as possible. Confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area by reducing trace length. This confinement decreases the loop inductance and minimize noise issues on the gate terminals of the MOSFETs.
- In QFN package device variants, NC pins can be connected to GND to increase ground conenction between thermal pad and external ground plane.
- Refer to sections *General Routing Techniques and MOSFET Placement and Power Stage Routing* in Application Report

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8770RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8770	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8770RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8770RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

Images above are just a representation of the package family, actual package may vary.
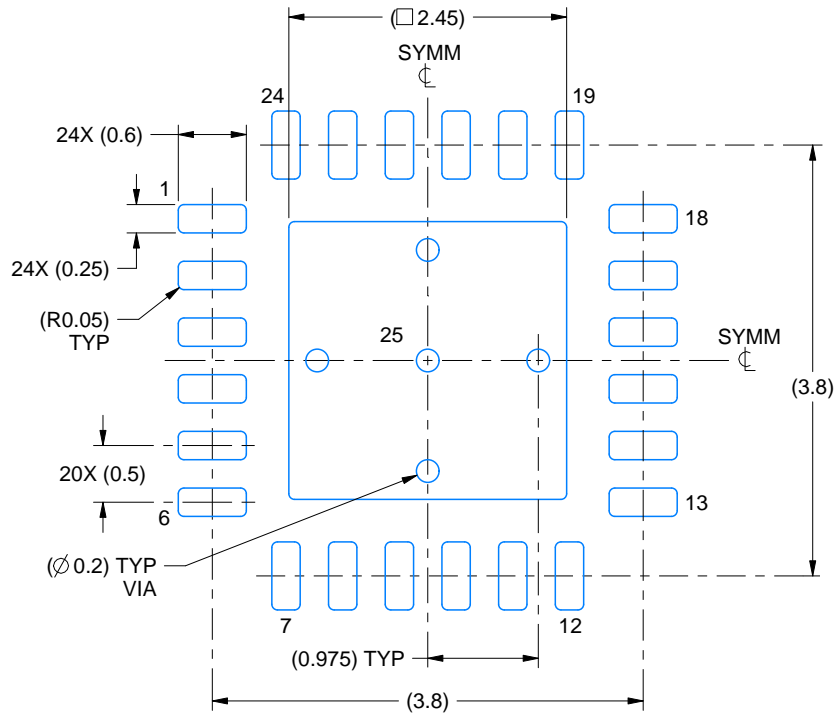Refer to the product data sheet for package details.

4204104/H

TEXAS
INSTRUMENTS

A

4.1
3.9

B

PIN 1 INDEX AREA

4.1
3.9

0.5
0.3

0.3
0.2

DETAIL
OPTIONAL TERMINAL
TYPICAL

1 MAX

0.05
0.00

C

SEATING PLANE

⌒ | 0.08 | C

2X | 2.5

☐ 2.45 ± 0.1

7

12

SEE TERMINAL
DETAIL

6

EXPOSED
THERMAL PAD

13

2X
2.5

25

SYMM
₵

18

1

20X | 0.5

24

19

SYMM
₵

PIN 1 ID
(OPTIONAL)

24X 0.5
0.3

24X 0.3
0.2

⊕ | 0.1 Ⓜ | C | A | B
0.05 Ⓜ

(0.2) TYP
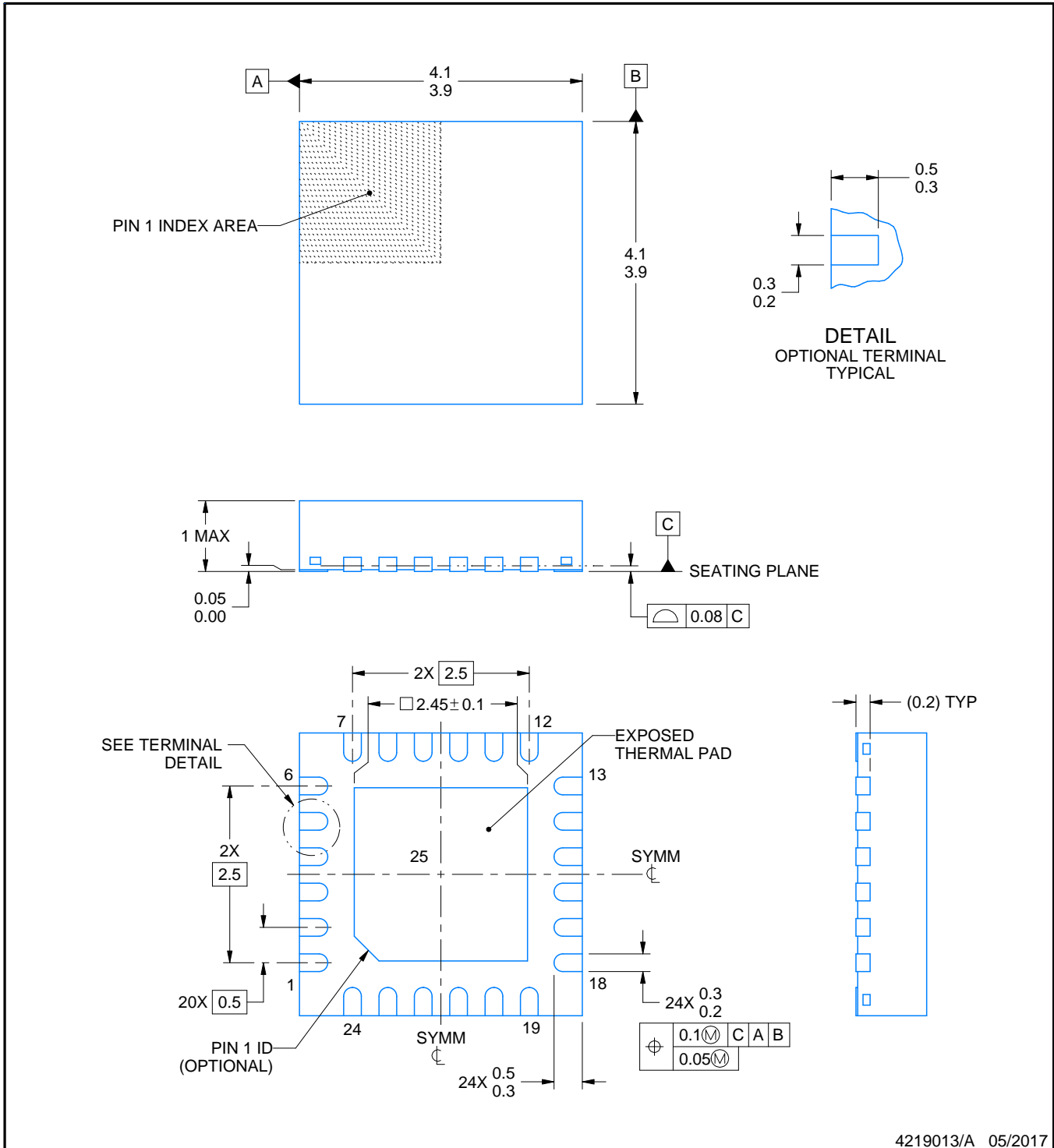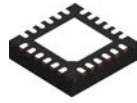
4219013/A   05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

RGE0024B

(□ 2.45)

SYMM
℄

24

19

24X (0.6)

1

24X (0.25)

(R0.05)
TYP

18

25

SYMM
℄

(3.8)

20X (0.5)

6

(∅ 0.2) TYP
VIA

13

7

12

(0.975) TYP

(3.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

0.07 MAX
ALL AROUND

METAL

EXPOSED
METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED
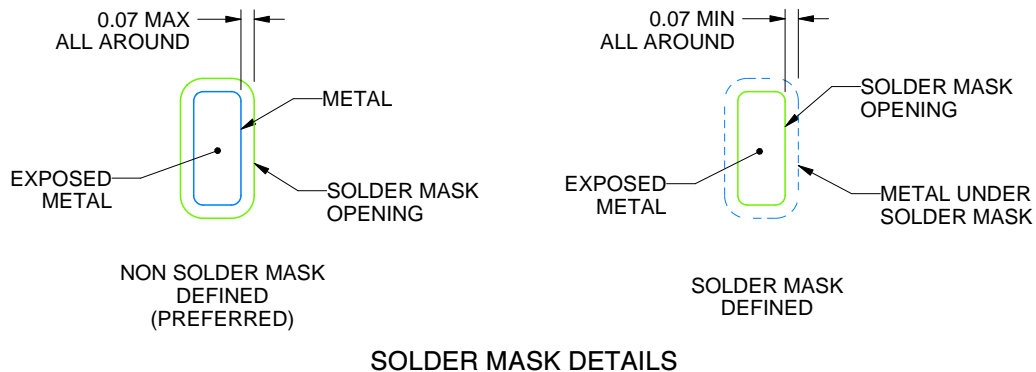
SOLDER MASK DETAILS

4219013/A   05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.

4X (□ 1.08)
(0.64) TYP
24
19
24X (0.6)
1
25
24X (0.25)
(R0.05) TYP
18
SYMM
(0.64)
TYP
(3.8)
20X (0.5)
6
13
METAL
TYP
7
12
SYMM
(3.8)
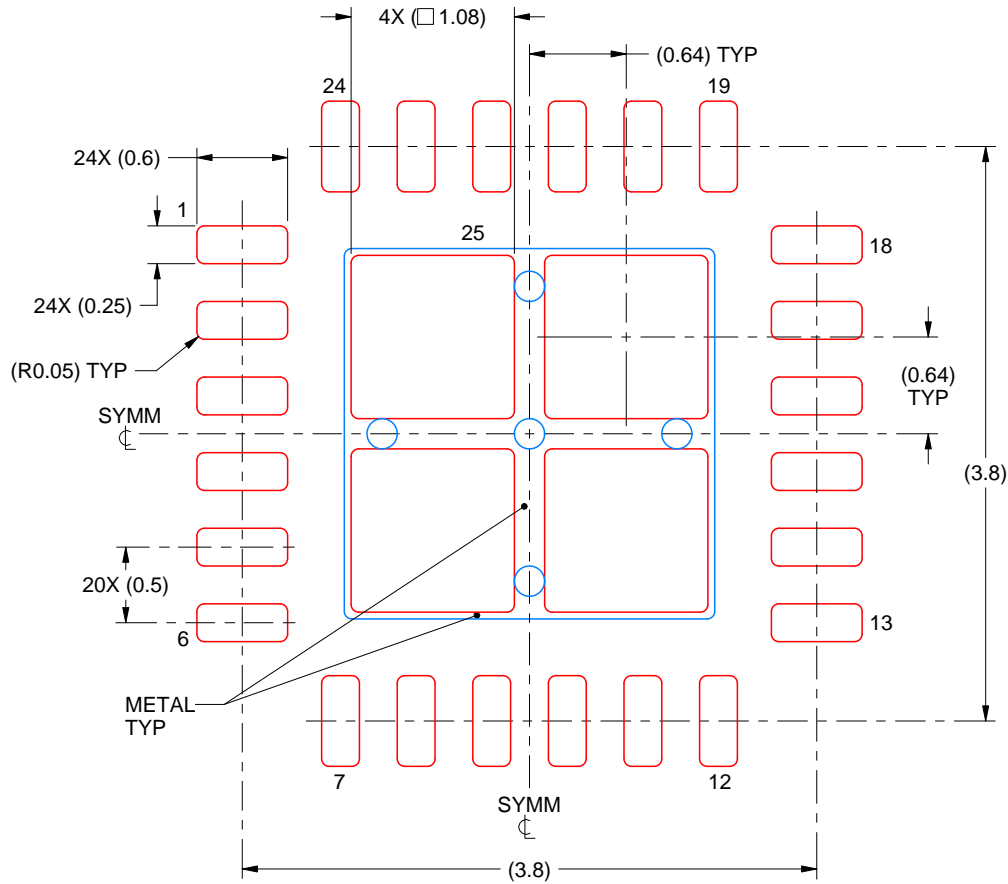
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A   05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.