

DRV5023 デジタル・スイッチ・ホール効果センサ

1 特長

- デジタル・ユニポーラスイッチ・ホール・センサ
- 優れた温度安定性
 - 温度範囲の全体で感度 $\pm 10\%$
- 複数の感度オプション(B_{OP} / B_{RP})
 - 3.5 / 2mT (FA, [図 24](#)を参照)
 - 6.9 / 3.2mT (AJ, [図 24](#)を参照)
 - 14.5 / 6mT (BI, [図 24](#)を参照)
- 広い範囲の電圧をサポート
 - 2.5~38V
 - 外部レギュレータ不要
- 広い範囲の温度で動作
 - $T_A = -40 \sim 125^\circ\text{C}$ (Q, [図 24](#)を参照)
- オープン・ドレイン出力(30mAシンク)
- 高速な電源オン時間: 35 μs
- 小さなパッケージと占有面積
 - 表面実装の3ピンSOT-23 (DBZ)
 - 2.92mm \times 2.37mm
 - スルーホールの3ピンTO-92 (LPG)
 - 4.00mm \times 3.15mm
- 保護機能
 - 逆電圧保護(最大-22V)
 - 40Vまでの負荷ダンピングをサポート
 - 出力短絡保護
 - 出力電流制限

2 アプリケーション

- ドッキング検出
- ドアの開閉検出
- 近接センシング
- バルブの位置決め
- パルスのカウント

3 概要

DRV5023 デバイスはチョップ安定化されたホール効果センサで、温度範囲全体にわたって優れた感度の安定性を持つ磁気センシング・ソリューションを提供し、保護機能が内蔵されています。

周囲の磁束密度が B_{OP} スレッショルドを超えると、DRV5023のオープン・ドレイン出力がLOWに変化します。磁場が B_{RP} 未満に低下するまで出力はLOWに維持され、その後で出力がハイ・インピーダンスになります。出力電流のシンク能力は30mAです。2.5~38Vまでの広い範囲の電圧で動作し、-22Vまでの逆電圧から保護されるため、広範な産業用アプリケーションに適したデバイスです。

逆電圧の状態、負荷ダンピング、および出力短絡や過電流に対して、内部的な保護機能が搭載されています。

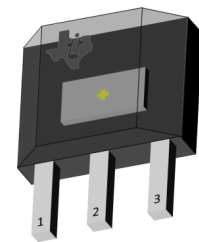
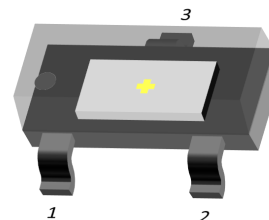
製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
DRV5023	SOT-23 (3)	2.92mm \times 1.30mm
	TO-92 (3)	4.00mm \times 3.15mm

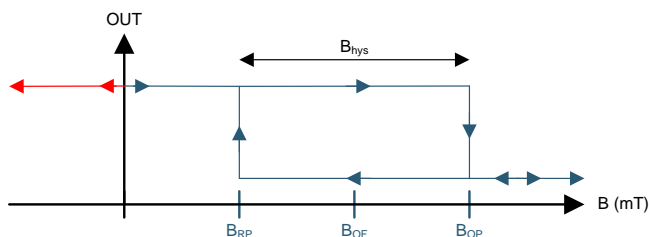
(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

SOT-23

TO-92



出力状態



目次

1	特長	1	7.3	Feature Description	10
2	アプリケーション	1	7.4	Device Functional Modes	15
3	概要	1	8	Application and Implementation	16
4	改訂履歴	2	8.1	Application Information	16
5	Pin Configuration and Functions	4	8.2	Typical Applications	16
6	Specifications	5	9	Power Supply Recommendations	18
6.1	Absolute Maximum Ratings	5	10	Layout	19
6.2	ESD Ratings	5	10.1	Layout Guidelines	19
6.3	Recommended Operating Conditions	5	10.2	Layout Example	19
6.4	Thermal Information	5	11	デバイスおよびドキュメントのサポート	20
6.5	Electrical Characteristics	6	11.1	デバイス・サポート	20
6.6	Switching Characteristics	6	11.2	ドキュメントの更新通知を受け取る方法	21
6.7	Magnetic Characteristics	6	11.3	コミュニティ・リソース	21
6.8	Typical Characteristics	7	11.4	商標	21
7	Detailed Description	9	11.5	静電気放電に関する注意事項	21
7.1	Overview	9	11.6	Glossary	21
7.2	Functional Block Diagram	9	12	メカニカル、パッケージ、および注文情報	21

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (May 2016) から Revision G に変更	Page
• Changed the power-on time for the FA version in the <i>Electrical Characteristics</i> table	6
• Added the <i>Layout</i> section	19
• 追加「ドキュメントの更新通知を受け取る方法」セクション	21

Revision E (February 2016) から Revision F に変更	Page
• Revised preliminary limits for the FA version	6

Revision D (December 2015) から Revision E に変更	Page
• FAデバイス・オプション 追加	1
• Added the typical bandwidth value to the <i>Magnetic Characteristics</i> table	6

Revision C (May 2015) から Revision D に変更	Page
• SOT-23パッケージの本体サイズを訂正し、SIPパッケージ名をTO-92に訂正	1
• Added B_{MAX} to <i>Absolute Maximum Ratings</i>	5
• Removed table note from junction temperature	5
• パッケージのテープ&リールに関するMとブランクのオプションを更新	20
• コミュニティ・リソース を追加	21

Revision B (September 2014) から Revision C に変更	Page
• デバイスのステータスを量産データに更新	1

Revision A (August 2014) から Revision B に変更
Page

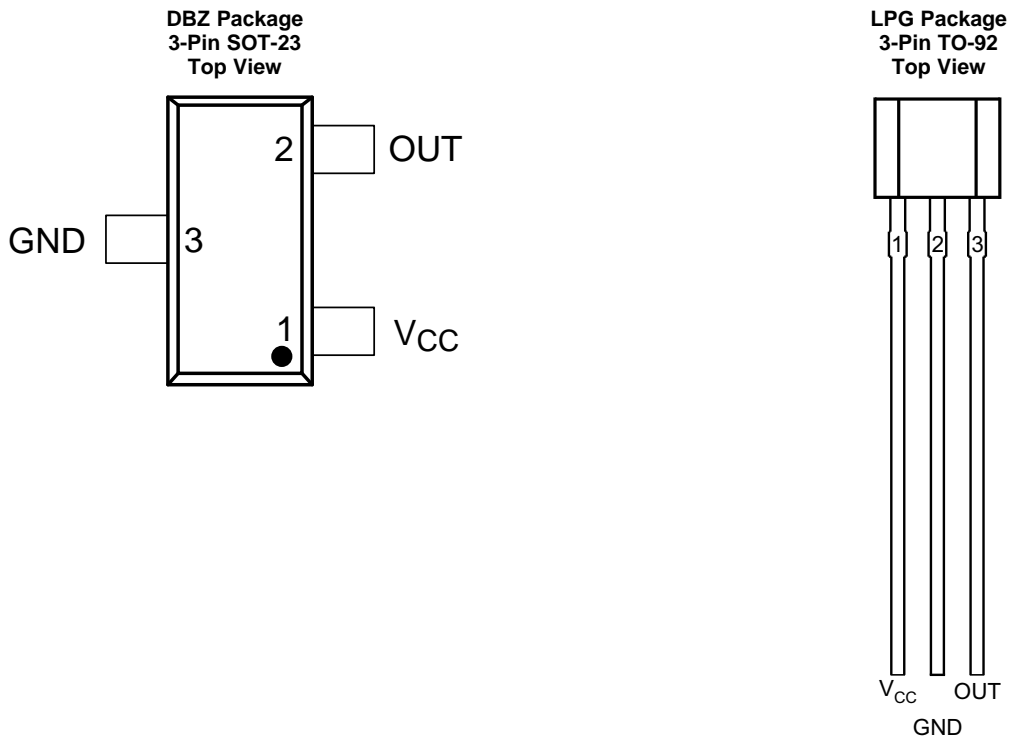
• 高感度オプションを+6.9 / +3.2mT (AJ)および+14.5 / +6mT (BI)へ更新	1
• Added typical rise and fall time and removed maximum value	6
• Updated the device values and typical values in Magnetic Characteristics	6
• Updated all <i>Typical Characteristics</i> graphs	7
• Updated Equation 4	17
• 図 24 を更新	20

2014年5月発行のものから更新
Page

• 高感度オプションを+6.9 / +2.3mT (AJ)から+6.9 / +3.3mT (AJ)へ 変更	1
• Changed the maximum T_J value from 175°C to 150°C	5
• Changed MIN value for I_{OCP} from 20 to 15	6
• Changed Max value for I_{OCP} from 40 to 45	6
• Updated <i>Magnetic Characteristics</i> table.	6

5 Pin Configuration and Functions

For additional configuration information, see [デバイスのマーキング](#) and [メカニカル、パッケージ、および注文情報](#).



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG		
GND	3	2	GND	Ground pin
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V _{CC}	1	1	Power	2.5 to 38 V power supply. Bypass this pin to the GND pin with a 0.01- μ F (minimum) ceramic capacitor rated for V _{CC} .

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Power supply voltage	V _{CC}	-22 ⁽²⁾	40	V
	Voltage ramp rate (V _{CC}), V _{CC} < 5 V	Unlimited		V/μs
	Voltage ramp rate (V _{CC}), V _{CC} > 5 V	0	2	
Output pin voltage		-0.5	40	V
Output pin reverse current during reverse supply condition		0	100	mA
Magnetic flux density, B _{MAX}		Unlimited		
Operating junction temperature, T _J		-40	150	°C
Storage temperature, T _{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Ensured by design. Only tested to -20 V.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Power supply voltage	2.5	38	V
V _O	Output pin voltage (OUT)	0	38	V
I _{SINK}	Output pin current sink (OUT) ⁽¹⁾	0	30	mA
T _A	Operating ambient temperature	-40	125	°C

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	DRV5023		UNIT	
	DBZ (SOT-23)	LPG (TO-92)		
	3 PINS	3 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	333.2	180	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	99.9	98.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	66.9	154.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	4.9	40	°C/W
ψ _{JB}	Junction-to-board characterization parameter	65.2	154.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V _{CC}	V _{CC} operating voltage		2.5		38	V
I _{CC}	Operating supply current	V _{CC} = 2.5 to 38 V, T _A = 25°C		2.7		mA
		V _{CC} = 2.5 to 38 V, T _A = 125°C		3	3.5	
t _{on}	Power-on time	AJ, BI versions		35	50	μs
		FA version		35	70	
OPEN DRAIN OUTPUT (OUT)						
r _{DS(on)}	FET on-resistance	V _{CC} = 3.3 V, I _O = 10 mA, T _A = 25°C		22		Ω
		V _{CC} = 3.3 V, I _O = 10 mA, T _A = 125°C		36	50	
I _{lkg(off)}	Off-state leakage current	Output Hi-Z			1	μA
PROTECTION CIRCUITS						
V _{CCR}	Reverse supply voltage		-22			V
I _{OCP}	Overcurrent protection level	OUT shorted V _{CC}	15	30	45	mA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t _d	Output delay time	B = B _{RP} – 10 mT to B _{OP} + 10 mT in 1 μs		13	25	μs
t _r	Output rise time (10% to 90%)	R1 = 1 kΩ, C _O = 50 pF, V _{CC} = 3.3 V		200		ns
t _f	Output fall time (90% to 10%)	R1 = 1 kΩ, C _O = 50 pF, V _{CC} = 3.3 V		31		ns

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

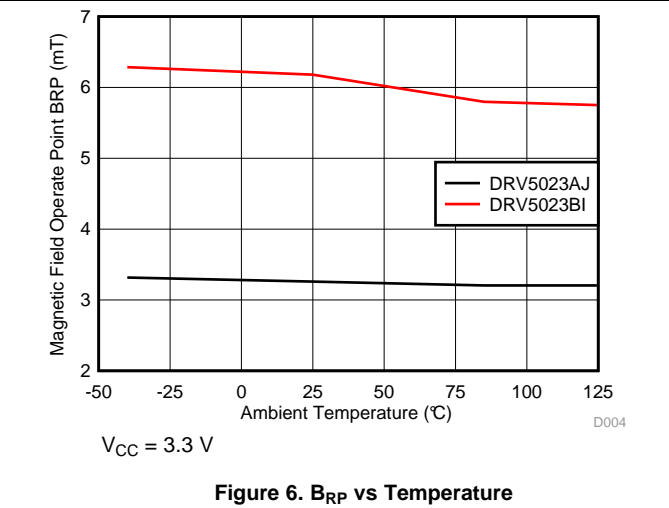
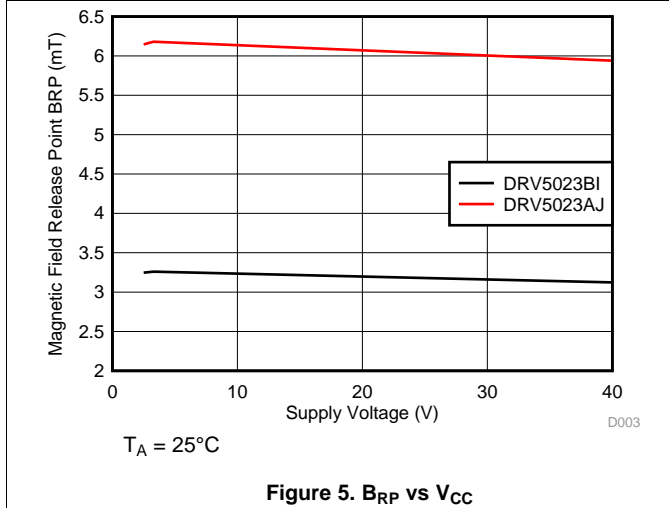
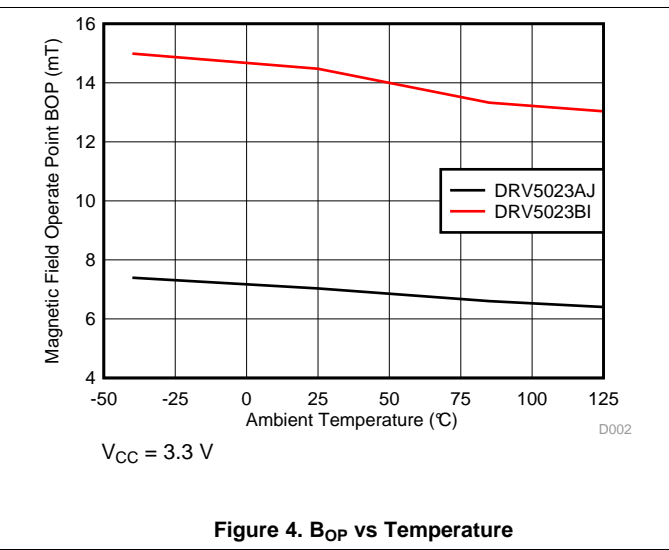
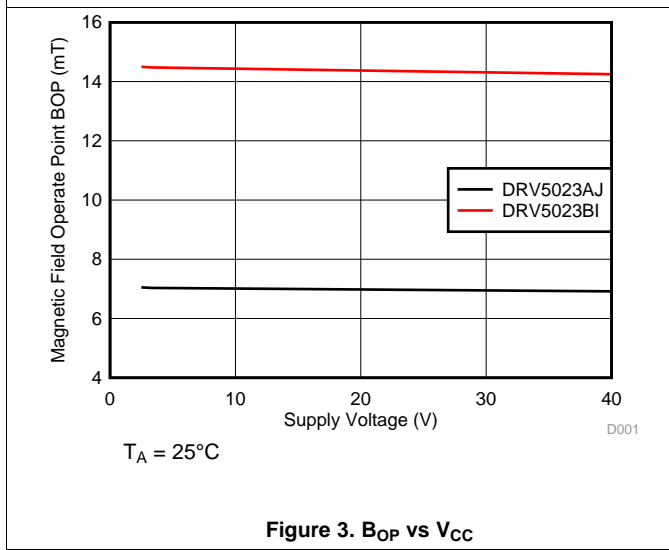
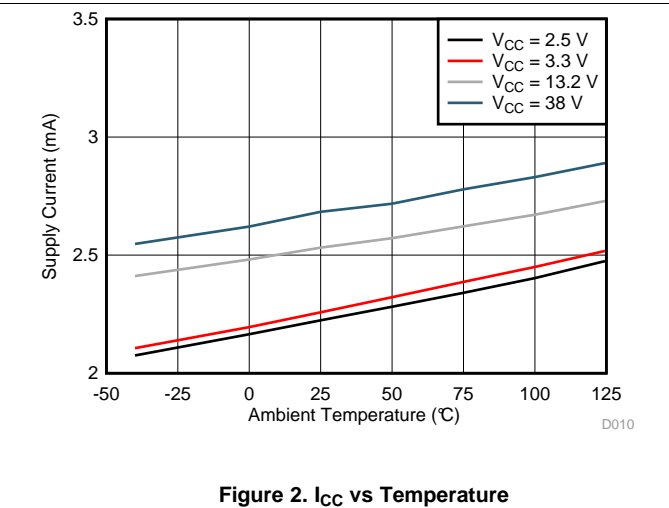
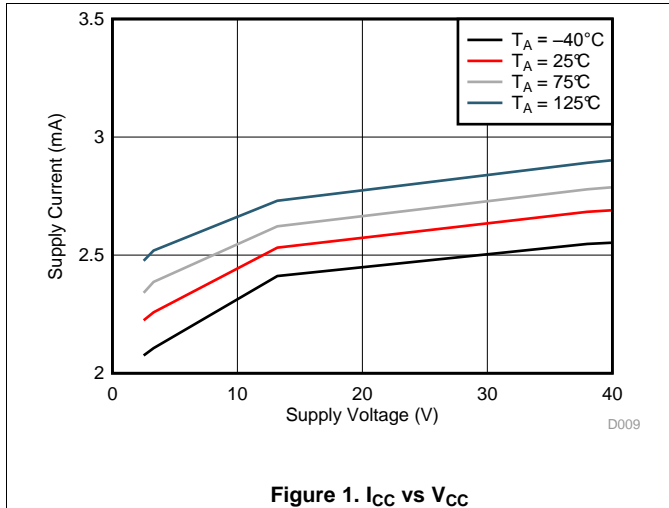
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT ⁽¹⁾
f _{BW}	Bandwidth ⁽²⁾		20	30		kHz
DRV5023FA: 3.5 / 2 mT						
B _{OP}	Operate point (see Figure 12)	T _A = -40°C to 125°C	1.8	3.5	6.8	mT
B _{RP}	Release point (see Figure 12)		0.5	2	4.2	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP})			1.5		mT
B _O	Magnetic offset, B _O = (B _{OP} + B _{RP}) / 2			2.8		mT
DRV5023AJ: 6.9 / 3.2 mT						
B _{OP}	Operate point (see Figure 12)	T _A = -40°C to 125°C	3	6.9	12	mT
B _{RP}	Release point (see Figure 12)		1	3.2	5	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP})			3.7		mT
B _O	Magnetic offset, B _O = (B _{OP} + B _{RP}) / 2			5		mT
DRV5023BI: 14.5 / 6 mT						
B _{OP}	Operate point (see Figure 12)	T _A = -40°C to 125°C	6	14.5	24	mT
B _{RP}	Release point (see Figure 12)		3	6	9	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP}) ⁽³⁾			8.5		mT
B _O	Magnetic offset, B _O = (B _{OP} + B _{RP}) / 2			10.3		mT

(1) 1 mT = 10 Gauss

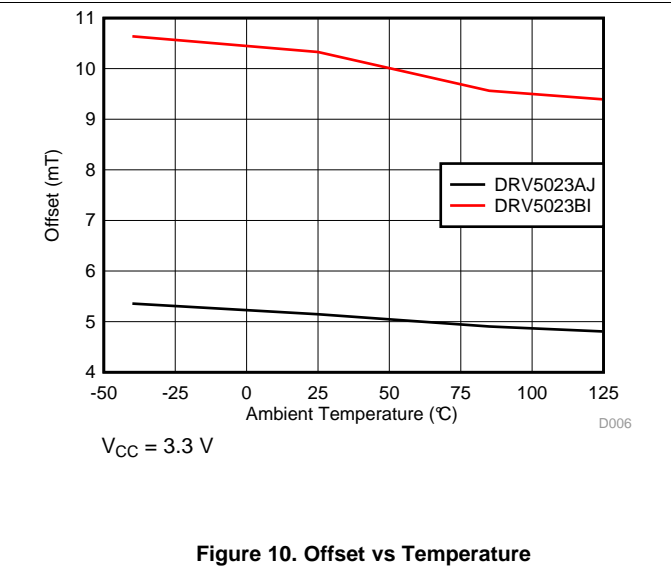
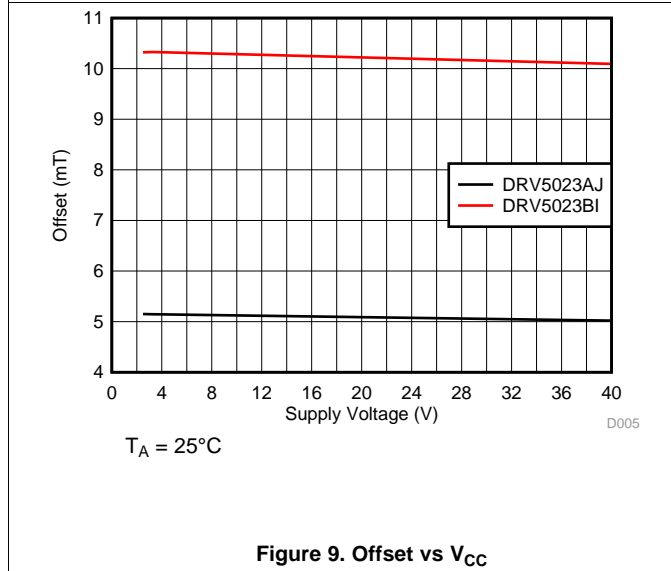
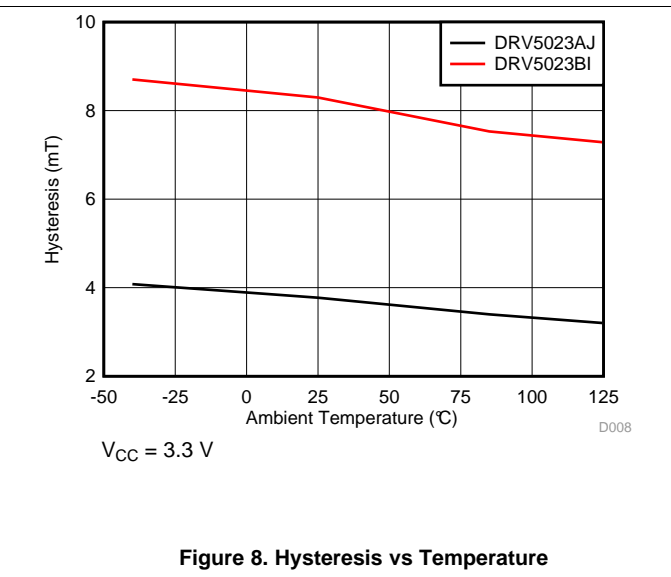
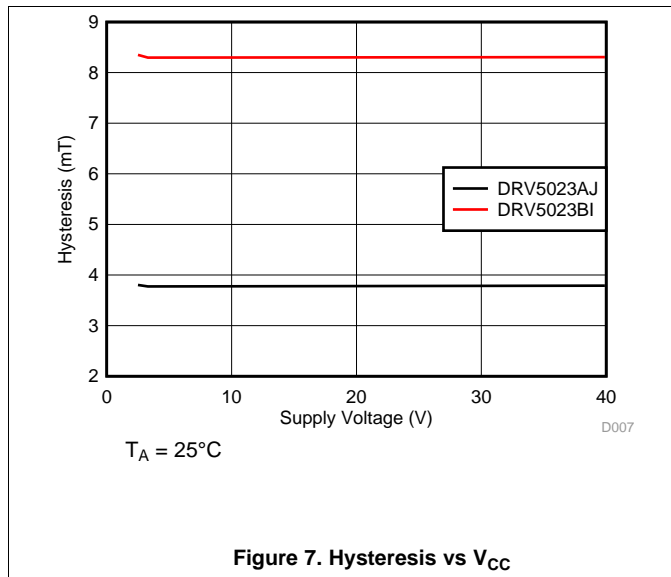
(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.

 (3) |B_{OP}| is always greater than |B_{RP}|.

6.8 Typical Characteristics



Typical Characteristics (continued)



7 Detailed Description

7.1 Overview

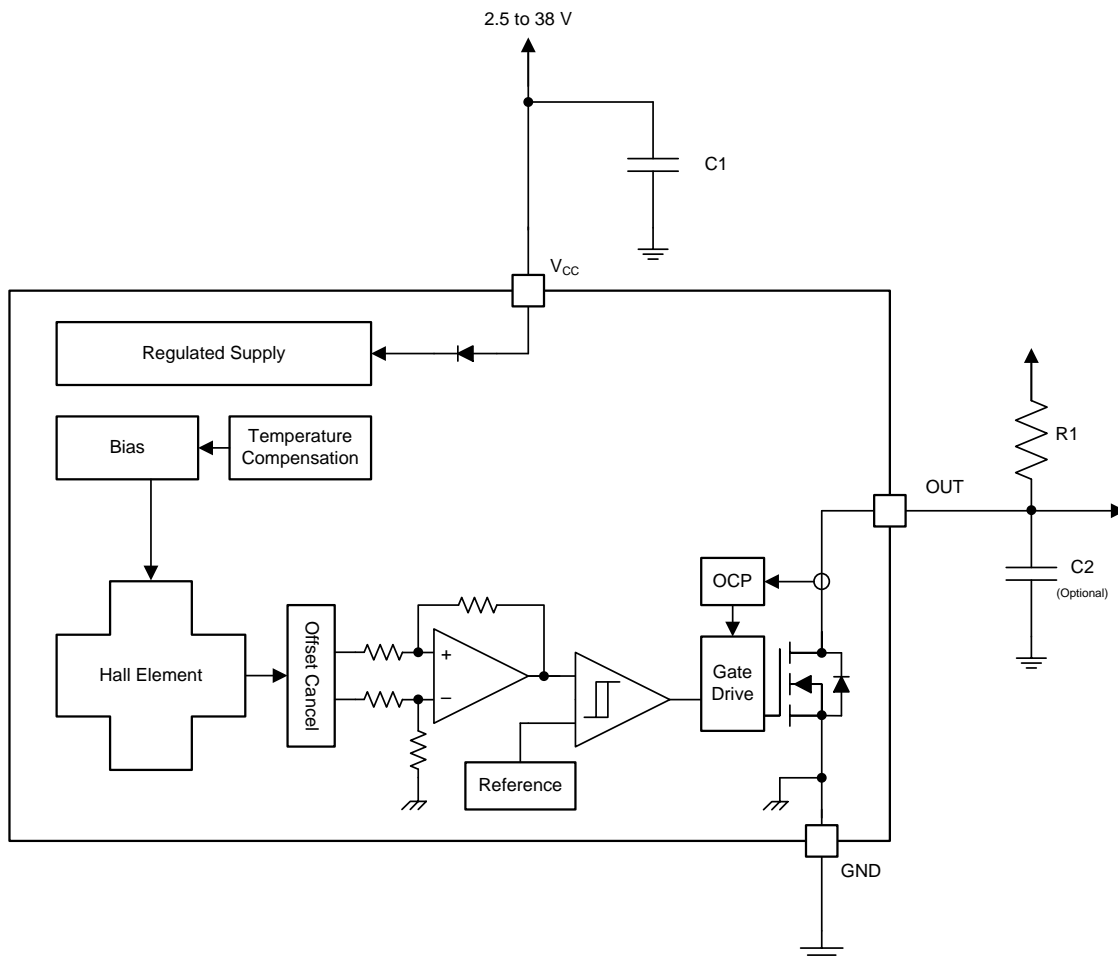
The DRV5023 device is a chopper-stabilized Hall sensor with a digital output for magnetic sensing applications. The DRV5023 device can be powered with a supply voltage between 2.5 and 38 V, and will survive -22 V reverse-battery conditions. The DRV5023 device does not operate when -22 to 2.4 V is applied to the V_{CC} pin (with respect to GND pin). In addition, the device can withstand supply voltages up to 40 V for transient durations.

The field polarity is defined as follows: a **south pole** near the marked side of the package is a positive magnetic field. A **north pole** near the marked side of the package is a negative magnetic field.

The output state is dependent on the magnetic field perpendicular to the package. A strong **south pole** near the marked side of the package causes the output to pull low (operate point, BOP), and a weak **south pole** causes the output to release (release point, BRP). Hysteresis is included in between the operate point and the release point therefore magnetic-field noise does not accidentally trip the output.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC} , or to a different voltage supply. This allows for easier interfacing with controller circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

A positive magnetic field is defined as a **south pole** near the marked side of the package as shown in [Figure 11](#).

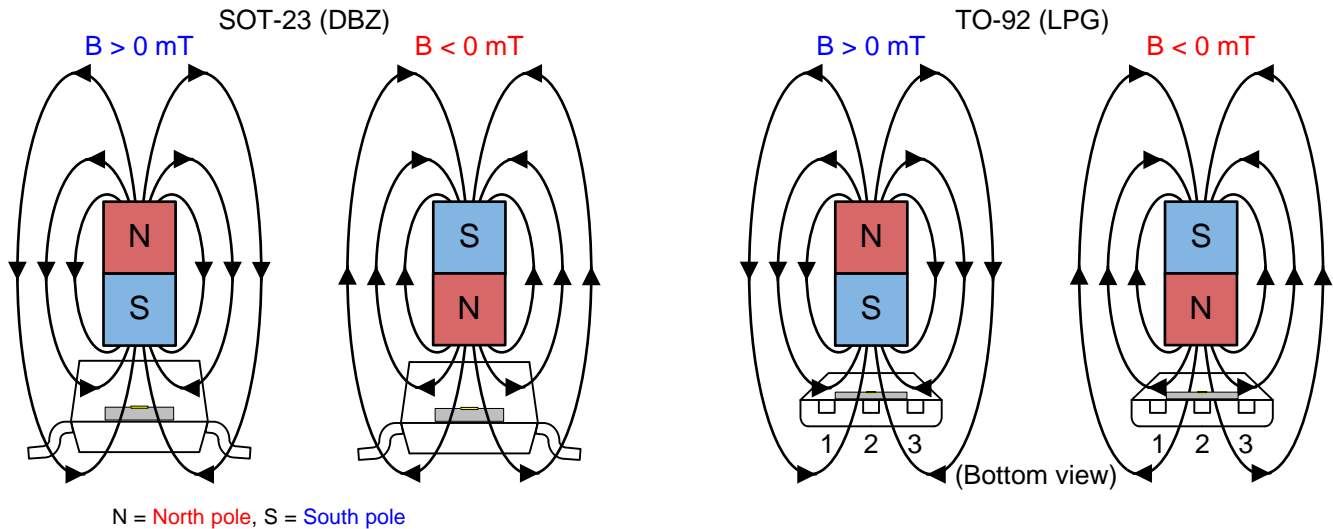


Figure 11. Field Direction Definition

7.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP} , then the device output is indeterminate and can either be Hi-Z or Low. For the FA, AJ, and BI device versions, if the field strength is greater than B_{OP} , then the output is pulled low; if the field strength is less than B_{RP} , then the output is released. For the FI device version, if the field strength is greater than B_{OP} , then the output is Hi-Z; if the field strength is less than B_{RP} , then the output is pulled Low.

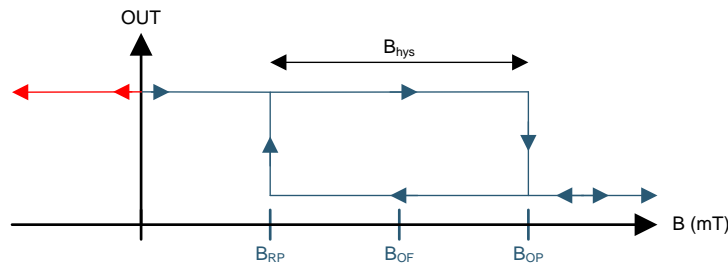


Figure 12. Output State

Feature Description (continued)

7.3.3 Power-On Time

After applying V_{CC} to the DRV5023 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on} . This pulse can allow the host processor to determine when the DRV5023 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field $B > B_{OP}$ and $B < B_{RP}$.

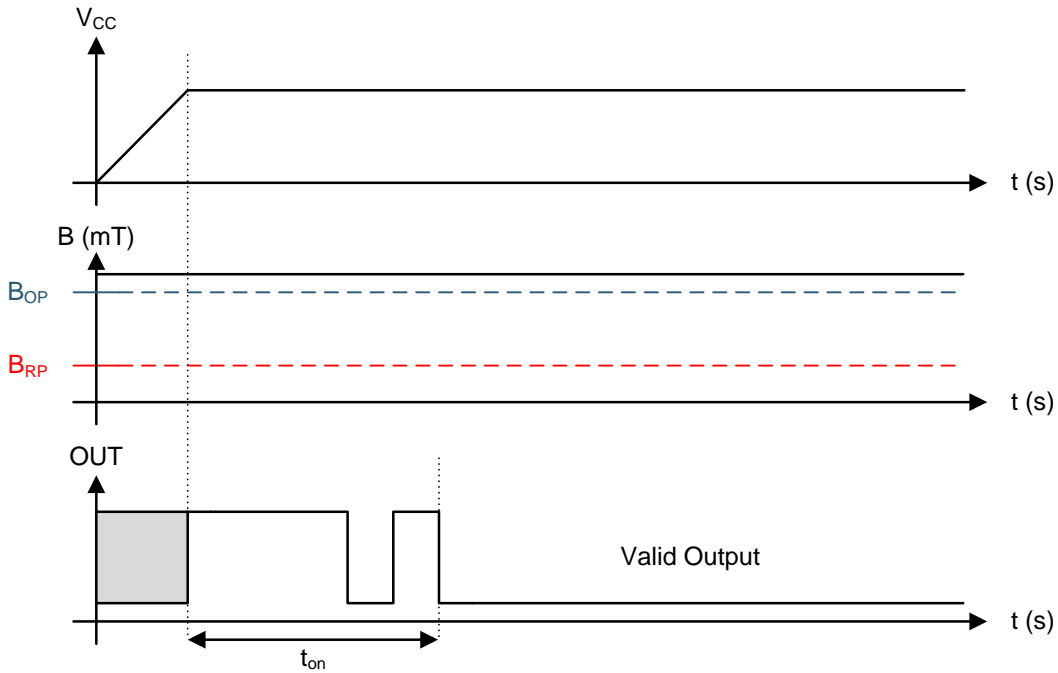


Figure 13. Case 1: Power On When $B > B_{OP}$

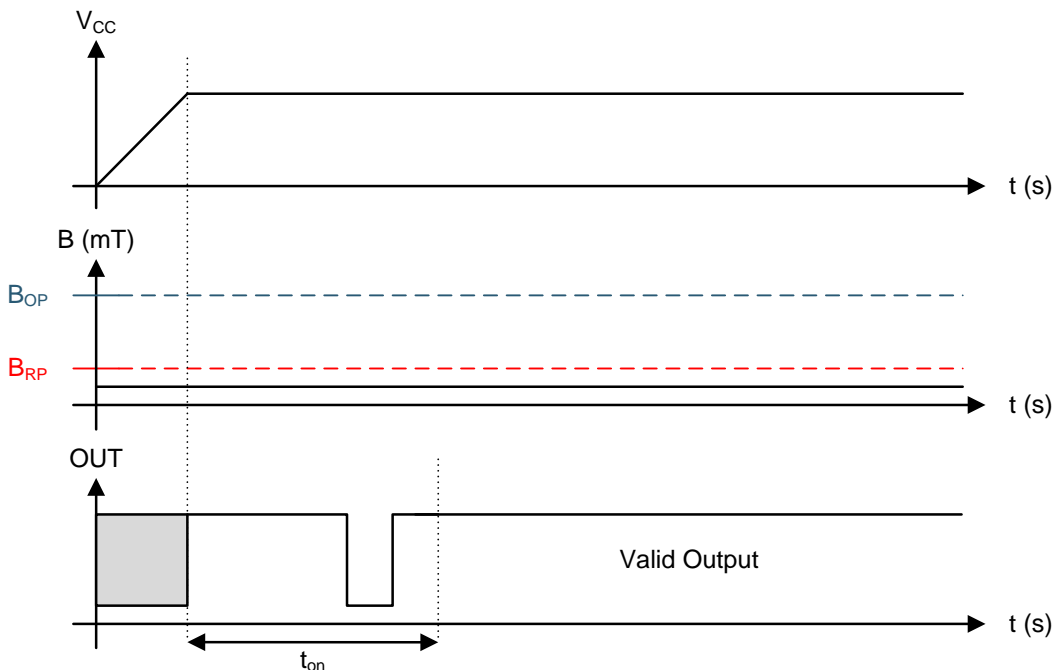


Figure 14. Case 2: Power On When $B < B_{RP}$

Feature Description (continued)

If the device is powered on with the magnetic field strength $B_{RP} < B < B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on} , a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on} , if the magnetic field changes such that $B_{OP} < B$, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

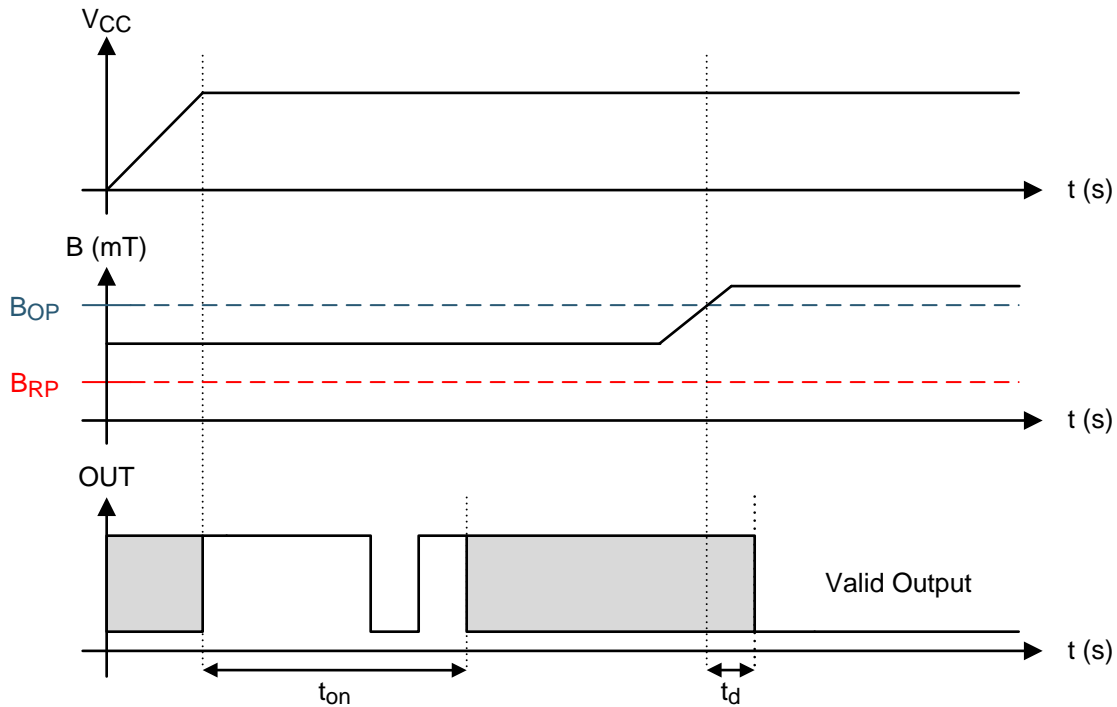


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$

Feature Description (continued)

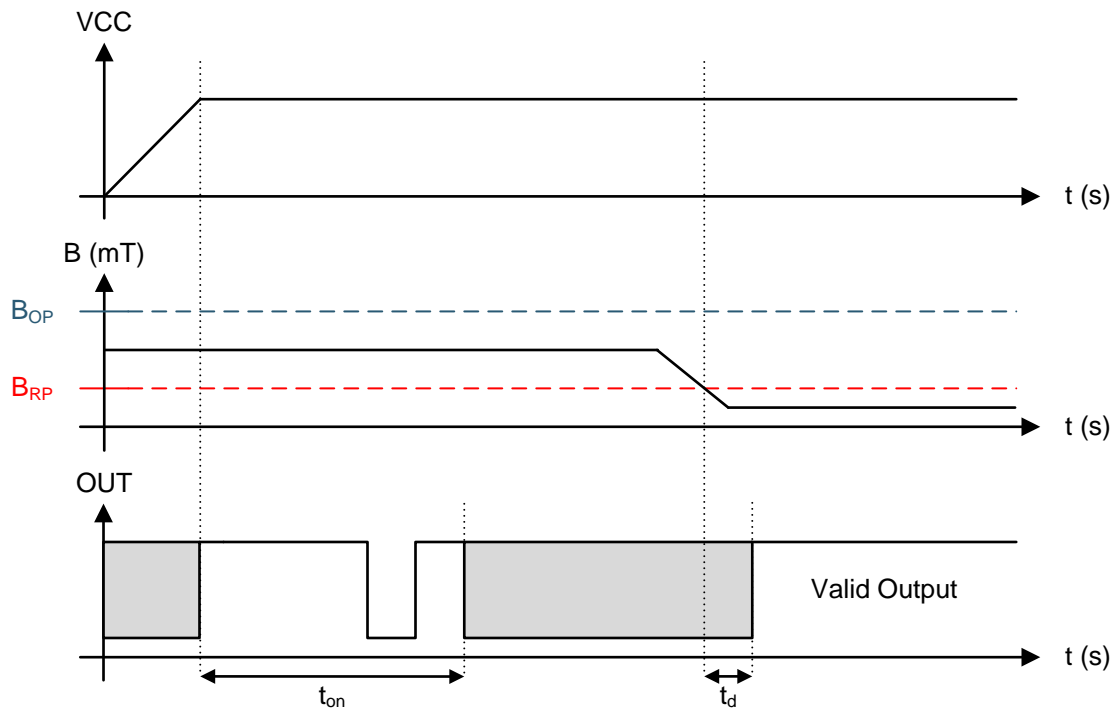


Figure 16. Case 4: Power On When $B_{RP} < B < B_{OP}$, Followed by $B < B_{RP}$

Feature Description (continued)

7.3.4 Output Stage

The DRV5023 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using [Equation 1](#).

$$\frac{V_{\text{ref max}}}{30 \text{ mA}} \leq R1 \leq \frac{V_{\text{ref min}}}{100 \mu\text{A}} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of R1 > 500 Ω to ensure the output driver can pull the OUT pin close to GND.

NOTE

V_{ref} is not restricted to V_{CC} . The allowable voltage range of this pin is specified in the [Absolute Maximum Ratings](#).

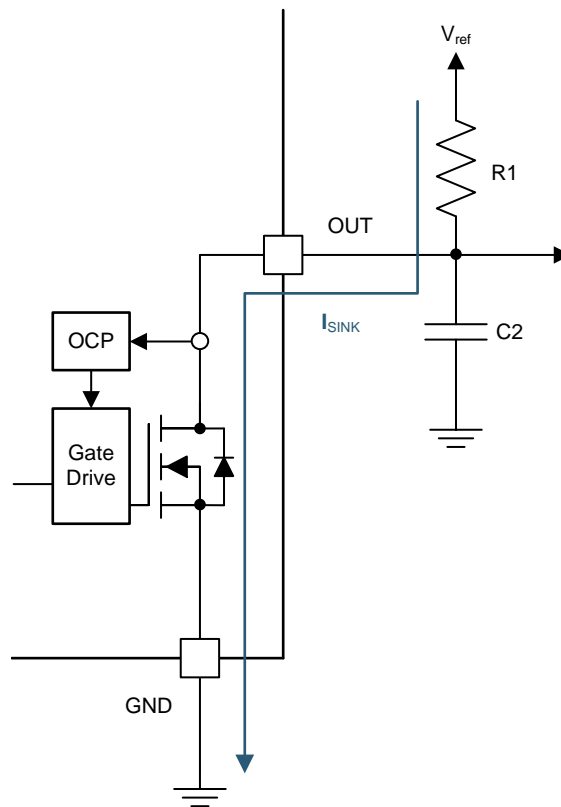


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in [Equation 2](#).

$$2 \times f_{\text{BW}} \text{ (Hz)} < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do not require this C2 filtering capacitor.

Feature Description (continued)

7.3.5 Protection Circuits

The DRV5023 device is fully protected against overcurrent and reverse-supply conditions.

7.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP} . During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.5.2 Load Dump Protection

The DRV5023 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand $V_{CC} = 40$ V. No current-limiting series resistor is required for this protection.

7.3.5.3 Reverse Supply Protection

The DRV5023 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to -22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the [Absolute Maximum Ratings](#).

Table 1.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load dump	$38\text{ V} < V_{CC} < 40\text{ V}$	Operating	Device will operate for a transient duration	$V_{CC} \leq 38\text{ V}$
Reverse supply	$-22\text{ V} < V_{CC} < 0\text{ V}$	Disabled	Device will survive this condition	$V_{CC} \geq 2.5\text{ V}$

7.4 Device Functional Modes

The DRV5023 device is active only when V_{CC} is between 2.5 and 38 V.

When a reverse supply condition exists, the device is inactive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5023 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Standard Circuit

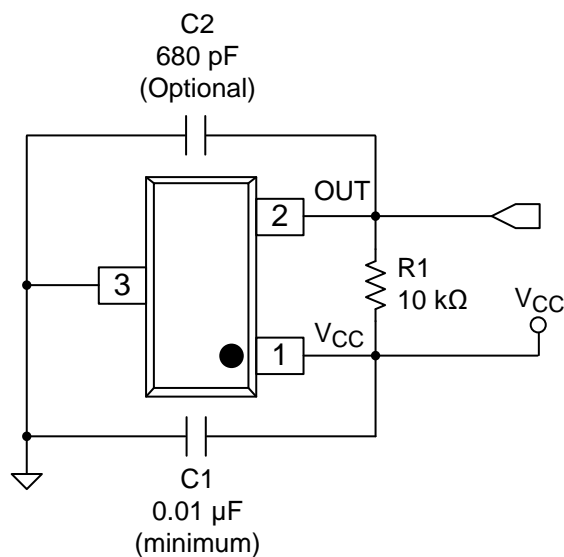


Figure 18. Typical Application Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#) as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

8.2.1.2 Detailed Design Procedure

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01- μ F (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	Optional: Place a ceramic capacitor to GND
R1	OUT	REF ⁽¹⁾	Requires a resistor pullup

(1) REF is not a pin on the DRV5023 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC} .

8.2.1.2.1 Configuration Example

In a 3.3-V system, $3.2\text{ V} \leq V_{\text{ref}} \leq 3.4\text{ V}$. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{\text{ref max}}}{30\text{ mA}} \leq R1 \leq \frac{V_{\text{ref min}}}{100\text{ }\mu\text{A}} \quad (3)$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\text{ V}}{30\text{ mA}} \leq R1 \leq \frac{3.2\text{ V}}{100\text{ }\mu\text{A}} \quad (4)$$

Therefore:

$$113\text{ }\Omega \leq R1 \leq 32\text{ k}\Omega \quad (5)$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 k Ω for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{\text{BW}}\text{ (Hz)} < \frac{1}{2\pi \times R1 \times C2} \quad (6)$$

For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\text{ kHz} < \frac{1}{2\pi \times R1 \times C2} \quad (7)$$

An R1 value of 10 k Ω and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

A selection of R1 = 10 k Ω and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

8.2.1.3 Application Curves

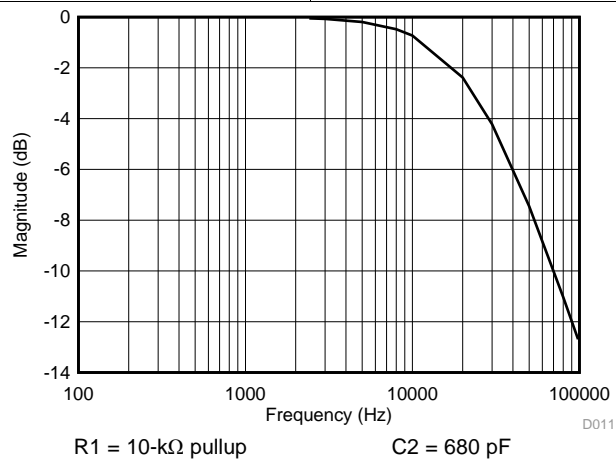
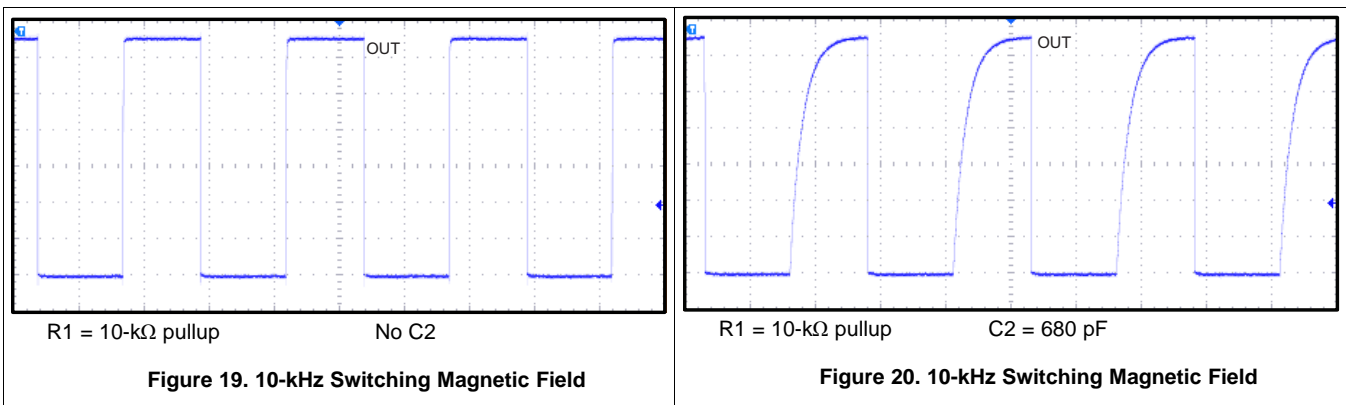


Figure 21. Low-Pass Filtering

8.2.2 Alternative Two-Wire Application

For systems that require minimal wire count, the device output can be connected to V_{CC} through a resistor, and the total supplied current can be sensed near the controller.

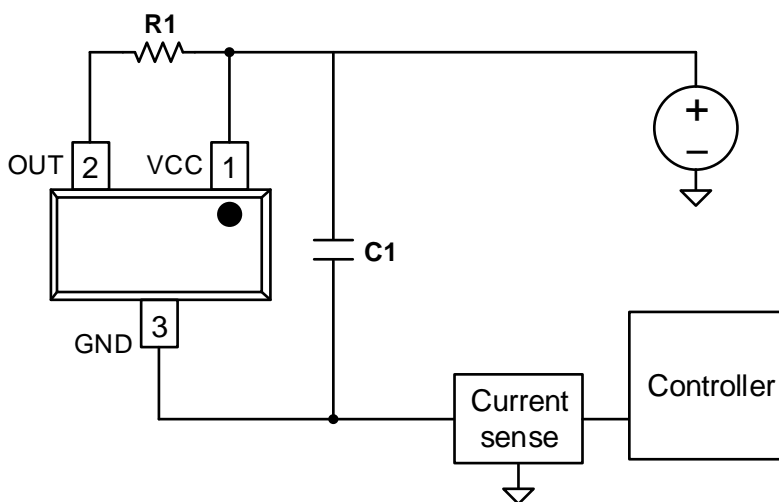


Figure 22. 2-Wire Application

Current can be sensed using a shunt resistor or other circuitry.

8.2.2.1 Design Requirements

Table 4 lists the related design parameters.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	12 V
OUT resistor	R1	1 k Ω
Bypass capacitor	C1	0.1 μ F
Current when $B < B_{RP}$	$I_{RELEASE}$	About 3 mA
Current when $B > B_{OP}$	$I_{OPERATE}$	About 15 mA

8.2.2.2 Detailed Design Procedure

When the open-drain output of the device is high-impedance, current through the path equals the I_{CC} of the device (approximately 3 mA).

When the output pulls low, a parallel current path is added, equal to $V_{CC} / (R1 + r_{DS(on)})$. Using 12 V and 1 k Ω , the parallel current is approximately 12 mA, making the total current approximately 15 mA.

The local bypass capacitor C1 should be at least 0.1 μ F, and a larger value if there is high inductance in the power line interconnect.

9 Power Supply Recommendations

The DRV5023 device is designed to operate from an input voltage supply (V_M) range between 2.5 and 38 V. A 0.01- μ F (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5023 device as possible.

10 Layout

10.1 Layout Guidelines

The bypass capacitor should be placed near the DRV5023 device for efficient power delivery with minimal inductance. The external pullup resistor should be placed near the microcontroller input to provide the most stable voltage at the input; alternatively, an integrated pullup resistor within the GPIO of the microcontroller can be used.

Generally, using PCB copper planes underneath the DRV5023 device has no effect on magnetic flux, and does not interfere with device performance. This is because copper is not a ferromagnetic material. However, if nearby system components contain iron or nickel, they may redirect magnetic flux in unpredictable ways.

10.2 Layout Example

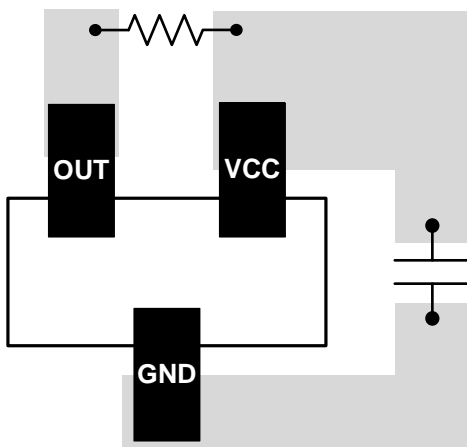


Figure 23. DRV5023 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デバイス名の見方

DRV5023のデバイス名の各部の読み方を図 24に示します。

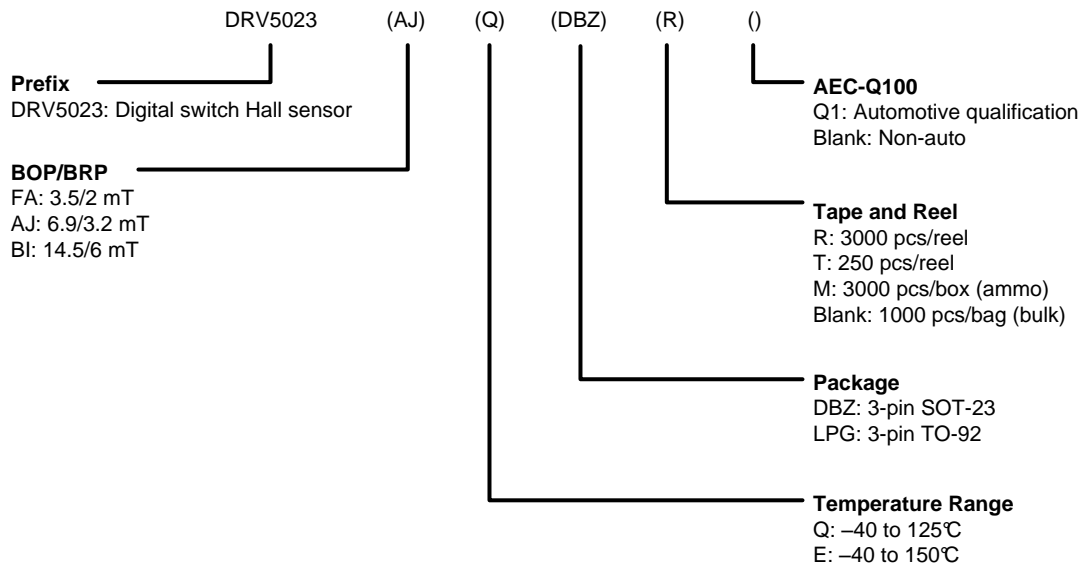


図 24. デバイス名の見方

11.1.2 デバイスのマーキング

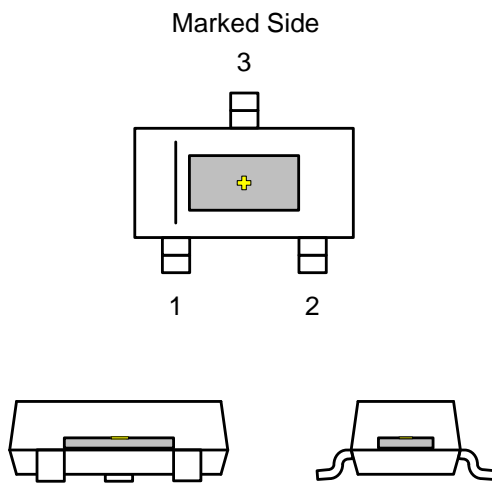


図 25. SOT-23 (DBZ)パッケージ

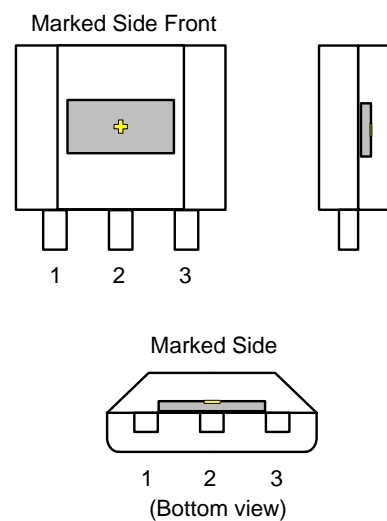


図 26. TO-92 (LPG)パッケージ

⊕はホール効果センサを示します(実際の大きさに比例してはいません)。ホール素子はパッケージの中心に、許容誤差 $\pm 100\mu\text{m}$ で配置されています。ホール素子の高さは、パッケージの底面から計測して、DBZパッケージでは $0.7\text{mm}\pm 50\mu\text{m}$ 、LPGパッケージでは $0.987\text{mm}\pm 50\mu\text{m}$ です。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5023AJQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG SN	Level-1-260C-UNLIM	-40 to 125	(+PLAJ, 1J22)	Samples
DRV5023AJQDBZT	OBSOLETE	SOT-23	DBZ	3		TBD	Call TI	Call TI	-40 to 125	(+PLAJ, 1J22)	
DRV5023AJQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+PLAJ	Samples
DRV5023AJQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+PLAJ	Samples
DRV5023BIQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG SN	Level-1-260C-UNLIM	-40 to 125	(+PLBI, 1J32)	Samples
DRV5023BIQDBZT	OBSOLETE	SOT-23	DBZ	3		TBD	Call TI	Call TI	-40 to 125	(+PLBI, 1J32)	
DRV5023BIQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+PLBI	Samples
DRV5023BIQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+PLBI	Samples
DRV5023FAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(+PLFA, 1J42)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV5023 :

- Automotive : [DRV5023-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5023AJQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
DRV5023BIQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
DRV5023FAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023FAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

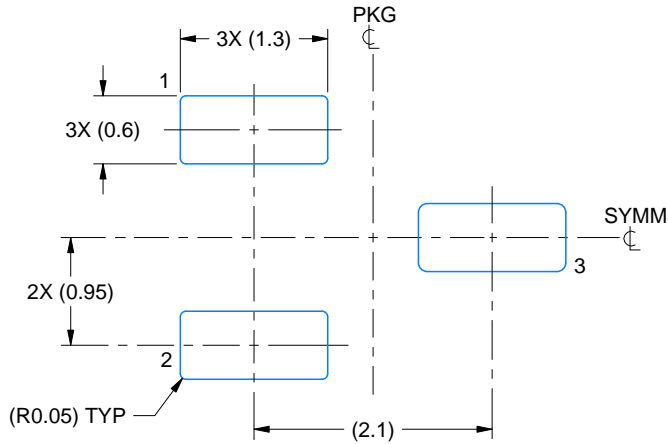
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5023AJQDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
DRV5023BIQDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
DRV5023FAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5023FAQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0

EXAMPLE BOARD LAYOUT

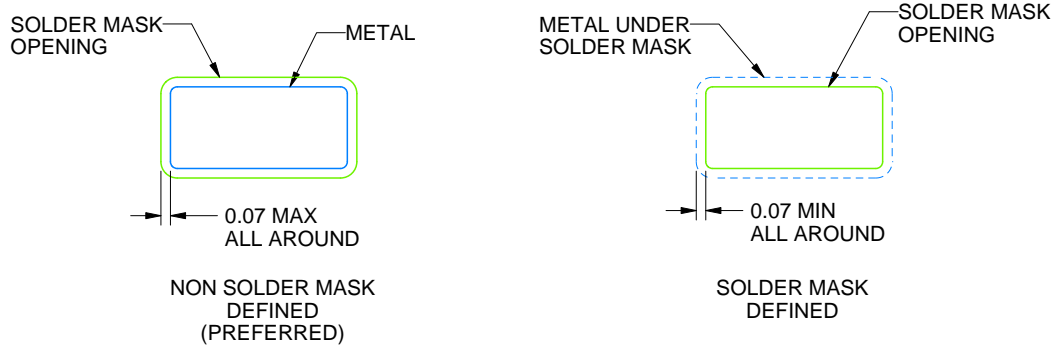
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

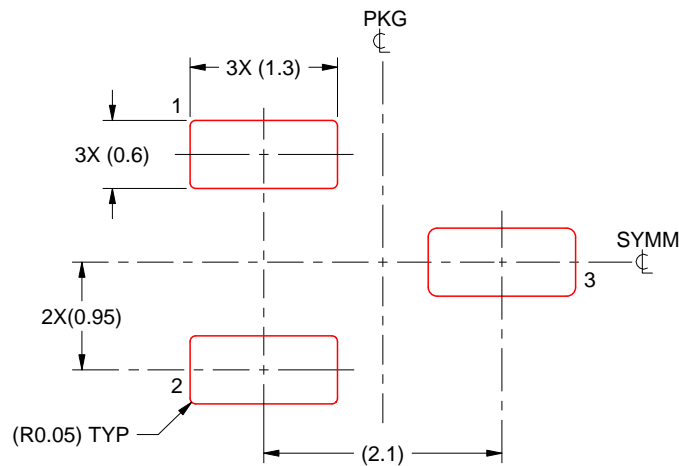
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

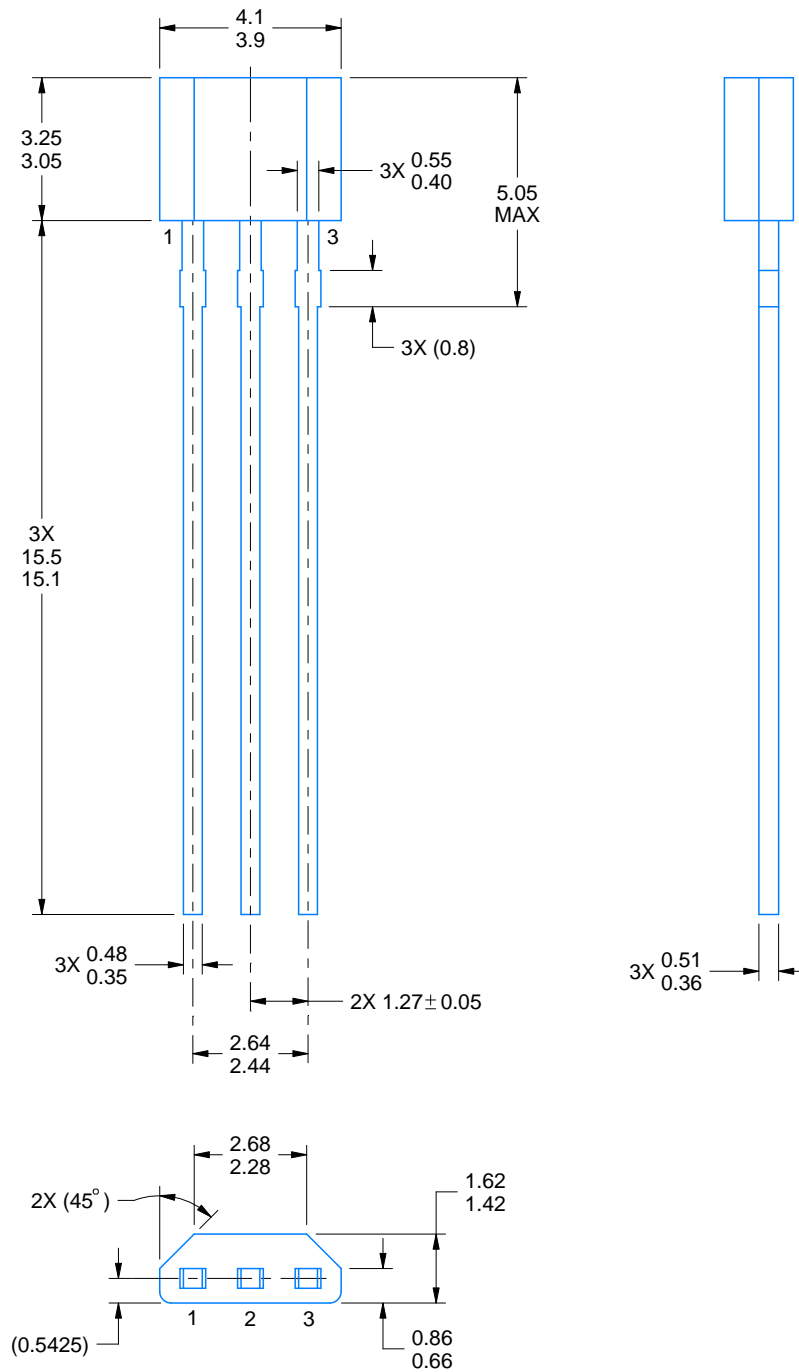
LPG0003A



PACKAGE OUTLINE

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4221343/C 01/2018

NOTES:

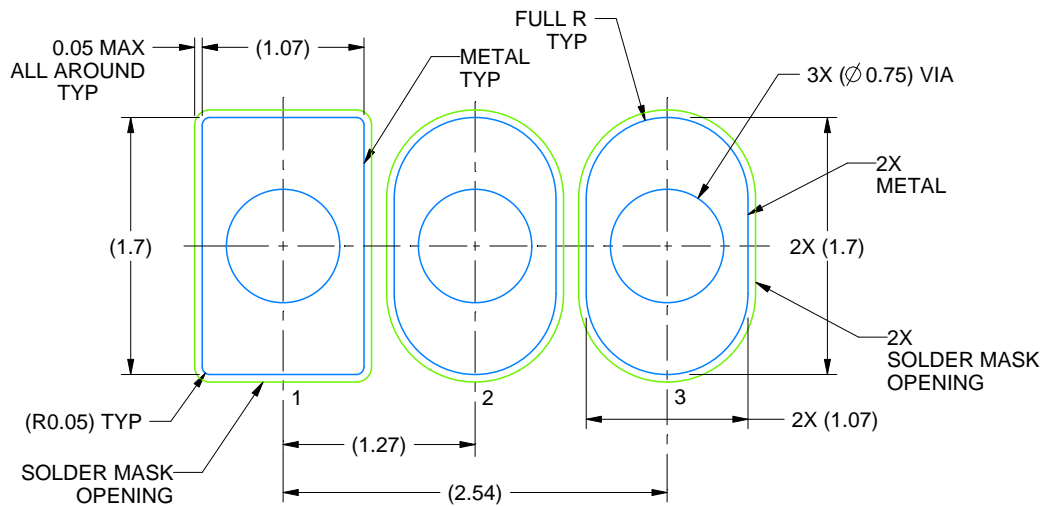
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

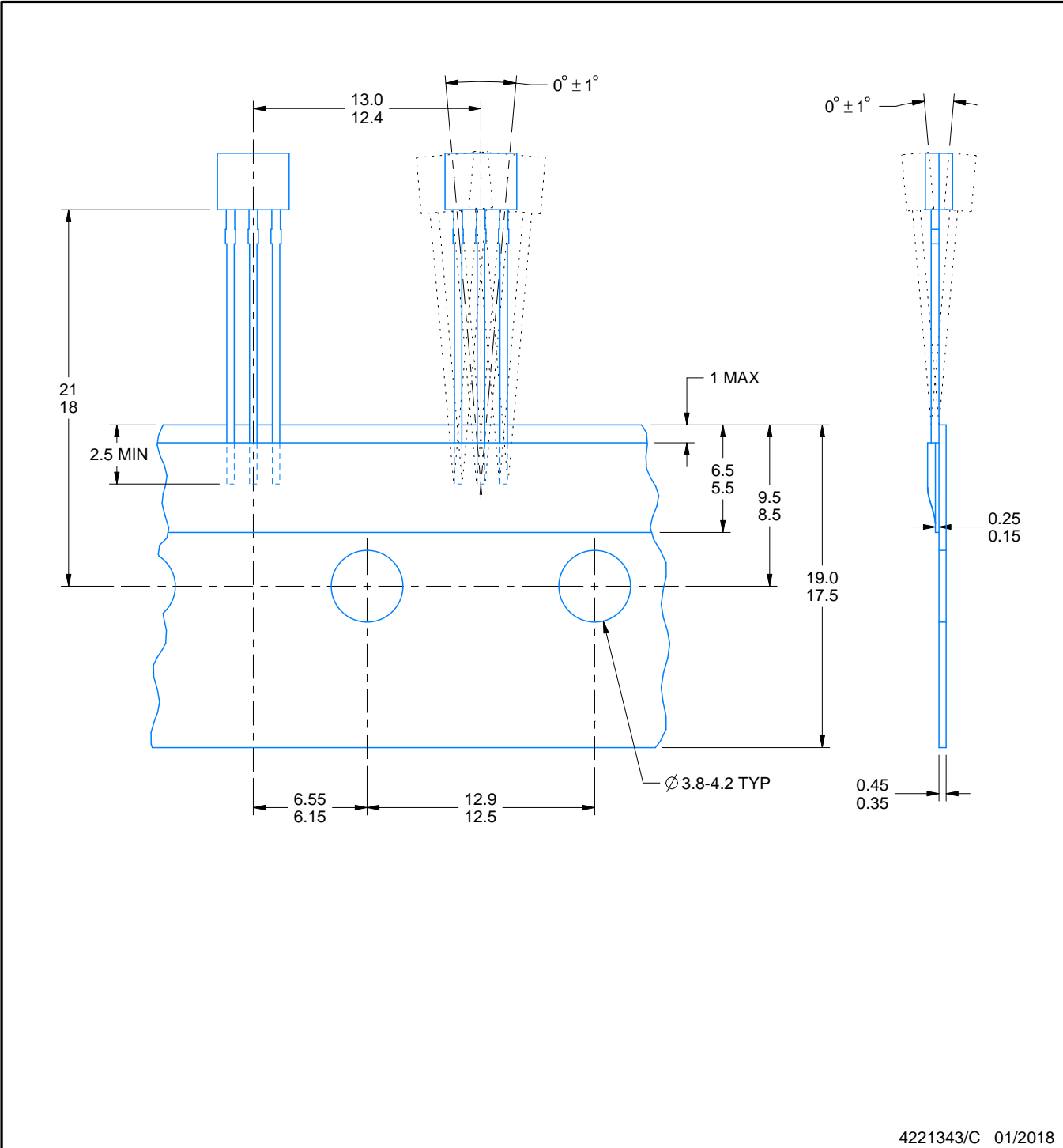
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4221343/C 01/2018

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated