DCH010505D, DCH010505S
DCH010512D, DCH010512S
DCH010515D, DCH010515S
JAJS137I – NOVEMBER 2006 – REVISED NOVEMBER 2016

DCH0105xxx 出力電力1W/絶縁耐圧3kV、小型非安定型DC/DCコンバータ

1 特長

- 最大78%の効率
- 3kVDC絶縁(動作時)
- UL60950認定済み製品
- 業界標準のフットプリント
- JEDEC 7ピンSIPパッケージ

2 アプリケーション

- 使用ポイントでの電力変換
- グランド・ループの排除
- データ収集
- 産業用制御および計測機器
- Test Equipment™

3 概要

DCH010505、DCH010512、DCH010515デバイスは、小型で1W、3kVの絶縁耐性を持つDC/DCコンバータのファミリです。DCH01シリーズは業界標準の7ピンSIPパッケージに搭載され、必要な外付け部品が最小限で、基板の面積を節約できます。DCH01シリーズには、シングルとデュアル両方の分離電源出力があります。

集積度の高いパッケージ設計を使用しているため、信頼性が高く、非常に電力密度の高い製品です。高性能と小さなサイズから、DCH01は信号チェーン・アプリケーションやグランド・ループの排除など、広範なアプリケーションに適しています。

警告

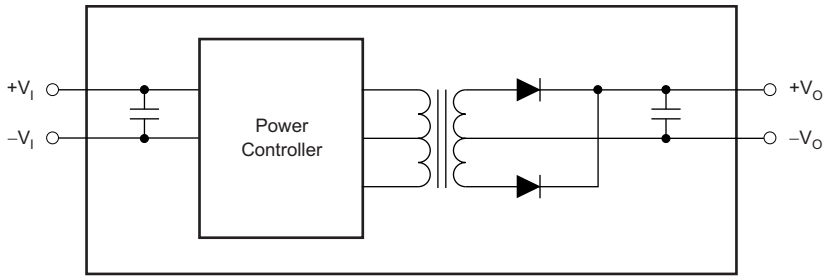
この製品の動作絶縁は、信号の絶縁のみを意図したものです。強化絶縁を必要とする安全用の絶縁回路の一部として使用してはいけません。***Feature Description*** の定義を参照してください。

製品情報(1)

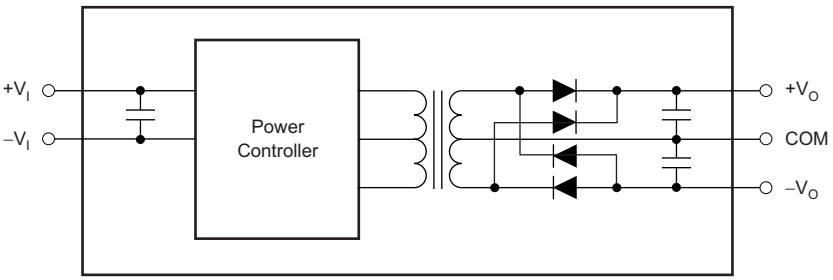
型番	パッケージ	本体サイズ(公称)
DCH0105xx	EDJ-Single (7)	19.50mm×10.00mm
	EDJ-Dual (7)	19.50mm×10.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

シングル出力のブロック図



デュアル出力のブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision H (January 2009) から **Revision I** に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Changed *Ordering Information* to *Device Comparison Tables* ... 3
- Deleted Wave soldering temperature (260°C maximum) from *Absolute Maximum Ratings* table ... 4
- Added *Thermal Information* table ... 4
- Added *Isolation* subsection to the *Feature Description* ... 10

5 Device Comparison Tables

Table 1. DCH01 Products

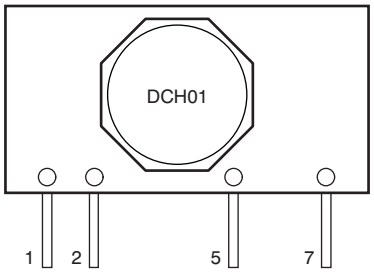
MODEL	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)	OUTPUT POWER (W)	ISOLATION VOLTAGE (kVDC)	PACKAGE-LEAD
DCH010505S	5 ± 10%	5	200	1	3	SIP-7
DCH010512S	5 ± 10%	12	83	1	3	SIP-7
DCH010515S	5 ± 10%	15	67	1	3	SIP-7
DCH010505D	5 ± 10%	±5	±100	1	3	SIP-7
DCH010512D	5 ± 10%	±12	±42	1	3	SIP-7
DCH010515D	5 ± 10%	±15	±33	1	3	SIP-7

Table 2. Part Numbering Scheme

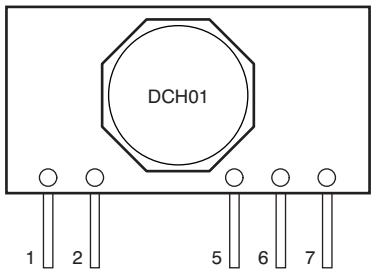
PRODUCT LINE	POWER	INPUT VOLTAGE	OUTPUT VOLTAGE	SINGLE/DUAL	PACKAGE	PIN CONFIG	TRANSPORT MEDIA
DCH	01	05	05	S	N	7	
H = 3 kV, unregulated output	01 = 1 W	05 = 5 V	05 = 5 V 12 =12 V 15 = 15 V	S = Single D = Dual	N = SIP Thru-hole	7 = SIP-7	Blank = Tray

6 Pin Configuration and Functions

EDJ Package
7-Pin SIP (Single)
Top View



EDJ Package
7-Pin SIP (Dual)
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	EDJ (SINGLE)	EDJ (DUAL)		
$-V_I$	2	2	I	Input side common
$+V_I$	1	1	I	Voltage input
$-V_O$	5	5	O	–Voltage out
$+V_O$	7	7	O	+Voltage out
COM	—	6	—	Output side common

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage (5-V input models)		7	V
Storage temperature, T_{stg}	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$+V_I$	Input voltage	4.5	5.5	V
T_A	Operating ambient temperature	–40	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		DCH01 SERIES		UNIT
		EDJ (SIP-SINGLE)	EDJ (SIP-DUAL)	
		7 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66	66	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66	66	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

At T_A = 25°C and V_I = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage	All devices nominal			5		V
V_{NOM}	Output voltage	100% load(1)	DCH010505S		5.1		V
			DCH010505D		±5.2		
			DCH010512S		12.4		
			DCH010512D		±12.5		
			DCH010515S		15.2		
			DCH010515D		±15.3		
	Load regulation	10% to 100% load(2)	DCH010505S		10%		
			DCH010505D		9%		
			DCH010512S		6%		
			DCH010512D		5%		
			DCH010515S		6%		
			DCH010515D		5%		
	Output ripple	100% LOAD(1)	DCH010505S		35		mV_{PP}
			DCH010505D		20		
			DCH010512S		18		
			DCH010512D		19		
			DCH010515S		31		
			DCH010515D		22		
I_Q	Input current	No load; 0% load	DCH010505x		60		mA
			DCH010512x		65		
			DCH010515x		65		
	Efficiency	100% load(1)	DCH010505x		72%		
			DCH010512S		74%		
			DCH010512D		75%		
			DCH010515S		75%		
			DCH010515D		76%		
C_{ISO}	Barrier capacitance	DCH010505x & DCH010515x			3		pF
		DCH010512x			4		
	Output power	100% full load				1(3)	W
		Over current duration(3)				1	sec
	Input voltage on V_I			–10%		10%	
	Isolation voltage	100% tested for 1 second		3.5			kVDC
	Line regulation	1% change in V_I			1%		
	Switching frequency (f_{SW})				70		kHz
	Calculated reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C	Single output	18			FITS
			Dual output	22			

(1) 100% load current = 1 W / V_{NOM} typical.
(2) Load regulation = (V_O at 10% load – V_O at 100% load) / V_O at 100% load.
(3) This converter does not have continuous over-current protection.

7.6 Typical Characteristics

at T_A = 25°C and V_{IN} = 5 V (unless otherwise noted)

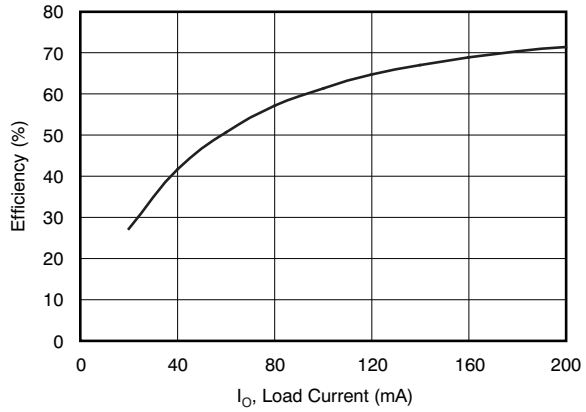


Figure 1. DCH010505S Efficiency

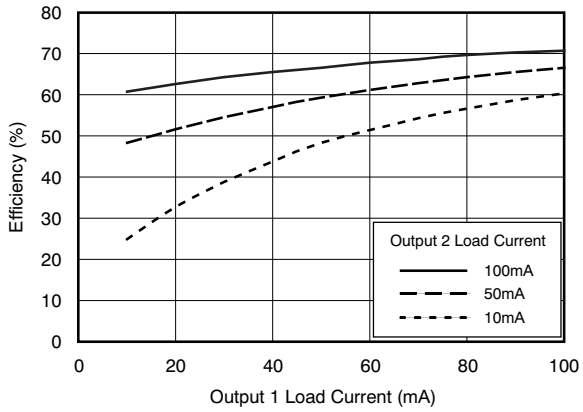


Figure 2. DCH010505D Efficiency

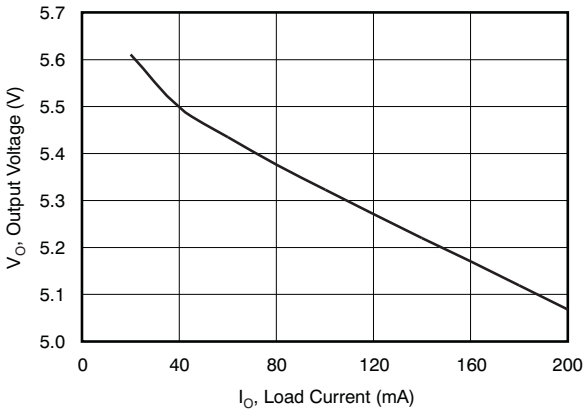


Figure 3. DCH010505S Load Regulation

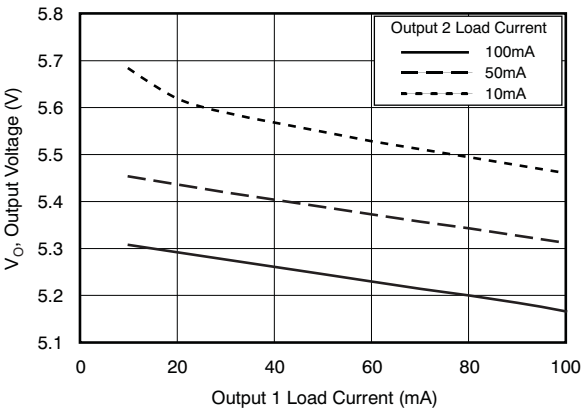


Figure 4. DCH010505D Load Regulation

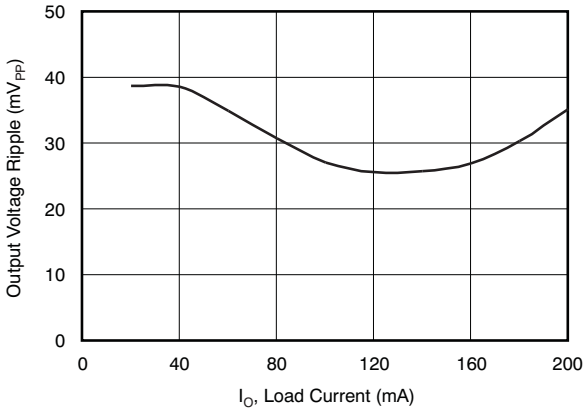


Figure 5. DCH010505S Ripple Voltage

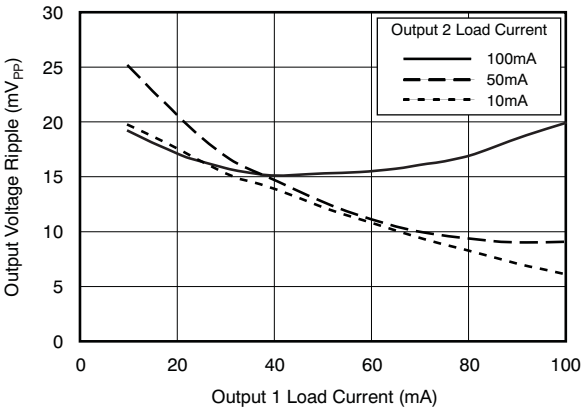


Figure 6. DCH010505D Ripple Voltage

Typical Characteristics (continued)

at T_A = 25°C and V_{IN} = 5 V (unless otherwise noted)

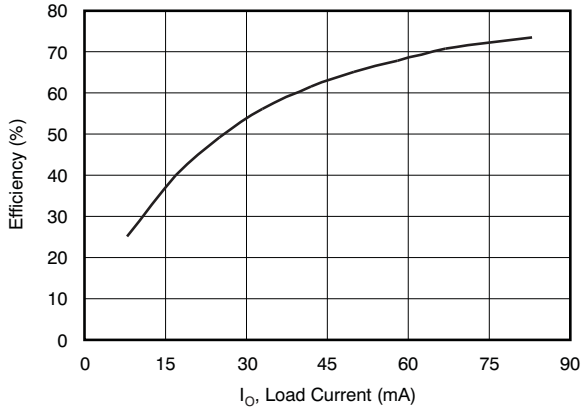


Figure 7. DCH010512S Efficiency

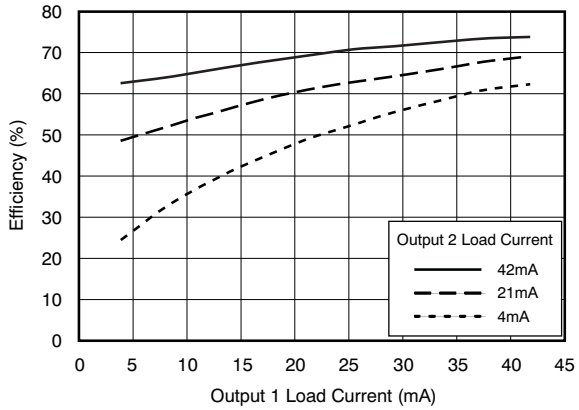


Figure 8. DCH010512D Efficiency

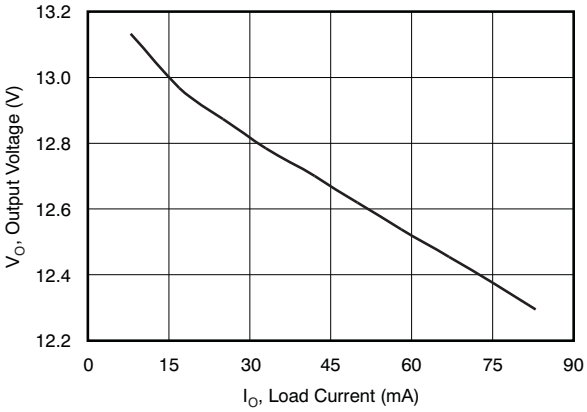


Figure 9. DCH010512S Load Regulation

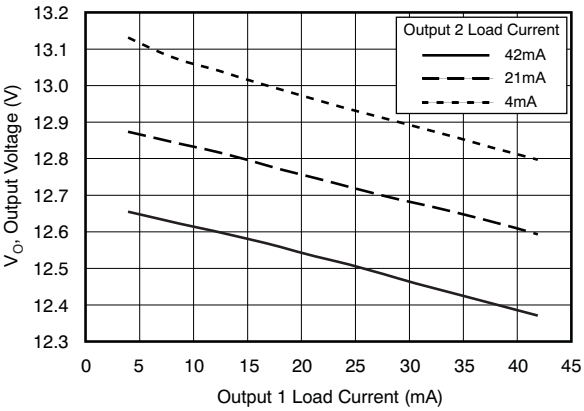


Figure 10. DCH010512D Load Regulation

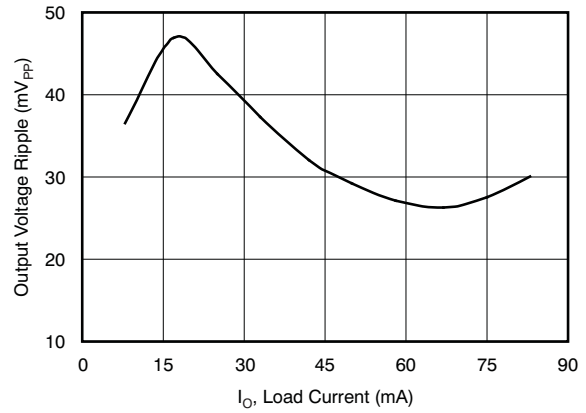


Figure 11. DCH010512S Ripple Voltage

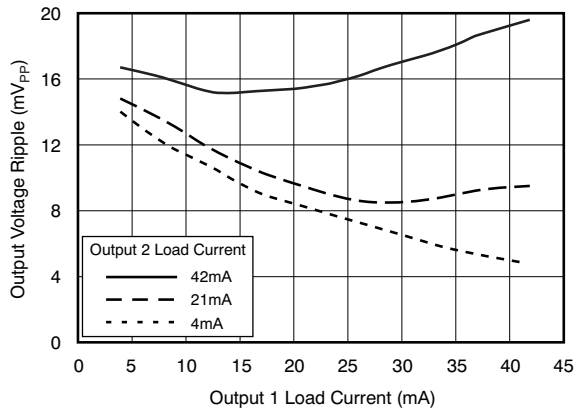


Figure 12. DCH010512D Ripple Voltage

Typical Characteristics (continued)

at T_A = 25°C and V_{IN} = 5 V (unless otherwise noted)

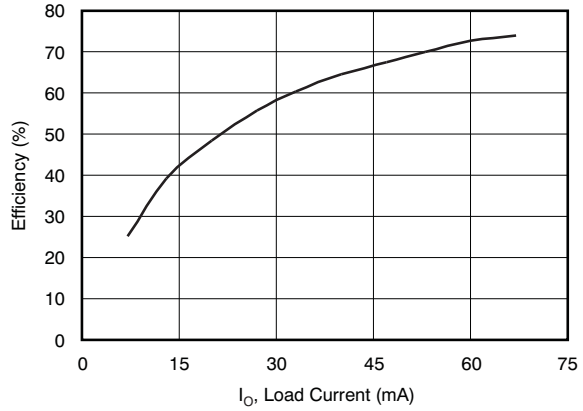


Figure 13. DCH010515S Efficiency

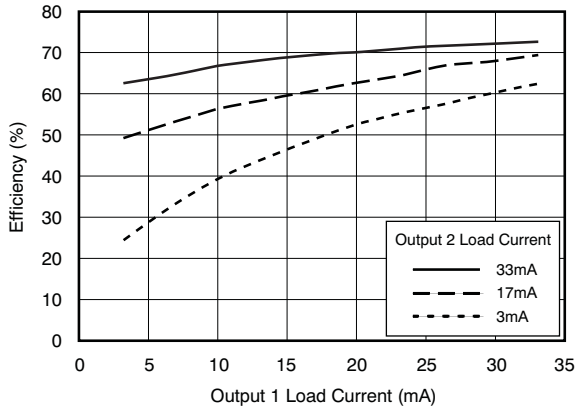


Figure 14. DCH010515D Efficiency

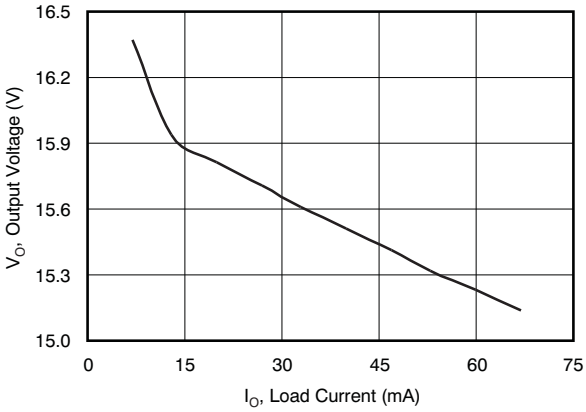


Figure 15. DCH010515S Load Regulation

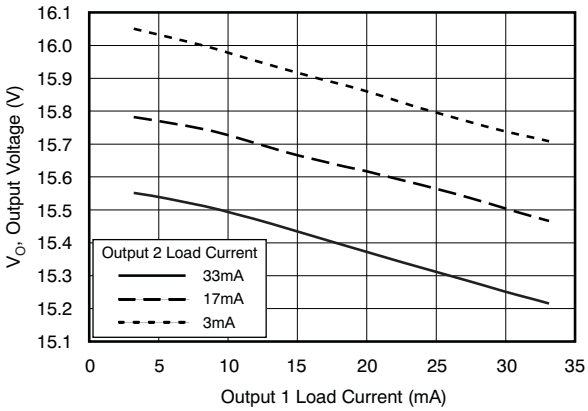


Figure 16. DCH010515D Load Regulation

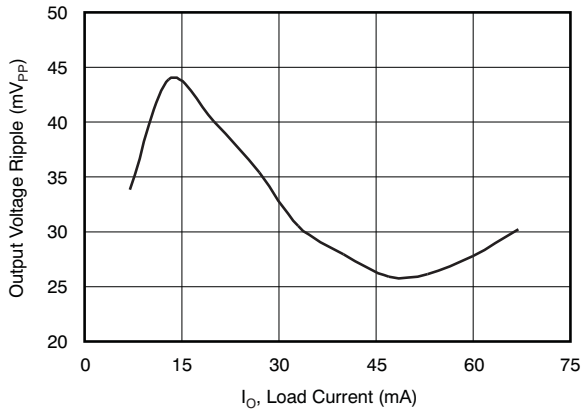


Figure 17. DCH010515S Ripple Voltage

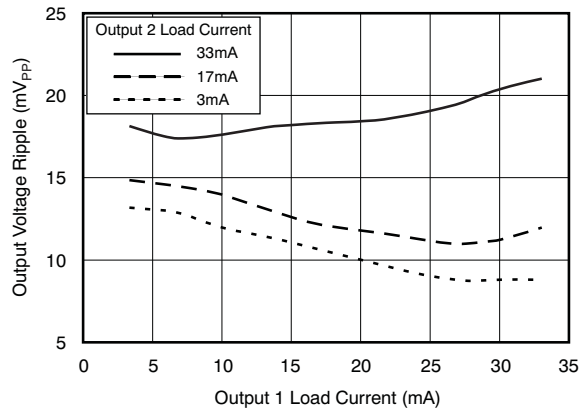


Figure 18. DCH010515D Ripple Voltage

Typical Characteristics (continued)

at T_A = 25°C and V_{IN} = 5 V (unless otherwise noted)

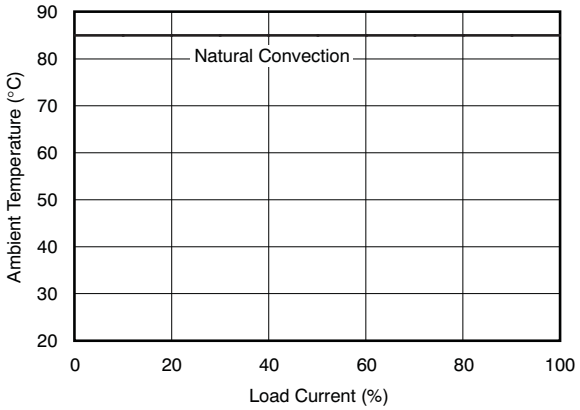


Figure 19. Safe Operating Area (All DCH0105 Products)

8 Detailed Description

8.1 Overview

The DCH01 series of DC/DC converters are 100% production tested at 3.5 kVDC for 1 second. The isolation test voltage represents an operational isolation to transient voltages and must not be relied upon for safety isolation.

The continuous voltage that can be applied across the DCH01 during normal operation must be < 60 VDC (within SELV limits).

8.1.1 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing can degrade the isolation capability of the DCH01.

8.2 Functional Block Diagrams

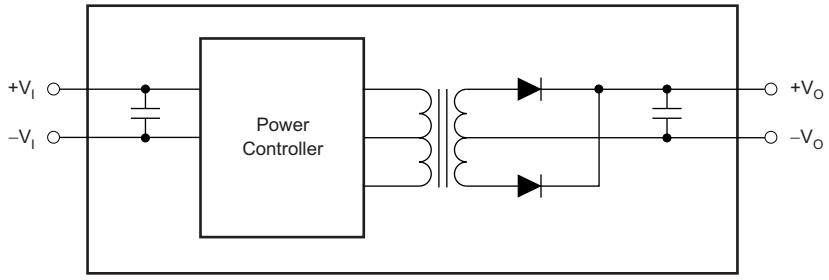


Figure 20. Single-Output Block Diagram

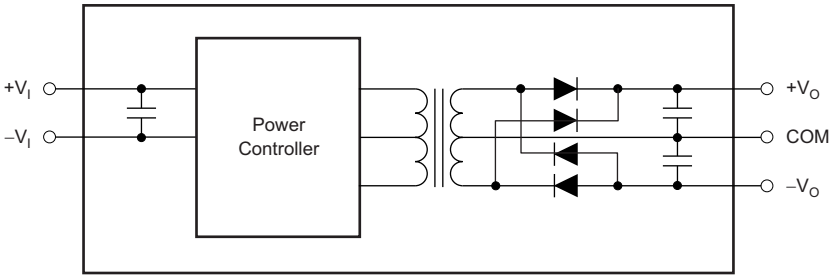


Figure 21. Dual-Output Block Diagram

8.3 Feature Description

8.3.1 Isolation

Underwriters Laboratories (UL)™ defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42-V peak or 60 V_{DC} for more than 1 second.

Feature Description (continued)

8.3.1.1 Operation or Functional Isolation

Operational or functional isolation is defined by the use of a high-potential (hipot) test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation must never be used as an element in a safety-isolation system.

8.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

8.3.1.3 Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than 42.4 V_{RMS} or 60 V_{DC}. Ensure that both input and output voltages maintain normal SELV limits. The isolation test voltage represents a measure of immunity to transient voltages.

WARNING

Do not use the device as an element of a safety isolation system when SELV is exceeded.

If the device is expected to function correctly with more than 42.4 V_{RMS} or 60 V_{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage. Further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

8.3.1.4 Isolation Voltage

Hipot test, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* are all terms that relate to the same thing: a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCH01 series of dc-dc converters are all 100% production tested at 3.5 kV_{DC} for 1 second.

8.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCH01 series of dc-dc converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of 1 second per test.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Optional Input and Output Filters

DCH01 power modules include internal input and output ceramic capacitors in all their designs. However, some applications require much lower levels of either input reflected or output ripple or noise. This application note describes various filters and design techniques found to be successful in reducing both input and output ripple or noise.

9.1.1.1 Input and Output Capacitors

The easiest way to reduce output ripple and noise is to add 1 or more ceramic capacitors each with a value of 4.7-µF or greater. Ceramic capacitors must be placed close to the output power terminals. A single 4.7-µF ceramic capacitor reduces the output ripple or noise by 10% to 30%.

Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple or noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of a 4.7-µF ceramic capacitor, near the input power pins, reduces reflected conducted ripple or noise by 30% to 50%.

The recommended maximum capacitive load on the output of the DCH01 is 100 µF (non-ceramic).

9.1.1.2 π Filters

If a further reduction in ripple or noise level is required for an application, higher order filters must be used. A π (pi) filter, employing a ferrite bead inductor in series with the input or output terminals of the regulator reduces the ripple or noise by at least 15-20 db (see Figure 22 and Figure 23). Ceramic capacitors are required for the inductor to be effective in reduction of ripple and noise.

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency. The placement of this filter is critical. It must be located as close as possible to the input or output pins to be efffective. The ferrite bead is small (5.1 mm x 3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite manufactures a surface-mount bead (part number 2773019447) or through hole (part number 2673000701) rated to 5 A. Inductors with a value from 1 µH to 5 µH can be used in place of the ferrite bead inductor.

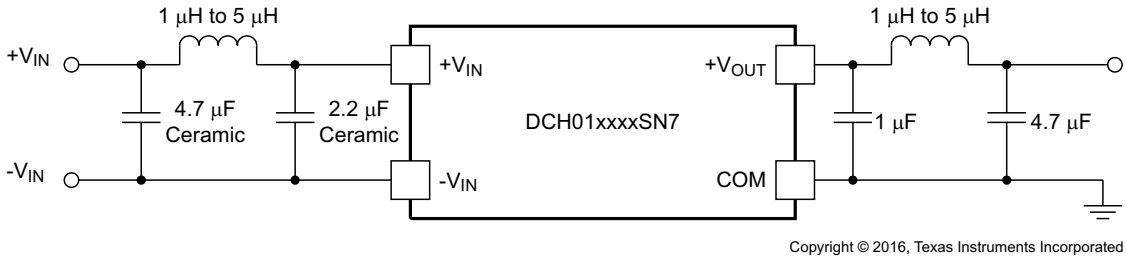


Figure 22. DCH01 Series π Filter

Application Information (continued)

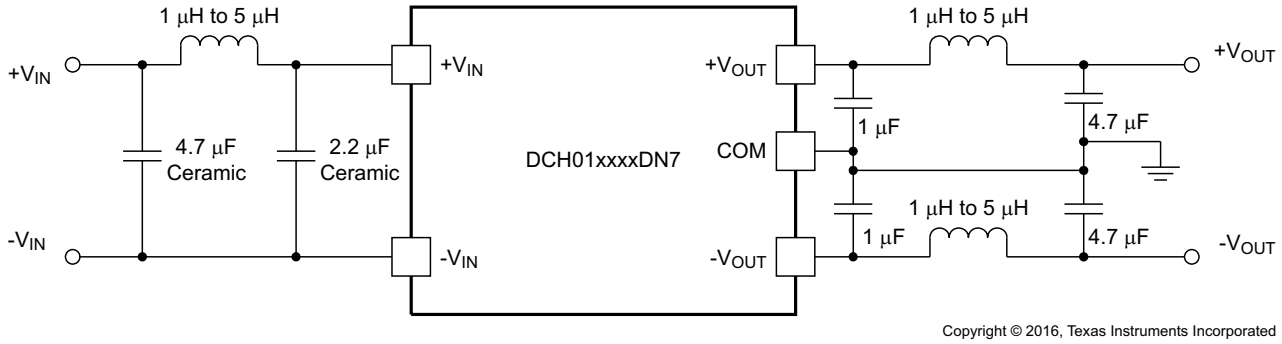


Figure 23. DCH01 Series π Filter (5 V at 1 W)

9.1.2 Start-Up

See Figure 24 for startup waveforms.

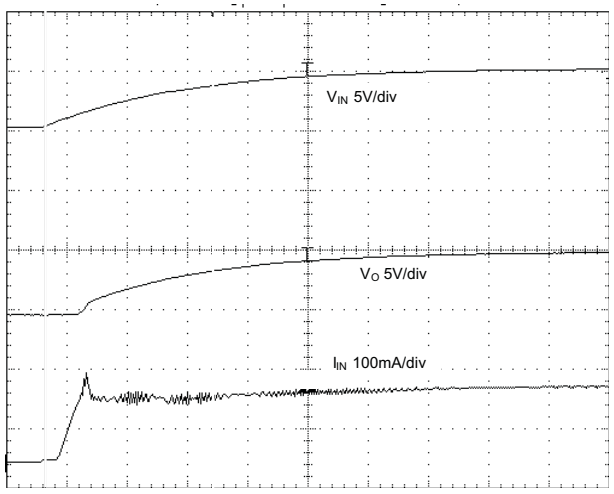


Figure 24. Startup Waveforms

9.1.3 Connecting the DCH01 in Series

It is possible to connect the outputs of multiple DCH01s in series to provide non-standard voltage rails. The outputs of dual output DCH01 versions can also be connected in series to provide 2 × the magnitude of V_O (as shown in Figure 25). For example, a dual 5-V DCH01 could be connected to provide a 10-V rail.

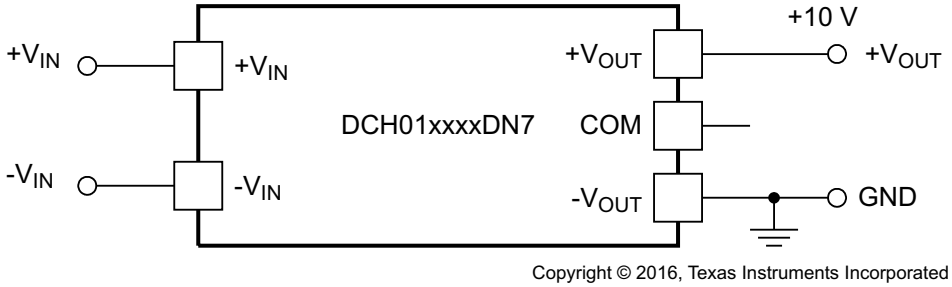


Figure 25. Connecting Dual Outputs in Series

9.1.4 Connecting the DCH01 in Parallel

If the output power from 1 DCH01 is not sufficient, it is possible to parallel the outputs of multiple DCH01s (as shown in Figure 26).

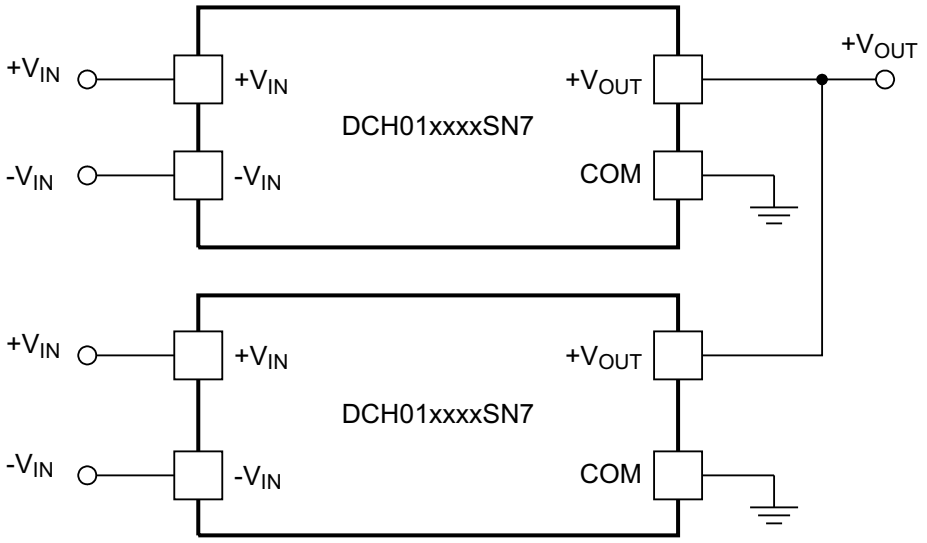


Figure 26. Connecting Multiple DCH01s in Parallel

9.2 Typical Application

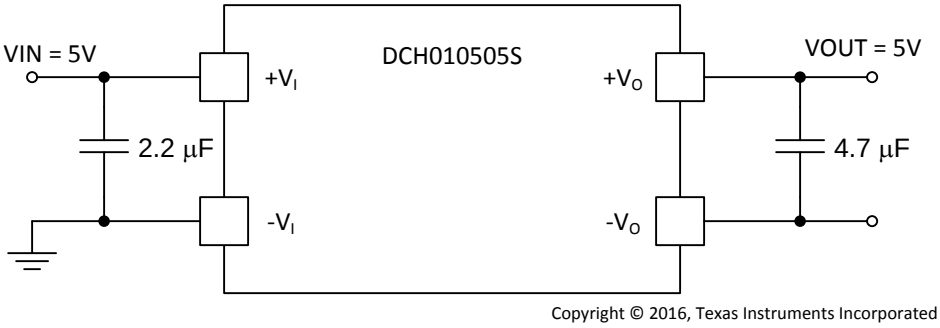


Figure 27. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 and follow the procedures in *Detailed Design Procedure*.

Table 3. Design Example Parameters

PARAMETER		VALUE
$+V_I$	Input voltage	5 V
$+V_O$	Output voltage	5 V
I_{OUT}	Output current rating	200 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Input Capacitor

For any DCH01 design, select a 2.2-µF, low-ESR, ceramic input capacitor to ensure a good startup performance.

9.2.2.2 Output Capacitor

For any DCH01 design, select a 4.7-µF, low-ESR, ceramic output capacitor to reduce output ripple.

9.2.3 Application Curves

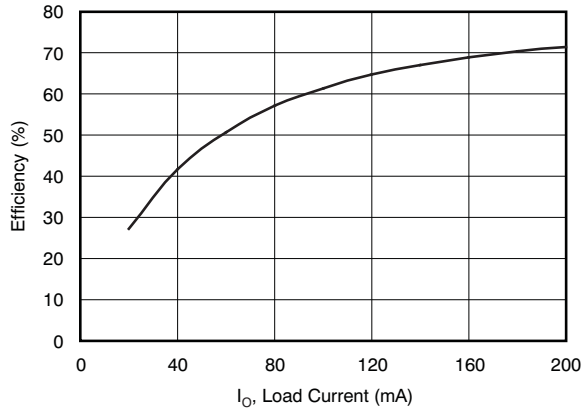


Figure 28. DCH010505S Efficiency

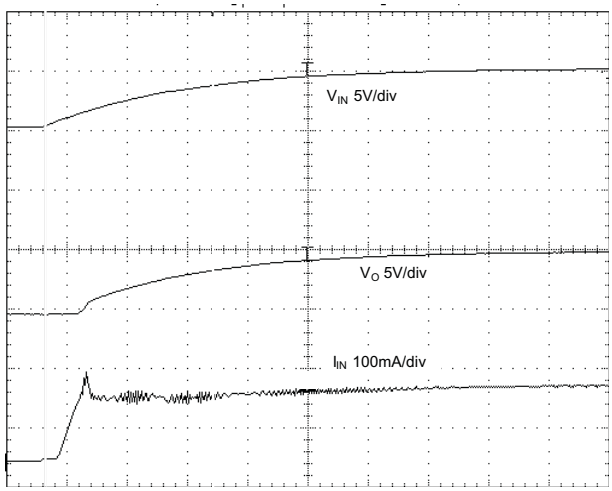


Figure 29. DCH010505 Startup Waveforms

10 Power Supply Recommendations

The DCH01 is a switching power supply, and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes must be used to connect the power to the input of DCH01. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

11 Layout

11.1 Layout Guidelines

Carefully consider the layout of the PCB in order for the best results to be obtained.

Input and output power and ground planes provide a low-impedance path for the input and output power. For the output, the positive and negative voltage outputs conduct through wide traces to minimize losses.

A good-quality, low-ESR, ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensure a smooth start-up.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

11.2 Layout Example

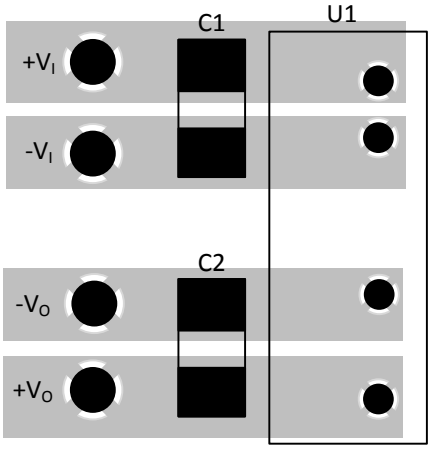


Figure 30. DCH01 Single Output Layout (Component-Side View)

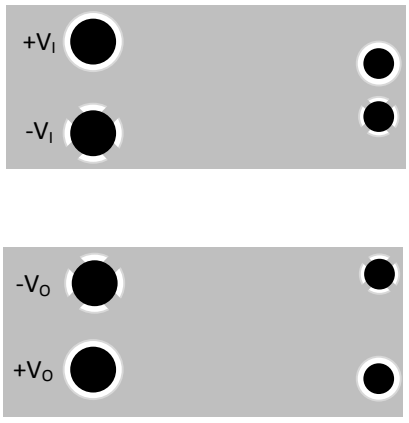


Figure 31. DCH01 Single Output Layout (Non-Component-Side View)

12 デバイスおよびドキュメントのサポート

12.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
DCH010505D	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCH010505S	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCH010512D	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCH010512S	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCH010515D	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCH010515S	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCH010505DN7	ACTIVE	SIP MODULE	EDJ	5	70	RoHS Exempt & Green	Call TI	N / A for Pkg Type	-40 to 85		Samples
DCH010505SN7	ACTIVE	SIP MODULE	EDJ	4	70	RoHS Exempt & Green	Call TI	N / A for Pkg Type	-40 to 85		Samples
DCH010512DN7	ACTIVE	SIP MODULE	EDJ	5	70	RoHS Exempt & Green	Call TI	N / A for Pkg Type	-40 to 85		Samples
DCH010512SN7	ACTIVE	SIP MODULE	EDJ	4	70	RoHS Exempt & Green	Call TI	N / A for Pkg Type	-40 to 85		Samples
DCH010515DN7	ACTIVE	SIP MODULE	EDJ	5	70	RoHS (In Work) & Green	Call TI	N / A for Pkg Type	-40 to 85		Samples
DCH010515SN7	ACTIVE	SIP MODULE	EDJ	4	70	RoHS Exempt & Green	Call TI	N / A for Pkg Type	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

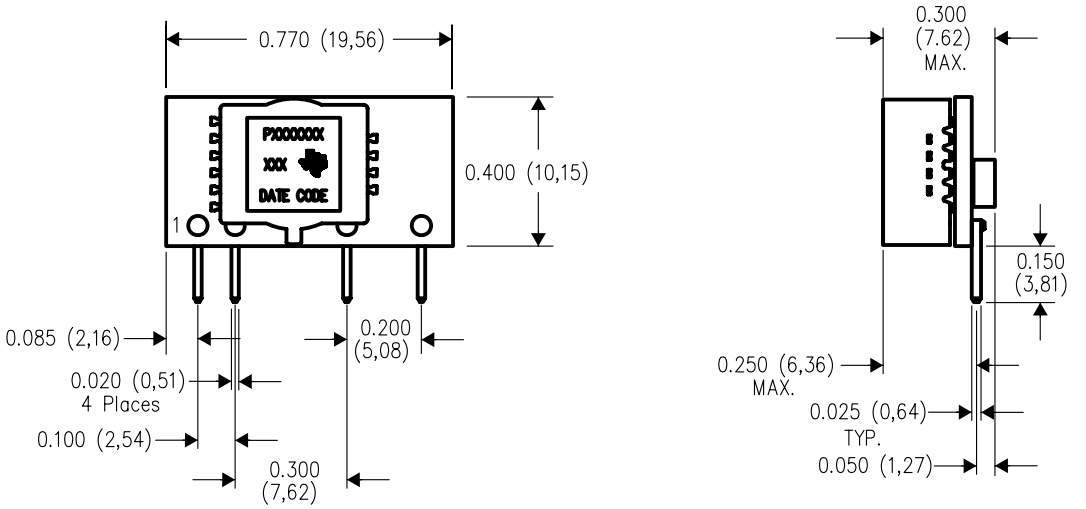
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

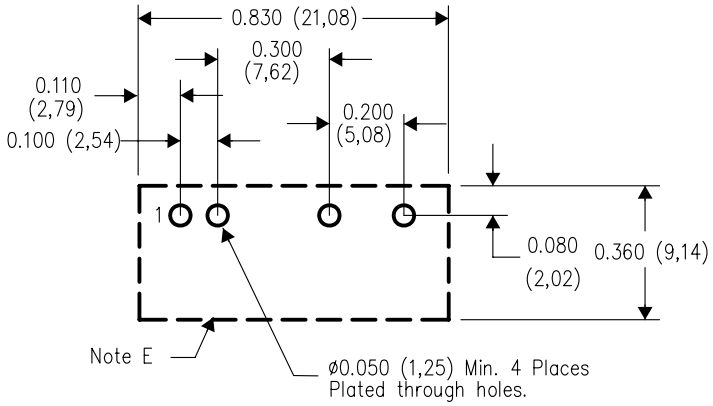
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

EDJ (R–PDSS–T4) DOUBLE SIDED MODULE

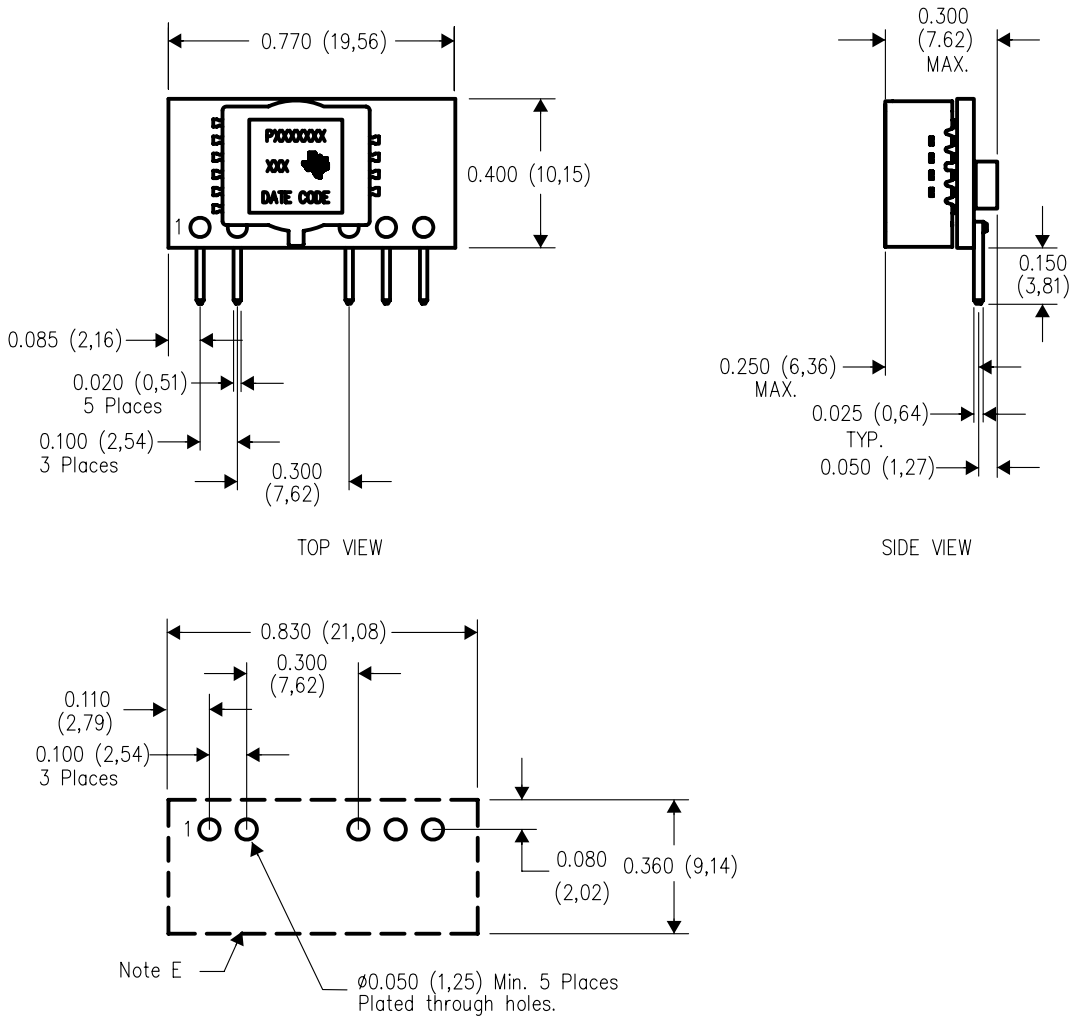




4207975–2/C 08/07

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.020" (0,51) x 0.025" (0,64).
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EDJ (R–PDSS–T5) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.020" (0,51) x 0.025" (0,64).
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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