TEXAS INSTRUMENTS

DAC8881

JAJS261B – JULY 2007 – REVISED JANUARY 2018

DAC8881 16ビット、シングル・チャネル、低ノイズ、電圧出力デジタル/アナログ・コンバータ

1 特長

- 相対精度: ±0.5 LSB
- 動作温度範囲全体で16ビットの単調特性
- 低ノイズ: 24nV/√Hz
- 高速セトリング: 5µs
- レール・ツー・レール動作のオンチップ出力バッファ・アンプ
- 広い電圧範囲の単一電源: +2.7V～+5.5V
- DACローディング制御
- パワーオン・リセットをゼロ・スケールまたは中間スケールに選択可能
- パワーダウン・モード
- ユニポーラのストレート・バイナリまたは2の補数入力モード
- シュミット・トリガ入力付きの高速 SPI™インターフェイス:
  最高50MHz、1.8V/3V/5Vロジック
- 小形のパッケージ: QFN-24、4×4mm

2 アプリケーション

- 産業用プロセス制御
- データ収集システム
- 自動テスト機器
- 通信
- 光学ネットワーク機器

3 概要

DAC8881は16ビット、シングル・チャネル、電圧出力のデジタル/アナログ・コンバータ(DAC)で、低消費電力の動作と柔軟なSPIシリアル・インターフェイスを実現します。また、16ビットの単調性、非常に優れた線形性、短いセトリング時間の特長があります。オンチップの高精度出力アンプにより、2.7V～5.5Vの電源電圧範囲の全体にわたってレール・ツー・レールの出力スイングを実現できます。

デバイスは、標準のSPIシリアル・インターフェイスをサポートし、最高50MHzの入力データ・クロック周波数で動作できます。DAC8881には、DACチャネルの出力範囲を設定するため、外部の基準電圧が必要です。プログラム可能なパワーオン・リセット回路もデバイスに組み込まれており、DAC出力電圧が電源オン時にゼロスケールと中間スケールのどちらかになり、有効な書き込みコマンドが実行されるまでその状態に維持されることを保証します。

さらに、デバイスにはユニポーラのストレート・バイナリ、または2の補数モードで動作する機能があります。DAC8881にはパワーダウン機能があり、PDNピンからアクセス可能で、5V時に消費電流を25µAに減らすことができます。消費電力は5V時に6mWで、パワーダウン・モードでは125µWに低下します。

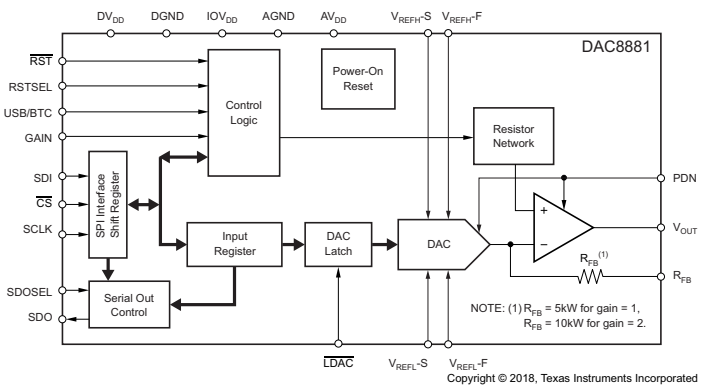
DAC8881は、4×4mmのQFN-24パッケージで供給され、-40℃～+105℃の温度範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DAC8881	VQFN	4.00mm×4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ブロック図



目次

4 改訂履歴

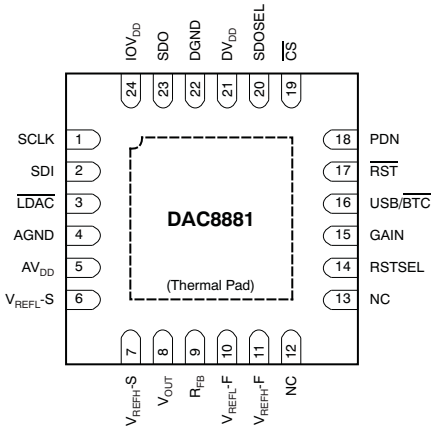
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (September 2007) から Revision B に変更 **Page**

- 「*製品情報*」表、「*ESD定格*」表、「*推奨動作条件*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Changed the text in the *Input Data Format* section ... 28
- Changed Table 3 ... 29

5 Pin Configuration and Functions

RGE Package
QFN-24
(Top View)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SCLK	I	SPI bus serial clock input
2	SDI	I	SPI bus serial data input
3	$\overline{\text{LDAC}}$	I	Load DAC latch control input (active low). When $\overline{\text{LDAC}}$ is low, the DAC latch is transparent, and the contents of the input register are transferred to the DAC latch. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated.
4	AGND	I	Analog ground
5	AV_{DD}	I	Analog power supply
6	V_{REFL}-S	I	Reference low input sense
7	V_{REFH}-S	I	Reference high input sense
8	V_{OUT}	O	Output of output buffer
9	R_{FB}	I	Feedback resistor connected to the inverting input of the output buffer.
10	V_{REFL}-F	I	Reference low input force
11	V_{REFH}-F	I	Reference high input force
12	NC	—	Do not connect.
13	NC	—	Do not connect.
14	RSTSEL	I	Selects the value of the output from the V_{OUT} pin after power-on or hardware reset. If RSTSEL = IOV_{DD}, then register data = 8000h. If RSTSEL = DGND, then register data = 0000h.
15	GAIN	I	Buffer gain setting. Gain = 1 when the pin is connected to DGND; Gain = 2 when the pin is connected to IOV_{DD}.
16	USB/$\overline{\text{BTC}}$	I	Input data format selection. Input data are straight binary format when the pin is connected to IOV_{DD}, and in two's complement format when the pin is connected to DGND.
17	$\overline{\text{RST}}$	I	Reset input (active low). Logic low on this pin causes the device to perform a reset.
18	PDN	I	Power-down input (active high). Logic high on this pin forces the device into power-down status. In power-down, the V_{OUT} pin connects to AGND through 10kΩ resistor.
19	$\overline{\text{CS}}$	I	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, SDO is in high-impedance status.
20	SDOSEL	I	SPI serial data output selection. When SDOSEL is tied to IOV_{DD}, the contents of the existing input register are shifted out from the SDO pin; this is Stand-Alone mode. When SDOSEL is tied to DGND, the contents in the SPI input shift register are shifted out from the SDO pin; this is Daisy-Chain mode for daisy chaining communication.
21	DV_{DD}	I	Digital power supply (connect to AV_{DD}, pin 5)
22	DGND	I	Digital ground
23	SDO	O	SPI bus serial data output. Refer to the *Timing Diagrams* for further detail.
24	IOV_{DD}	I	Interface power. Connect to +1.8V for 1.8V logic, +3V for 3V logic, and to +5V for 5V logic.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AV_{DD} to AGND	–0.3	6	V
DV_{DD} to DGND	–0.3	6	V
IOV_{DD} to DGND	–0.3	6	V
Digital input voltage to DGND	–0.3	IOV_{DD} + 0.3	V
V_{OUT} to AGND	–0.3	AV_{DD} + 0.3	V
Operating temperature range	–40	105	°C
Storage temperature range	–65	150	°C
Storage temperature, T_{stg}		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
AV_{DD}	Analog power supply		2.7		5.5	V
IOV_{DD}	Interface power supply		1.7		AV_{DD}	V
V_{REFH}	Reference high input voltage	AV_{DD} = 5.5 V	1.25	5	AV_{DD}	V
		AV_{DD} = 3 V	1.25	2.5	AV_{DD}	V
V_{REFL}	Reference low input voltage		–0.2	0	0.2	V
	Specified performance		–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		DAC8881 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD}$ = +2.7 V to +5.5 V, IOV_{DD} = +1.8 V to +5.5 V, gain = 1X mode, unless otherwise noted.

PARAMETER	CONDITIONS		DAC8881			UNIT
			MIN	TYP	MAX	
ACCURACY						
Linearity error	Measured by line passing through codes 0200h and FE00h			±0.5	±1	LSB
Differential linearity error	Measured by line passing through codes 0200h and FE00h			±0.25	±1	LSB
Monotonicity			16			Bits
Zero-scale error	T_A = +25°C, code = 0200h				±4	LSB
	T_{MIN} to T_{MAX}, code = 0200h				±8	LSB
Zero-scale drift	Code = 0200h			±0.5	±1	ppm/°C of FSR
Gain error	T_A = +25°C, Measured by line passing through codes 0200h and FE00h			±4	±8	LSB
Gain temperature drift	Measured by line passing through codes 0200h and FE00h			±0.5	±1	ppm/°C
PSRR	V_{OUT} = full-scale, AV_{DD} = +5 V ±10%				2	LSB/V
ANALOG OUTPUT(1)						
Voltage output(2)			0		AV_{DD}	V
Output voltage drift vs time	Device operating for 500 hours			5		ppm of FSR
	Device operating for 1000 hours			8		ppm of FSR
Output current				2.5		mA
Maximum load capacitance				200		pF
Short-circuit current				+31, –50		mA
REFERENCE INPUT(1)						
V_{REFH} input voltage range	AV_{DD} = +5.5 V		1.25	5.0	AV_{DD}	V
	AV_{DD} = +3 V		1.25	2.5	AV_{DD}	V
V_{REFH} input capacitance				5		pF
V_{REFH} input impedance				4.5		kΩ
V_{REFL} input voltage range			–0.2	0	+0.2	V
V_{REFL} input capacitance				4.5		pF
V_{REFL} input impedance				5		kΩ
DYNAMIC PERFORMANCE(1)						
Settling time	To ±0.003% FS, R_L = 10 kΩ, C_L = 50 pF, code 1000h to F000h			5		µs
Slew rate	From 10% to 90% of 0 V to +5 V			2.5		V/µs
Code change glitch	Code = 7FFFh to 8000h to 7FFFh	V_{REFH} = 5 V, gain = 1X mode		37		nV-s
		V_{REFH} = 2.5 V, gain = 1X mode		18		nV-s
		V_{REFH} = 1.25 V, gain = 1X mode		9		nV-s
		V_{REFH} = 2.5 V, gain = 2X mode		21		nV-s
		V_{REFH} = 1.25 V, gain = 2X mode		10		nV-s
Digital feedthrough				1		nV-s
Output noise voltage density	f = 1 kHz to 100 kHz, full-scale output	Gain = 1		24	30	nV/√Hz
		Gain = 2		40	48	nV/√Hz
Output noise voltage	f = 0.1Hz to 10Hz, full-scale output			2		μV_{PP}

(1) Specified by design. Not production tested.
(2) The output from the V_{OUT} pin = $[(V_{REFH} - V_{REFL})/65536] \times CODE \times$ Buffer GAIN + V_{REFL}. The maximum range of V_{OUT} is 0 V to AV_{DD}. The full-scale of the output must be less than AV_{DD}; otherwise, output saturation occurs.

Electrical Characteristics (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD}$ = +2.7 V to +5.5 V, IOV_{DD} = +1.8 V to +5.5 V, gain = 1X mode, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8881			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS(1)					
High-level input voltage, V_{IH}	IOV_{DD} = 4.5 V to 5.5 V	3.8		IOV_{DD} + 0.3	V
	IOV_{DD} = 2.7 V to 3.3 V	2.1		IOV_{DD} + 0.3	V
	IOV_{DD} = 1.7 V to 2 V	1.5		IOV_{DD} + 0.3	V
Low-level input voltage, V_{IL}	IOV_{DD} = 4.5 V to 5.5 V	–0.3		0.8	V
	IOV_{DD} = 2.7 V to 3.3 V	–0.3		0.6	V
	IOV_{DD} = 1.7 V to 2 V	–0.3		0.3	V
Digital input current (I_{IN})			±1	±10	µA
Digital input capacitance			5		pF
DIGITAL OUTPUT(1)					
High-level output voltage, V_{OH}	IOV_{DD} = 2.7 V to 5.5 V, I_{OH} = –1 mA	IOV_{DD} – 0.2			V
	IOV_{DD} = 1.7 V to 2 V, I_{OH} = –500 µA	IOV_{DD} – 0.2			V
Low-level output voltage, V_{OL}	IOV_{DD} = 2.7 V to 5.5 V, I_{OL} = 1 mA			0.2	V
	IOV_{DD} = 1.7 V to 2 V, I_{OL} = 500 µA			0.2	V
POWER SUPPLY					
AV_{DD}		+2.7		+5.5	V
DV_{DD}		+2.7		+5.5	V
IOV_{DD}		+1.7		DV_{DD}	V
AI_{DD}	$V_{IH} = IOV_{DD}$, V_{IL} = DGND			1.5	mA
DI_{DD}	$V_{IH} = IOV_{DD}$, V_{IL} = DGND		1	10	µA
IOI_{DD}	$V_{IH} = IOV_{DD}$, V_{IL} = DGND		1	10	µA
AI_{DD} power-down	PDN = IOV_{DD}		25	50	µA
Power dissipation	$AV_{DD} = DV_{DD}$ = 5.0V		6	7.5	mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

6.6 Timing Characteristics for Figure 1 (1) (2) (3)

At –40°C to +105°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Maximum clock frequency	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		40	MHz
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		50	MHz
t_1	Minumum $\overline{CS}$ high time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	30		ns
t_2	$\overline{CS}$ falling edge to SCLK rising edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
t_3	SCLK falling edge to $\overline{CS}$ falling edge setup time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_4	SCLK low time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_5	SCLK high time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_6	SCLK cycle time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_7	SCLK rising edge to $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6$V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_8	Input data setup time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_9	Input data hold time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{14}	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{15}	$\overline{LDAC}$ pulse width	$2.7 \le DV_{DD} < 3.6$V, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns

(1) All input signals are specified with $t_R = t_F$ = 2ns (10% to 90% of IOV_{DD}) and timed from a voltage level of $IOV_{DD}/2$.
(2) Specified by design. Not production tested.
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

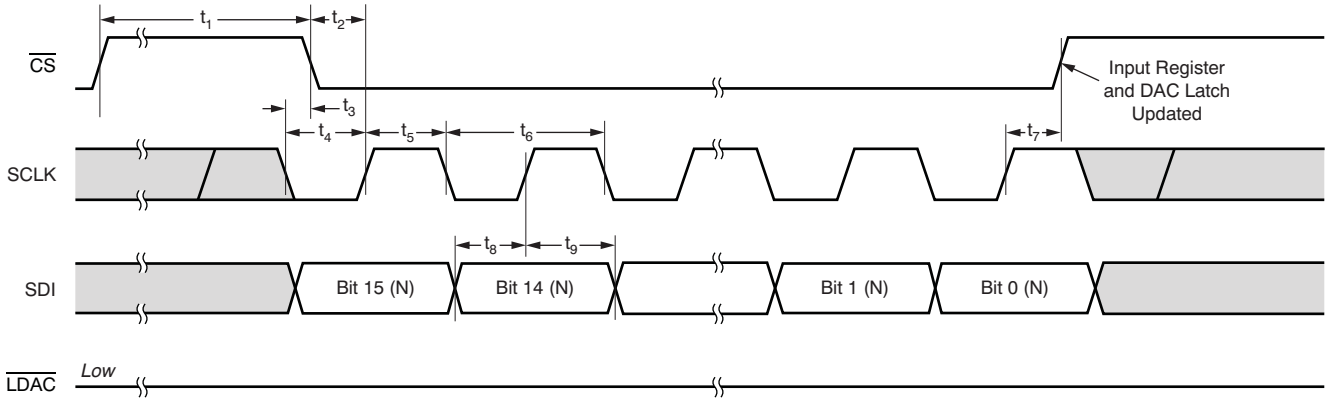
6.7 Timing Characteristics for Figure 2 and Figure 3 (1) (2) (3)

At –40°C to +105°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Maximum clock frequency	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		20	MHz
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		25	MHz
t_1	Minumum $\overline{CS}$ high time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	30		ns
t_2	$\overline{CS}$ falling edge to SCLK rising edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
t_3	SCLK falling edge to $\overline{CS}$ falling edge setup time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_4	SCLK low time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_5	SCLK high time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_6	SCLK cycle time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	40		ns
t_7	SCLK rising edge to $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_8	Input data setup time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_9	Input data hold time	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{10}	SDO active from $\overline{CS}$ falling edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		15	ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		10	ns
t_{11}	SDO data valid from SCLK falling edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		20	ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		15	ns
t_{12}	SDO data hold from SCLK rising edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_{13}	SDO High-Z from $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		8	ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$		5	ns
t_{14}	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{15}	$\overline{LDAC}$ pulse width	$2.7 \le DV_{DD} < 3.6$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5$ V, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns

(1) All input signals are specified with $t_R = t_F = 2$ns (10% to 90% of IOV_{DD}) and timed from a voltage level of $IOV_{DD}/2$.
(2) Specified by design. Not production tested.
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

Case 1: Standalone operation without SDO, $\overline{\text{LDAC}}$ tied low.



Case 2: Standalone operation without SDO, $\overline{\text{LDAC}}$ active.

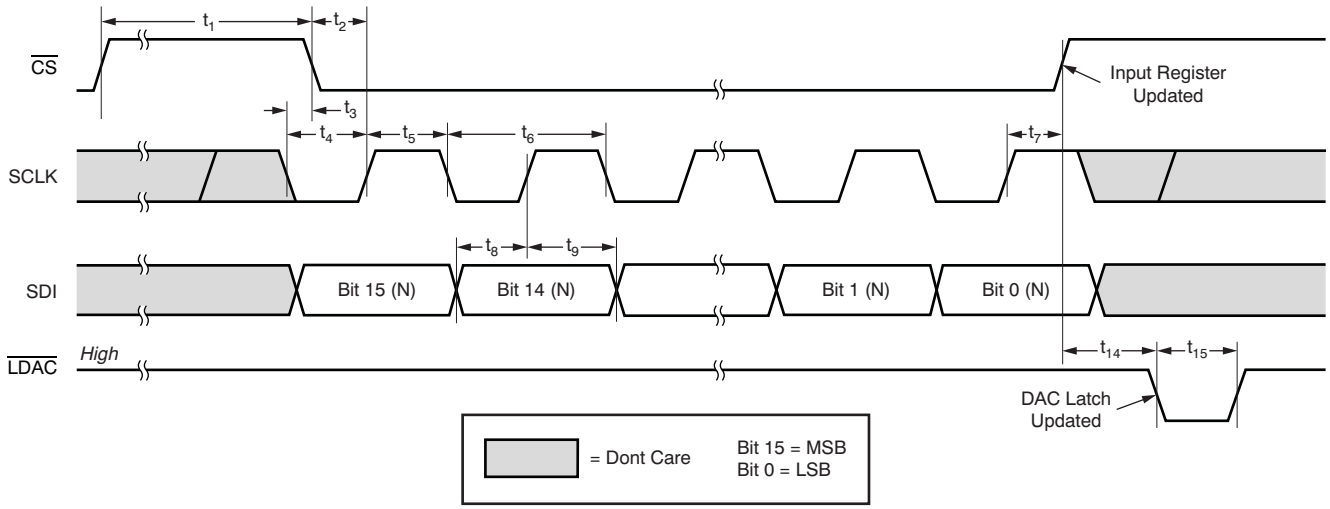
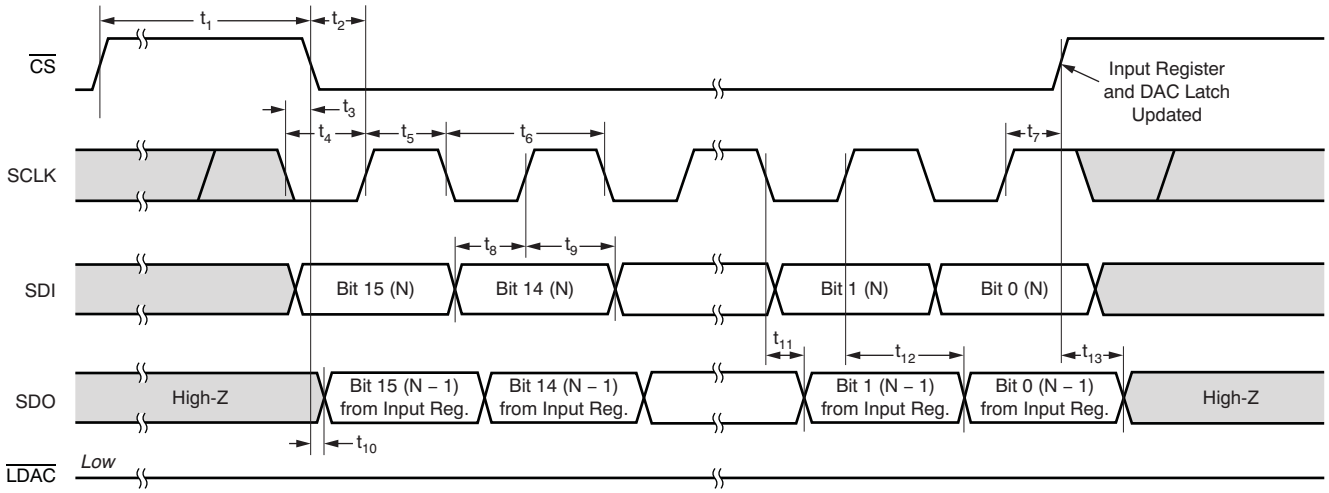


Figure 1. Timing Diagram of Standalone Operation Without SDO

Case 1: Standalone operation with output from SDO, $\overline{\text{LDAC}}$ tied low.



Case 2: Standalone operation with output from SDO, $\overline{\text{LDAC}}$ active.

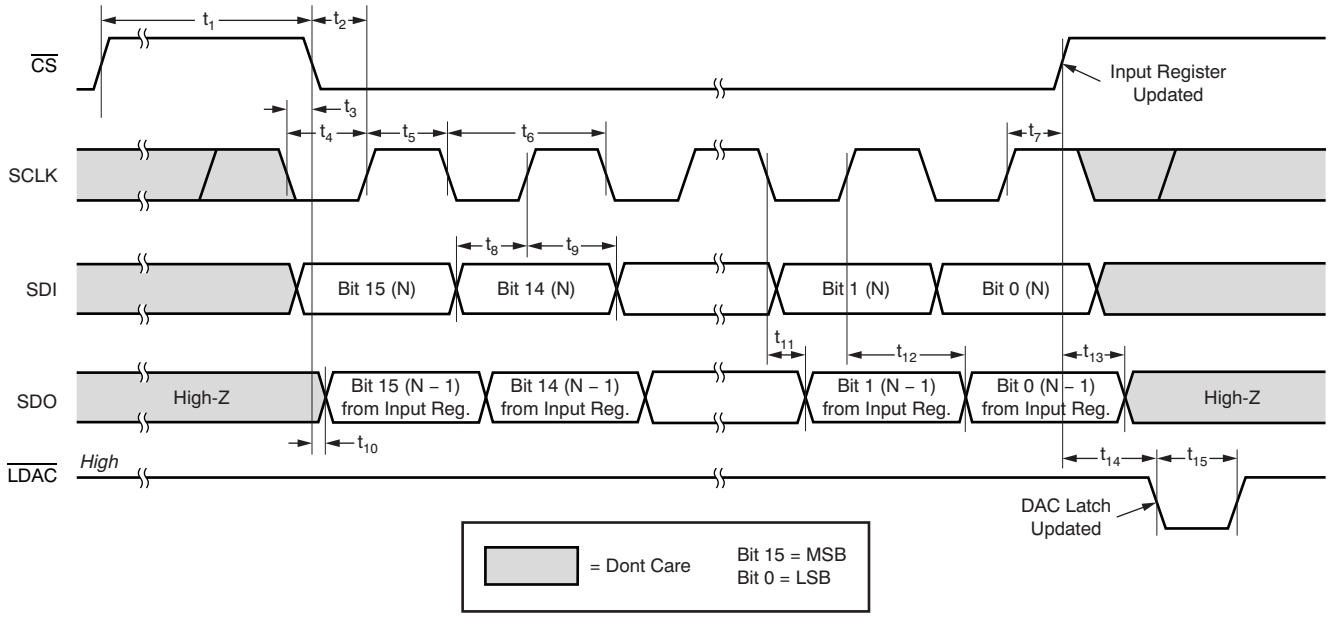
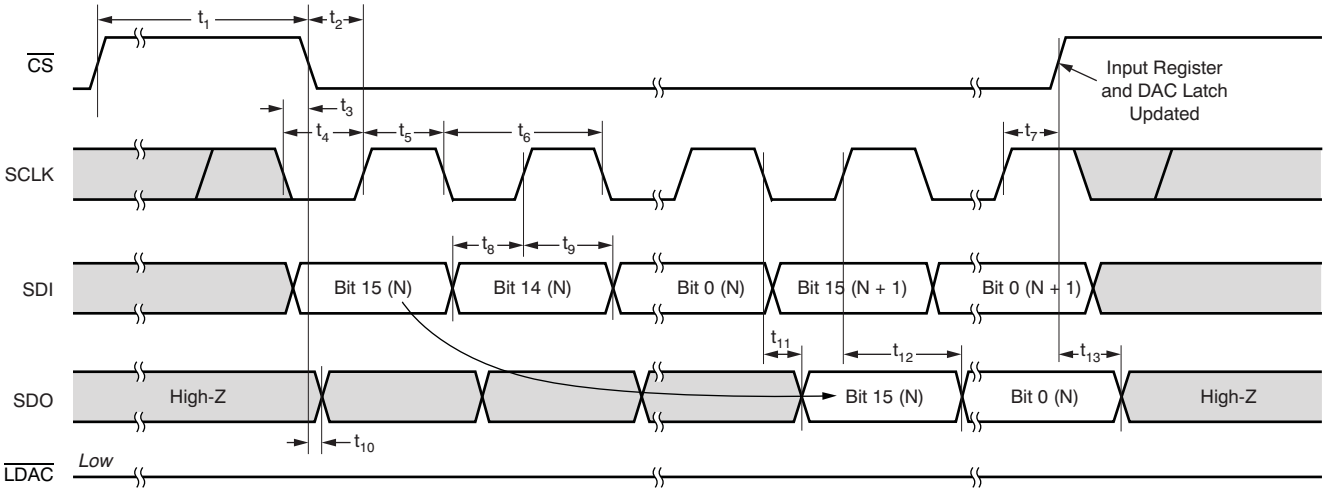


Figure 2. Timing Diagram of Standalone Operation With SDO

Case 1: Daisy Chain, $\overline{\text{LDAC}}$ tied low.



Case 2: Daisy Chain, $\overline{\text{LDAC}}$ active.

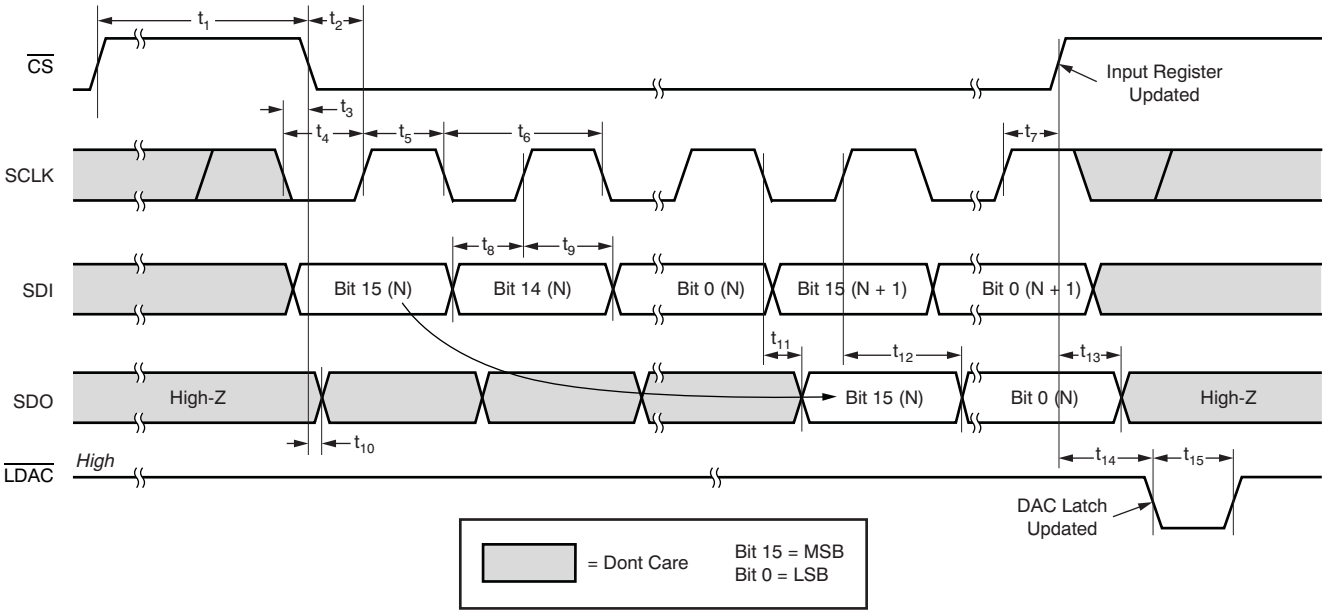


Figure 3. Timing Diagram of Daisy Chain Mode, Two Cascaded Devices

6.8 Typical Characteristics: V_{DD} = +5 V

At T_A = +25°C, V_{REFH} = +5 V, V_{REFL} = 0 V, and Gain = 1X Mode, unless otherwise noted.

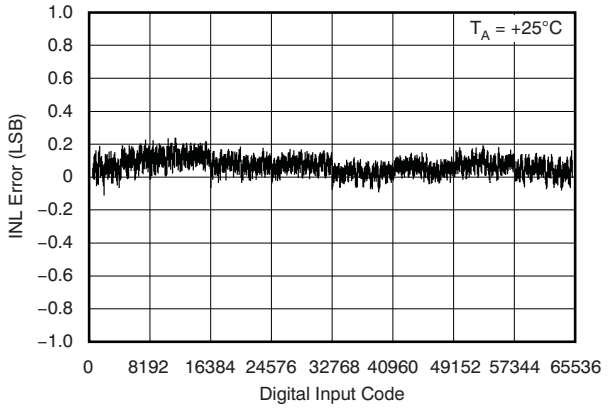


Figure 4. Linearity Error vs Digital Input Code

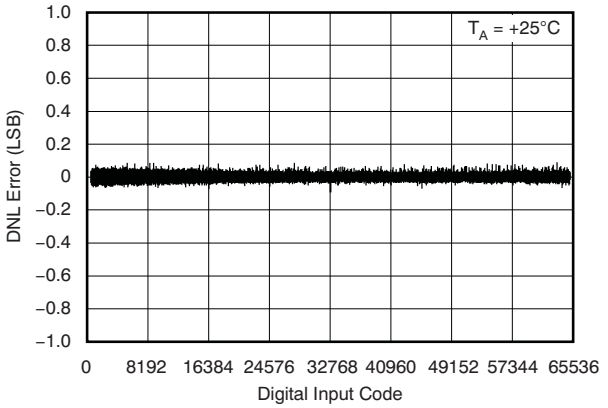


Figure 5. Differential Linearity Error vs Digital Input Code

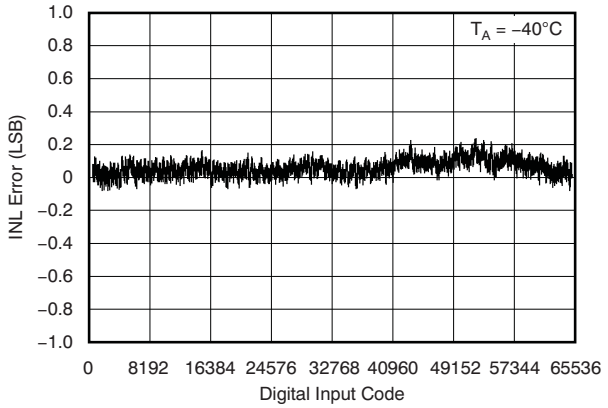


Figure 6. Linearity Error vs Digital Input Code

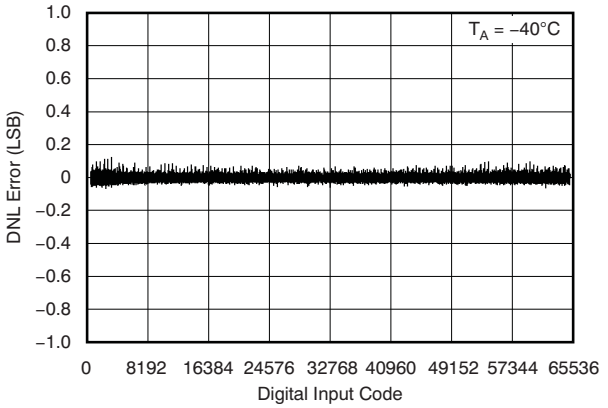


Figure 7. Differential Linearity Error vs Digital Input Code

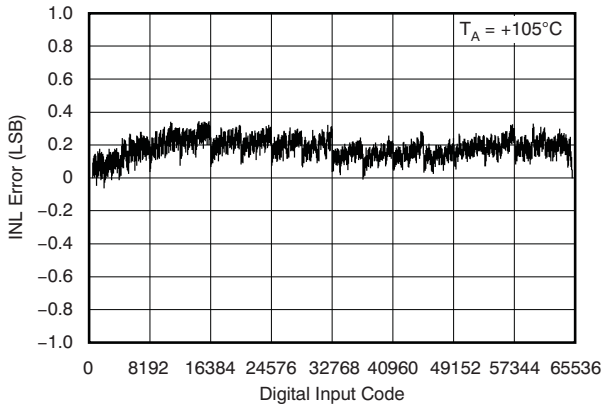


Figure 8. Linearity Error vs Digital Input Code

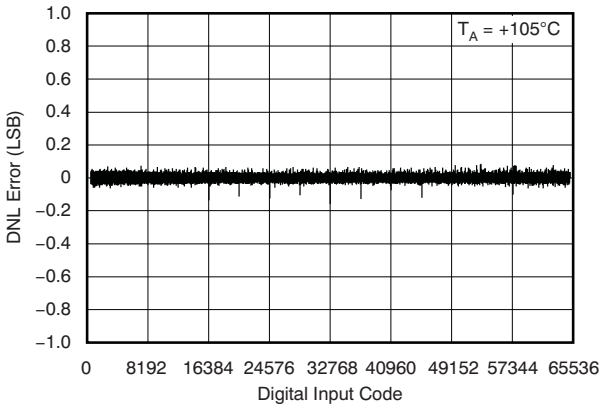


Figure 9. Differential Lineary Error vs Digital Input Code

Typical Characteristics: V_{DD} = +5 V (continued)

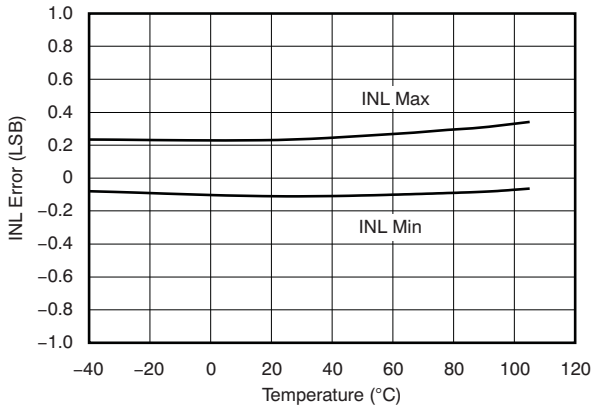


Figure 10. Linearity Error vs Temperature

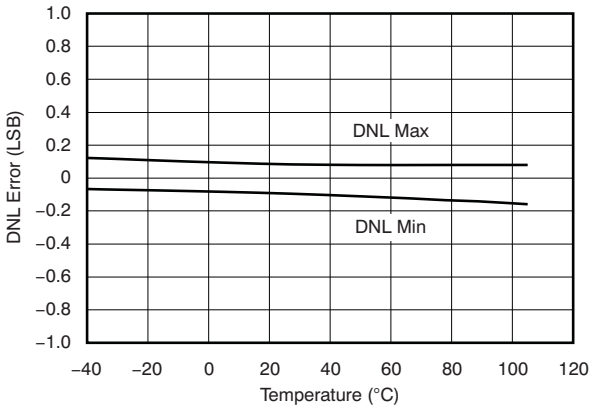


Figure 11. Differential Linearity Error vs Temperature

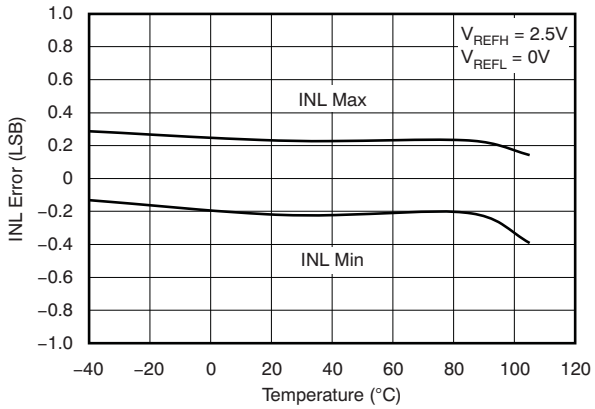


Figure 12. Linearity Error vs Temperature (Gain = 2X Mode)

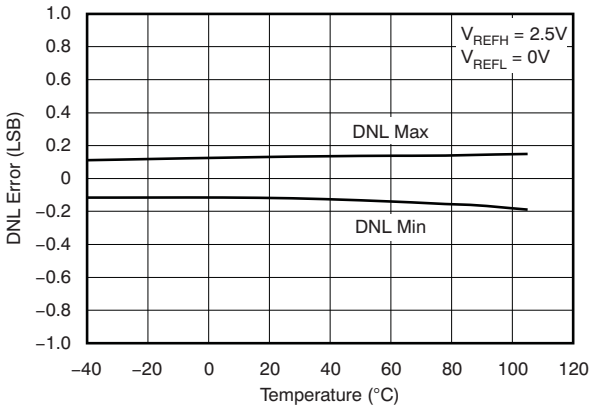


Figure 13. Differential Linearity Error vs Temperature (Gain = 2X Mode)

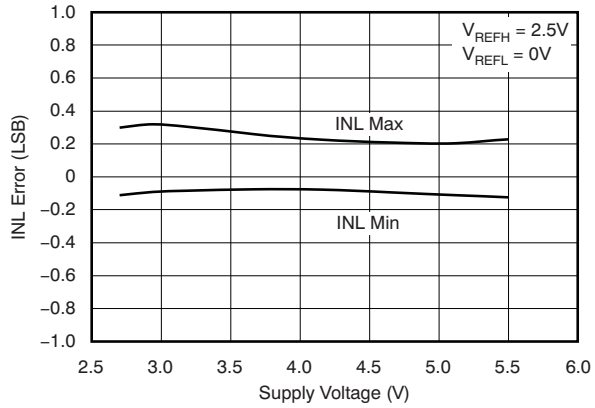


Figure 14. Linearity Error vs Supply Voltage

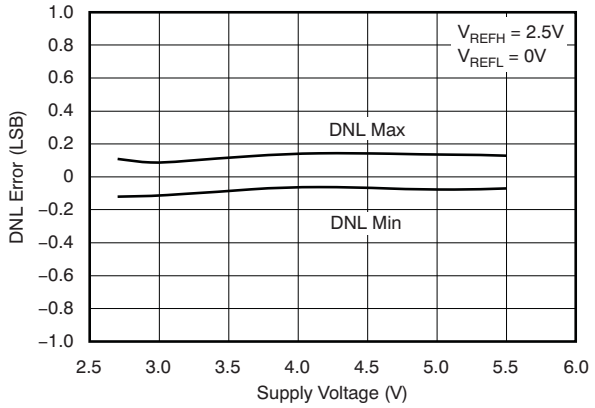


Figure 15. Differential Linearity Error vs Supply Voltage

Typical Characteristics: V_{DD} = +5 V (continued)

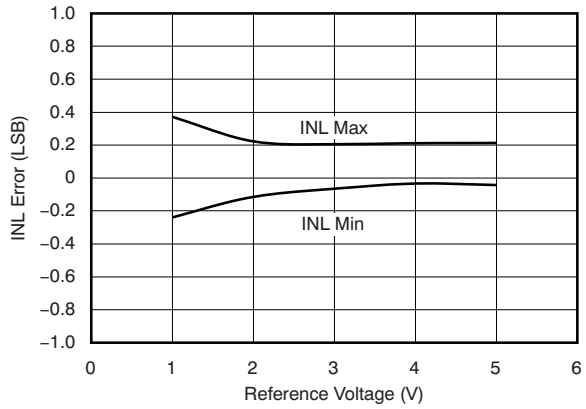


Figure 16. Linearity Error vs Reference Voltage

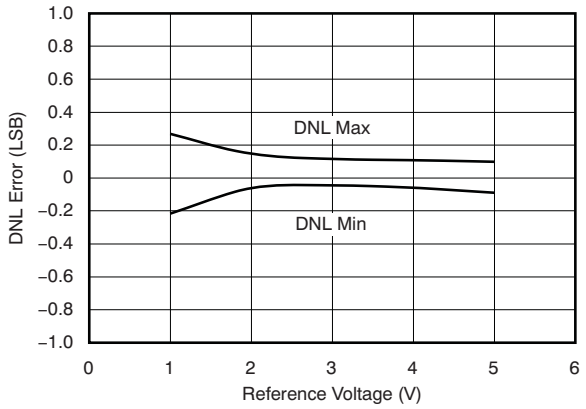


Figure 17. Differential Linearity Error vs Reference Voltage

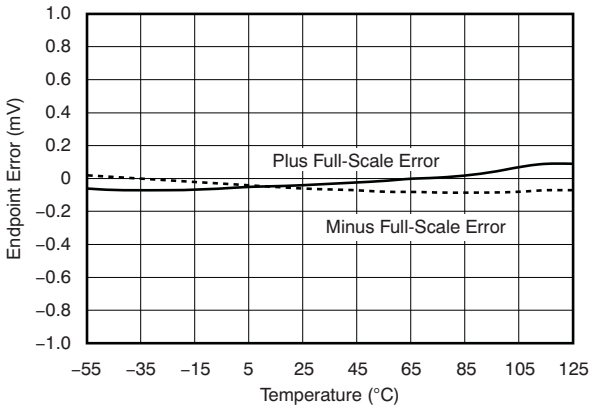


Figure 18. Endpoint Error vs Temperature

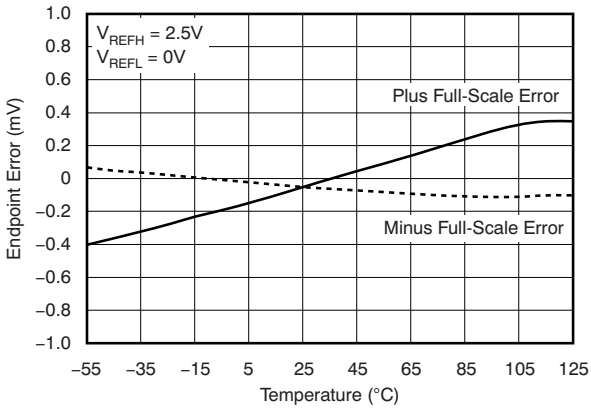


Figure 19. Endpoint Error vs Temperature (Gain = 2X Mode)

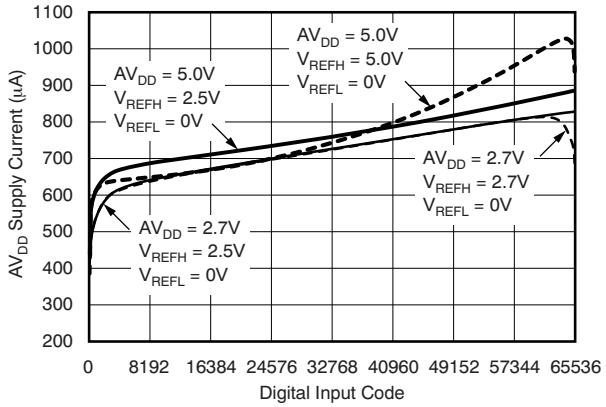


Figure 20. AV_{DD} Supply Current vs Digital Input Code

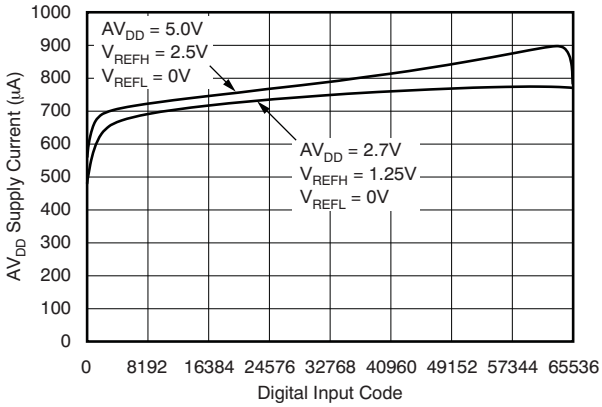


Figure 21. AV_{DD} Supply Current vs Digital Input Code (Gain = 2X Mode)

Typical Characteristics: V_{DD} = +5 V (continued)

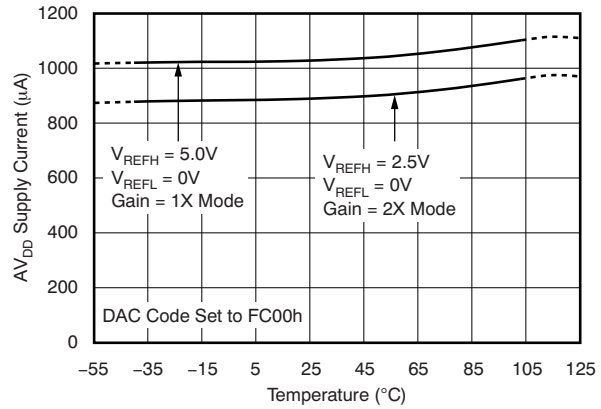


Figure 22. AV_{DD} Supply Current vs Temperature

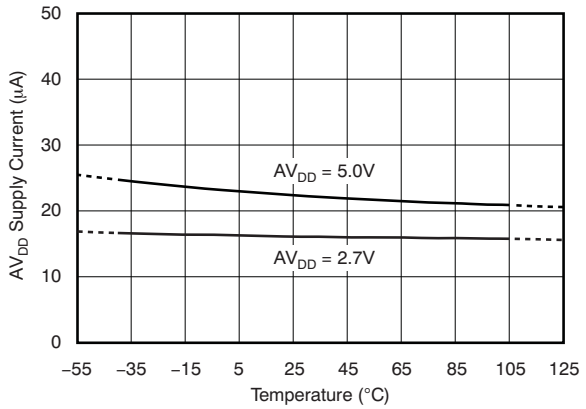


Figure 23. AV_{DD} Power-Down Current vs Temperature

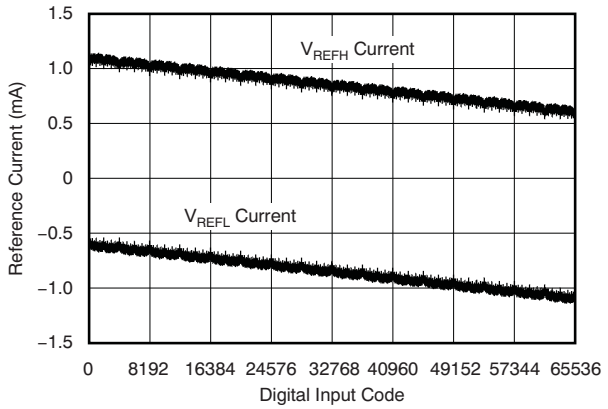


Figure 24. Reference Current vs Digital Input Code

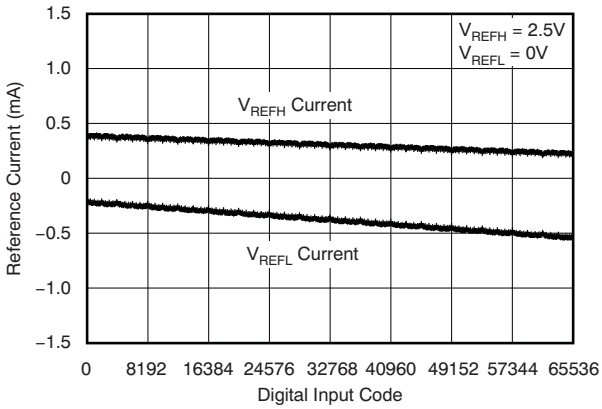


Figure 25. Reference Current vs Digital Input Code (Gain = 2X Mode)

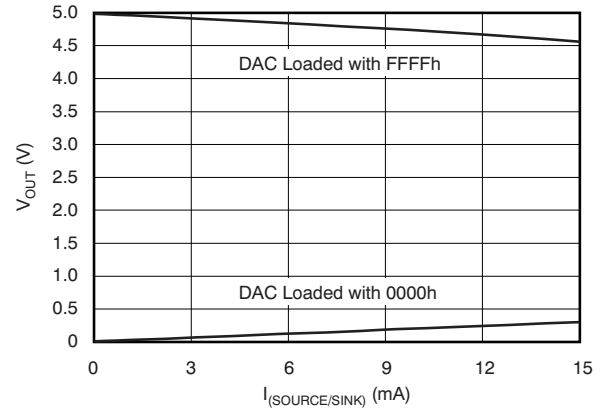


Figure 26. Output Voltage vs Drive Current Capability

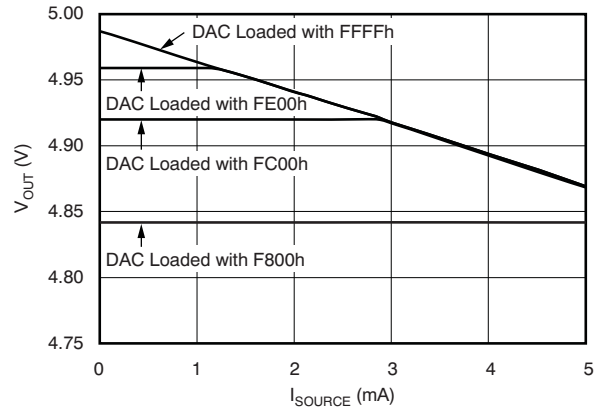


Figure 27. Output Voltage vs Drive Current Capability (Operation Near AV_{DD} Rail)

Typical Characteristics: V_{DD} = +5 V (continued)

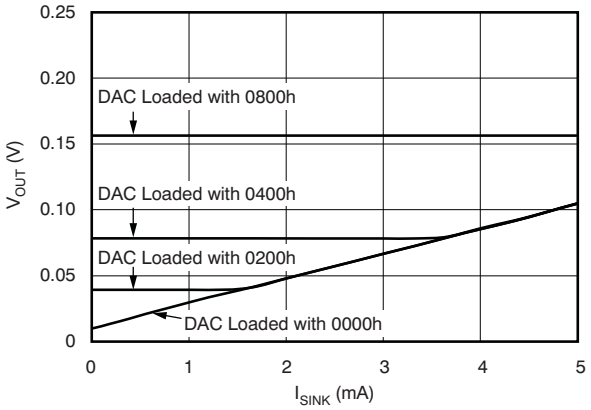


Figure 28. Output Voltage vs Drive Current Capability (Operation Near AGND Rail)

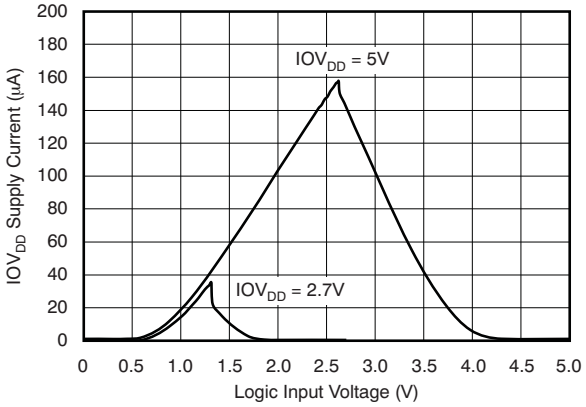


Figure 29. IOV_{DD} Supply Current vs Logic Input Voltage

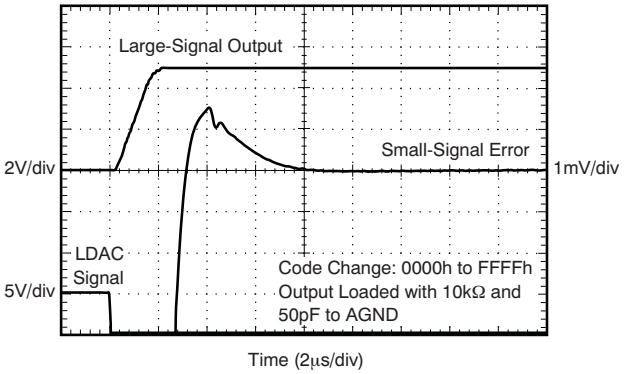


Figure 30. Large Signal Settling Time

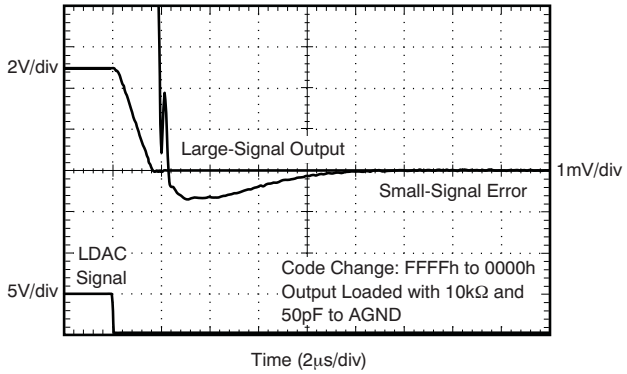


Figure 31. Large Signal Settling Time

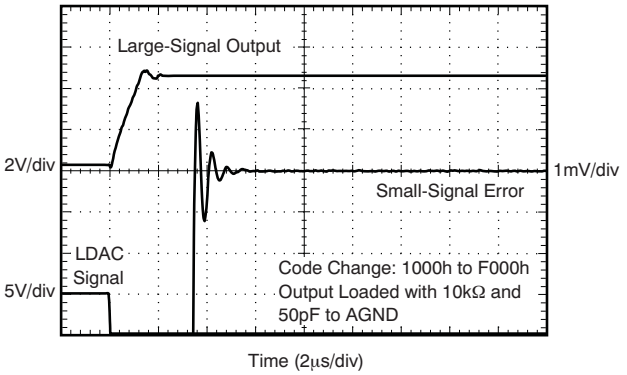


Figure 32. Large Signal Settling Time

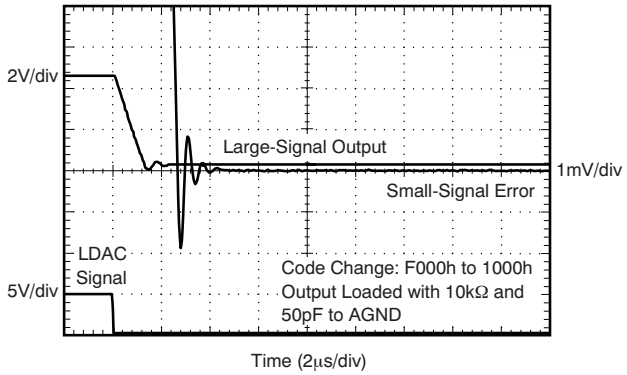


Figure 33. Large Signal Settling Time

Typical Characteristics: V_{DD} = +5 V (continued)

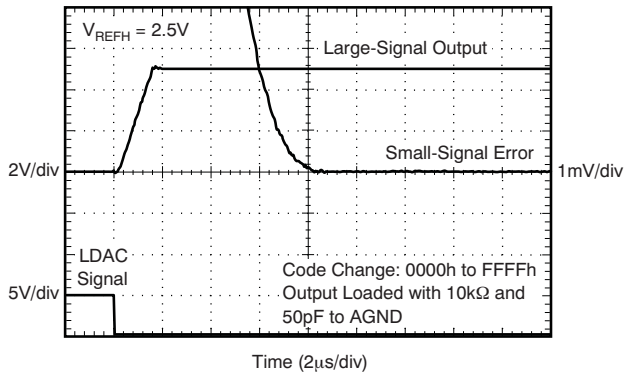


Figure 34. Large Signal Settling Time (Gain = 2X Mode)

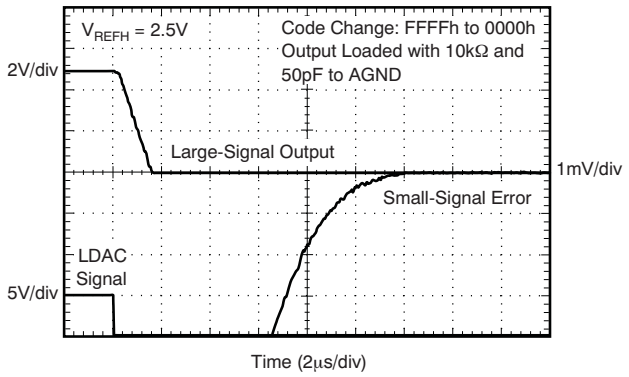


Figure 35. Large Signal Settling Time (Gain = 2X MI)

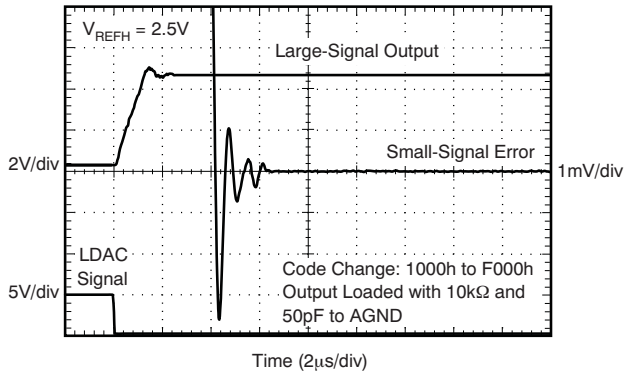


Figure 36. Large Signal Settling Time (Gain = 2X Mode)

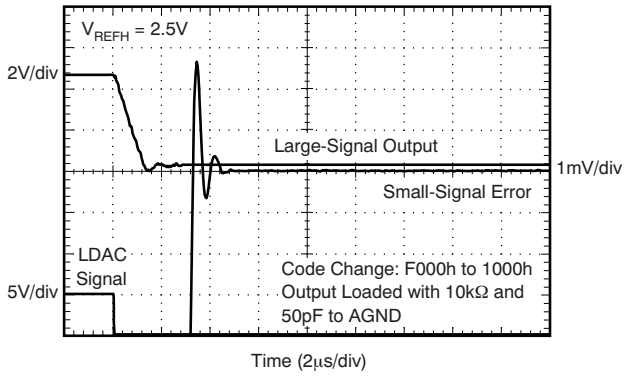


Figure 37. Large Signal Settling Time (Gain = 2X Mode)

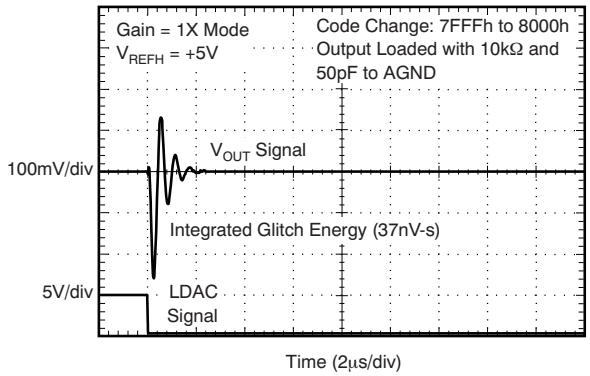


Figure 38. Major Carry Glitch

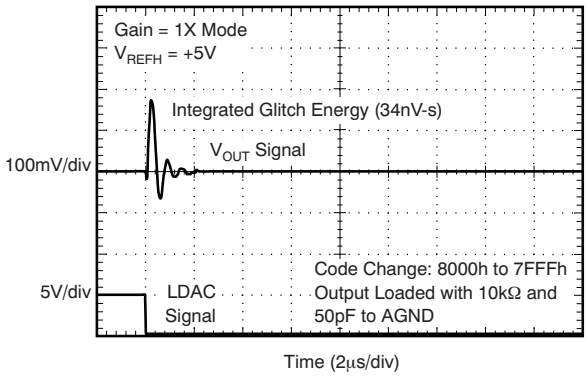


Figure 39. Major Carry Glitch

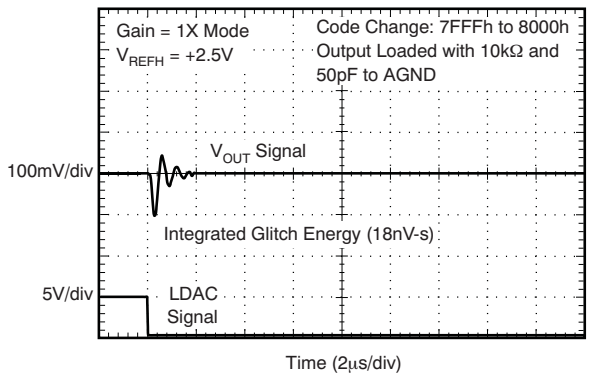


Figure 40. Major Carry Glitch

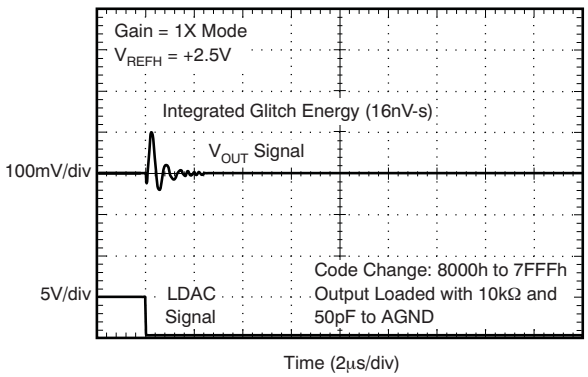


Figure 41. Major Carry Glitch

Typical Characteristics: V_{DD} = +5 V (continued)

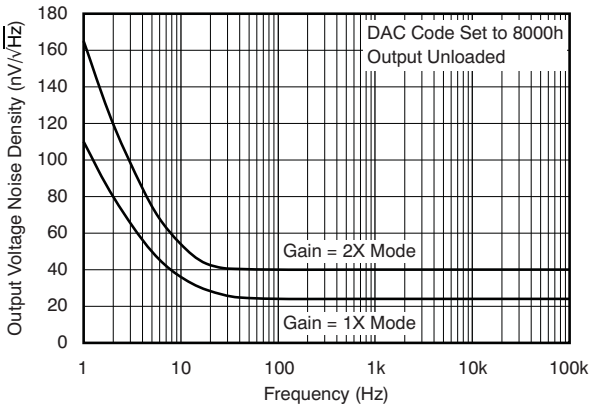


Figure 42. Output Noise Density vs Frequency

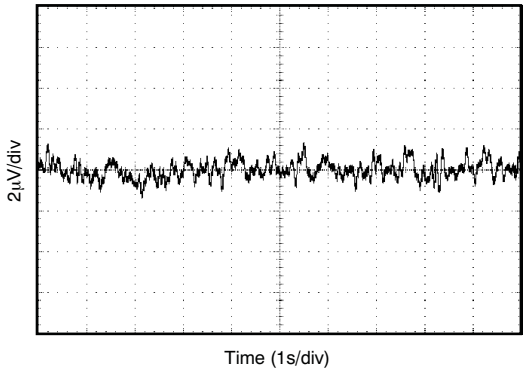


Figure 43. Low-Frequency Output Noise (0.1Hz to 10Hz)

6.9 TYpical Characteristics: V_{DD} = +2.7 V

At T_A = +25°C, V_{REFH} = +2.5 V, V_{REFL} = 0 V, and Gain = 1X Mode, unless otherwise noted.

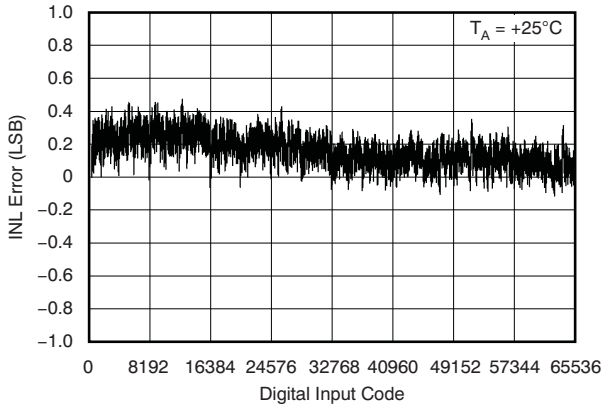


Figure 44. Linearity Error vs Digital Input Code

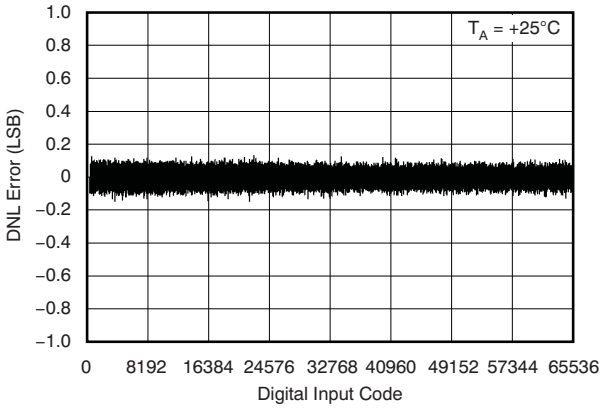


Figure 45. Differential Linearity Error vs Digital Input Code

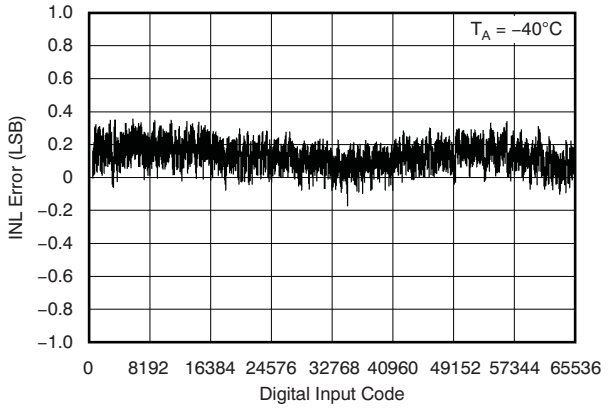


Figure 46. Linearity Error vs Digital Input Code

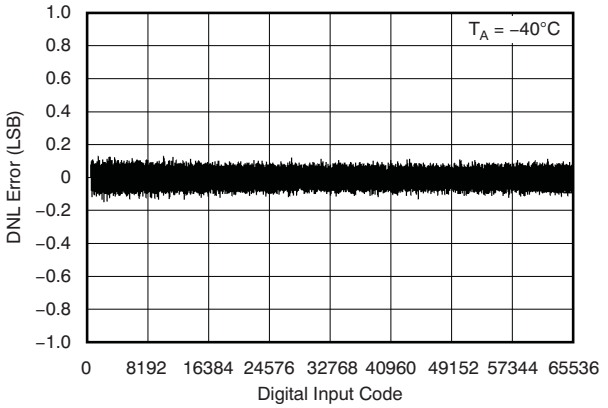


Figure 47. Differential Linearity Error vs Digital Input Code

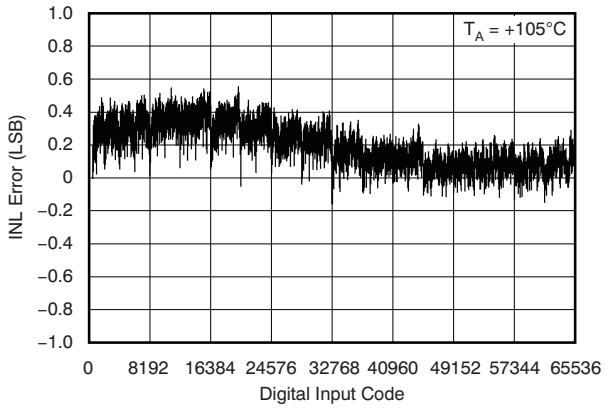


Figure 48. Linearity Error vs Digital Input Code

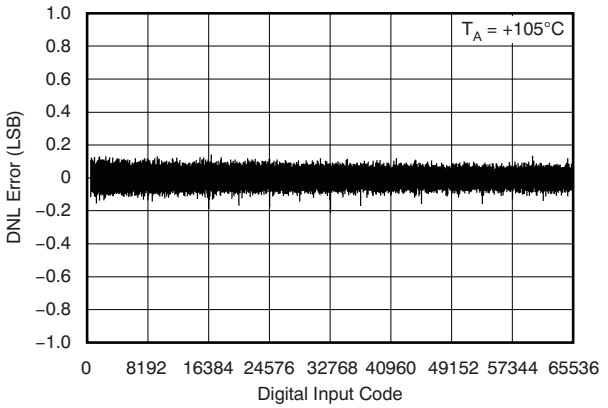


Figure 49. Differential Linearity Error vs Digital Input Code

TYpical Characteristics: V_{DD} = +2.7 V (continued)

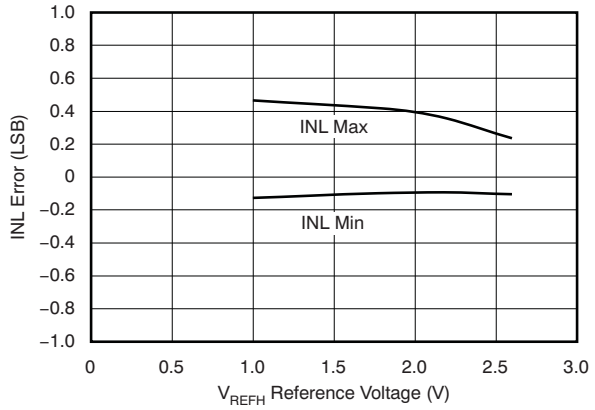


Figure 50. Linearity Error vs

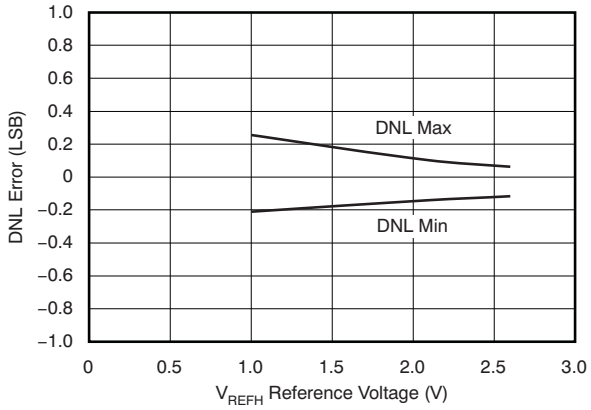


Figure 51. Differential Linearity Error vs Reference Voltage

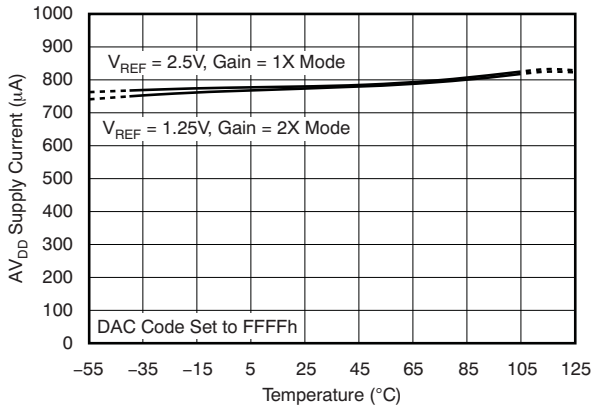


Figure 52. AV_{DD} Supply Current vs Temperature

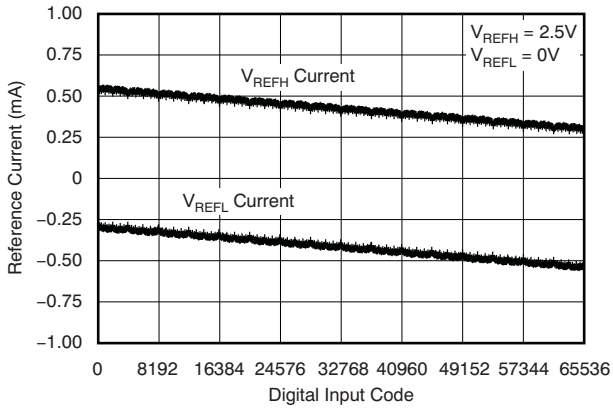


Figure 53. Reference Current vs Digital Input Code

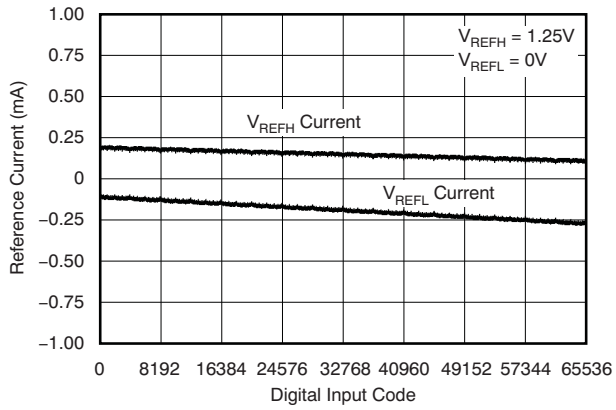


Figure 54. Reference Current vs Digital Input Code (Gain = 2X Mode)

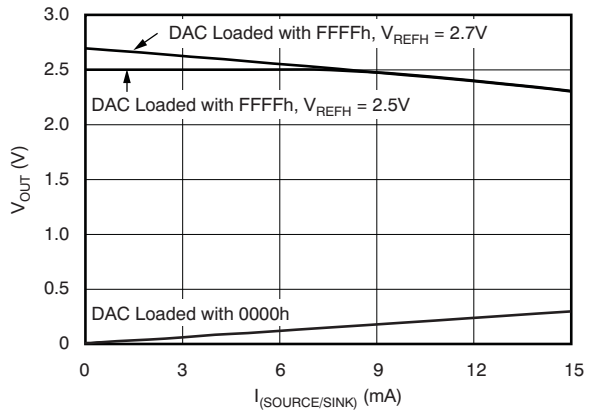


Figure 55. Output Voltage vs Drive Current Capability

TYpical Characteristics: V_{DD} = +2.7 V (continued)

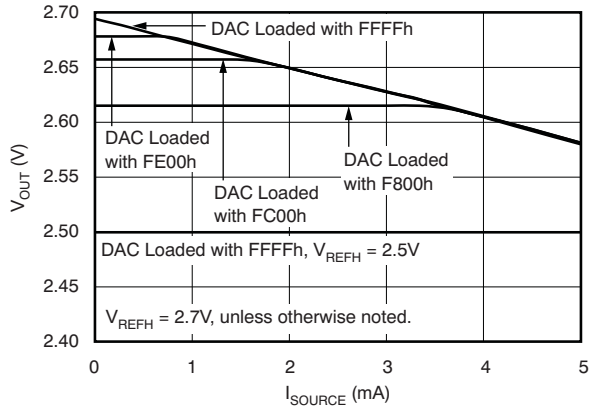


Figure 56. Output Voltage vs Drive Current Capability (Operation Near AV_{DD} Rail)

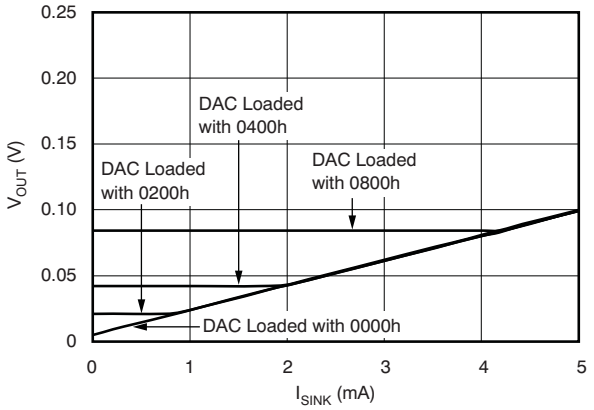


Figure 57. Output Voltage vs Drive Current Capability (Operation Near AGND Rail)

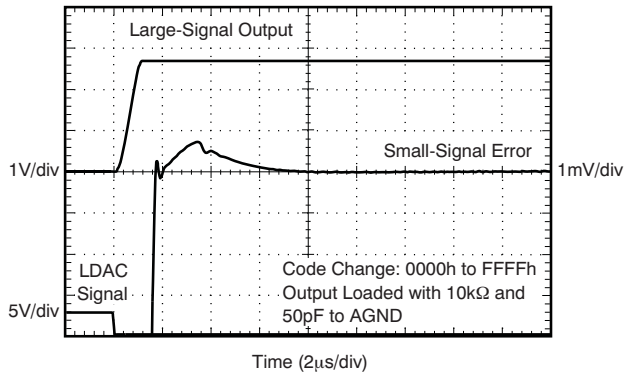


Figure 58. Large Signal Settling Time

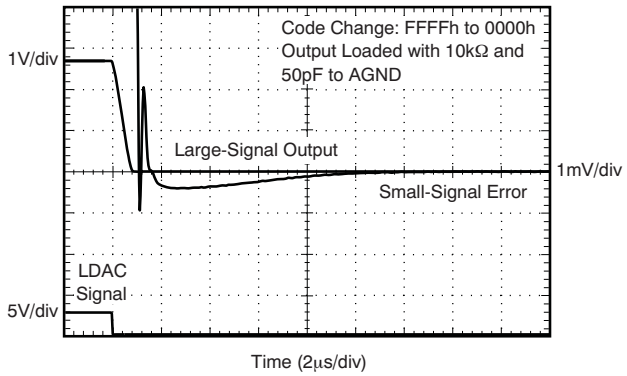


Figure 59. Large Signal Settling Time

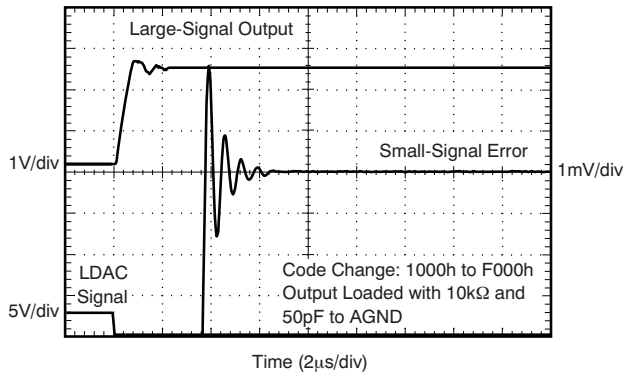


Figure 60. Large Signal Settling Time

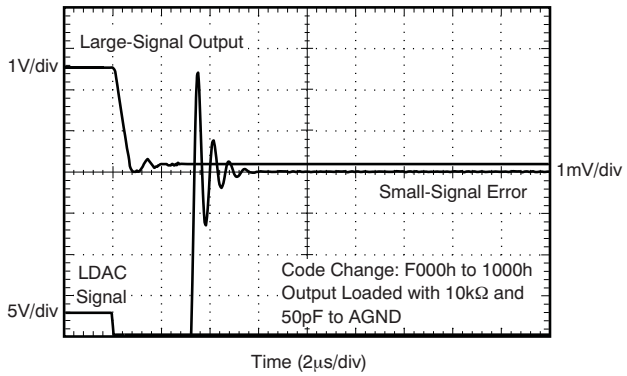


Figure 61. Large Signal Settling Time

TYpical Characteristics: V_{DD} = +2.7 V (continued)

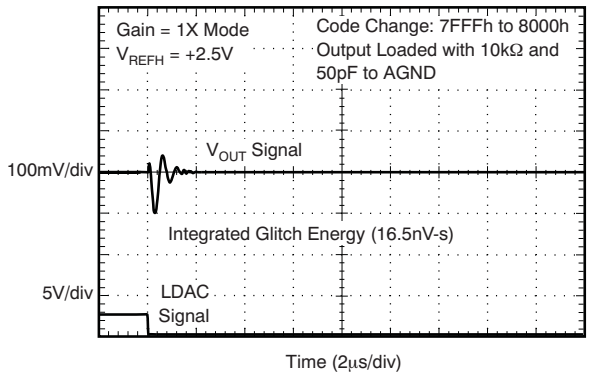


Figure 62. Major Carry Glitch

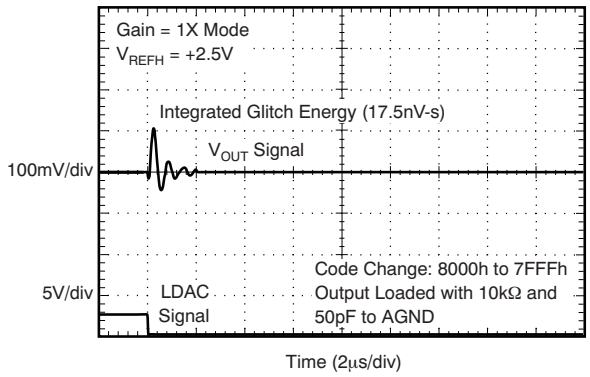


Figure 63. Major Carry Glitch

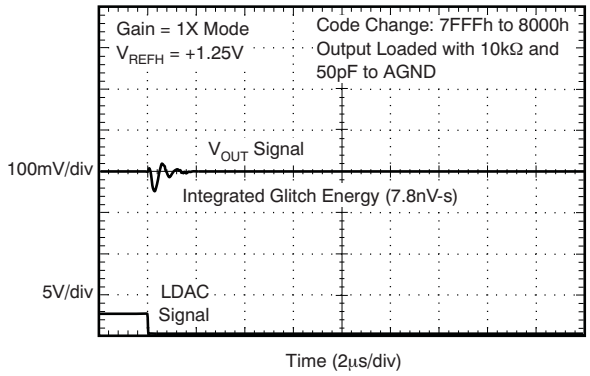


Figure 64. Major Carry Glitch

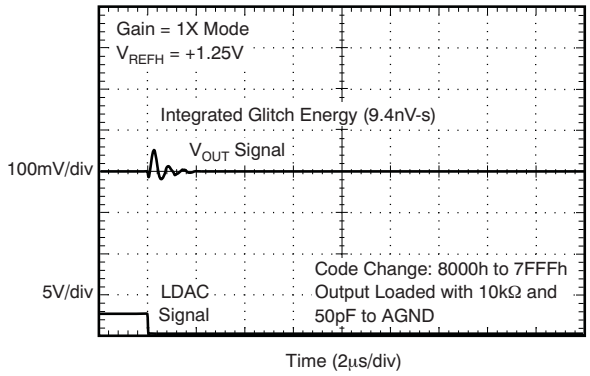


Figure 65. Major Carry Glitch

7 Detailed Description

7.1 Overview

The DAC8881 is a single-channel, 16-bit, serial-input, voltage-output digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the four MSBs segmented, followed by an operational amplifier that serves as a buffer, as shown in Figure 66. The on-chip output buffer allows rail-to-rail output swings while providing a low output impedance to drive loads. The DAC8881 operates from a single analog power supply that ranges from 2.7 V to 5.5 V, and typically consumes 850 μA when operating with a 3-V supply. Data are written to the device in a 16-bit word format, via an SPI serial interface. To enable compatibility with 1.8 V, 3 V, or 5 V logic families, an IOV_{DD} supply pin is provided. This pin allows the DAC8881 input and output logic to be powered from the same logic supply used to interface signals to and from the device. Internal voltage translators are included in the DAC8881 to interface digital signals to the device core. Separate AV_{DD} and DV_{DD} supply pins are provided, but should be connected together. See Figure 67 for the basic configuration of the DAC8881.

To ensure a known power-up state, the DAC8881 is designed with a power-on reset function. Upon power-up, the DAC8881 is reset to either zero-scale or midscale depending on the state of the RSTSEL pin. The device can also be hardware reset by using the $\overline{RST}$ and RSTSEL pins.

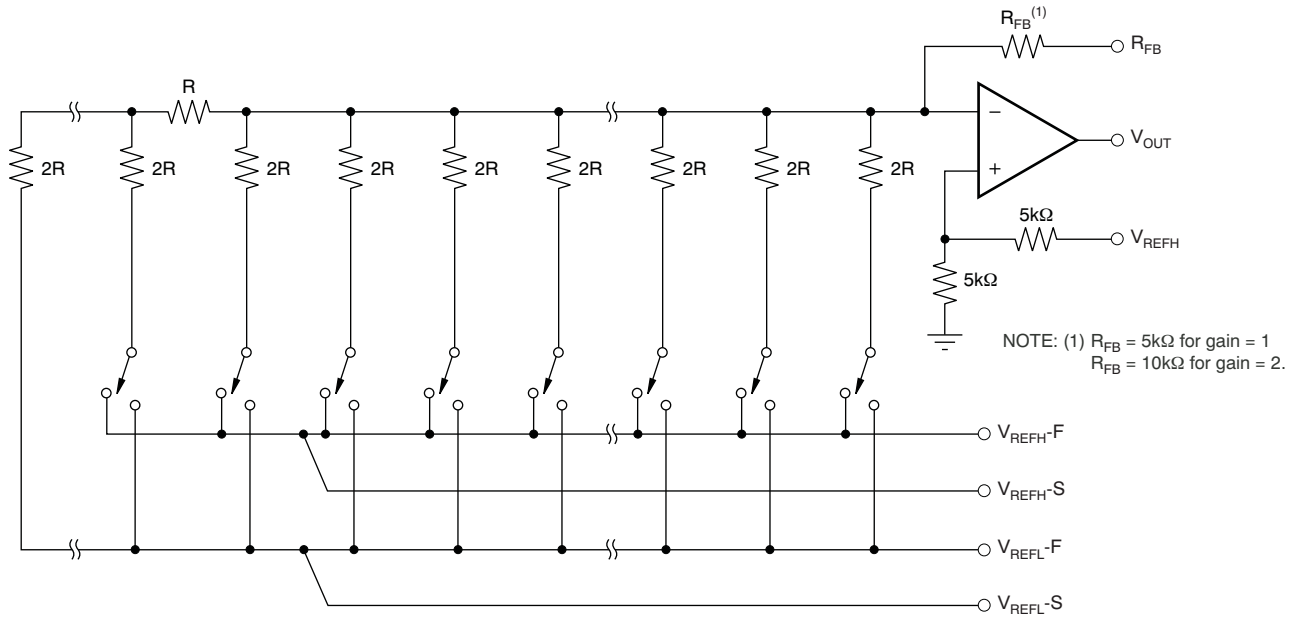


Figure 66. DAC8881 Architecture

Overview (continued)

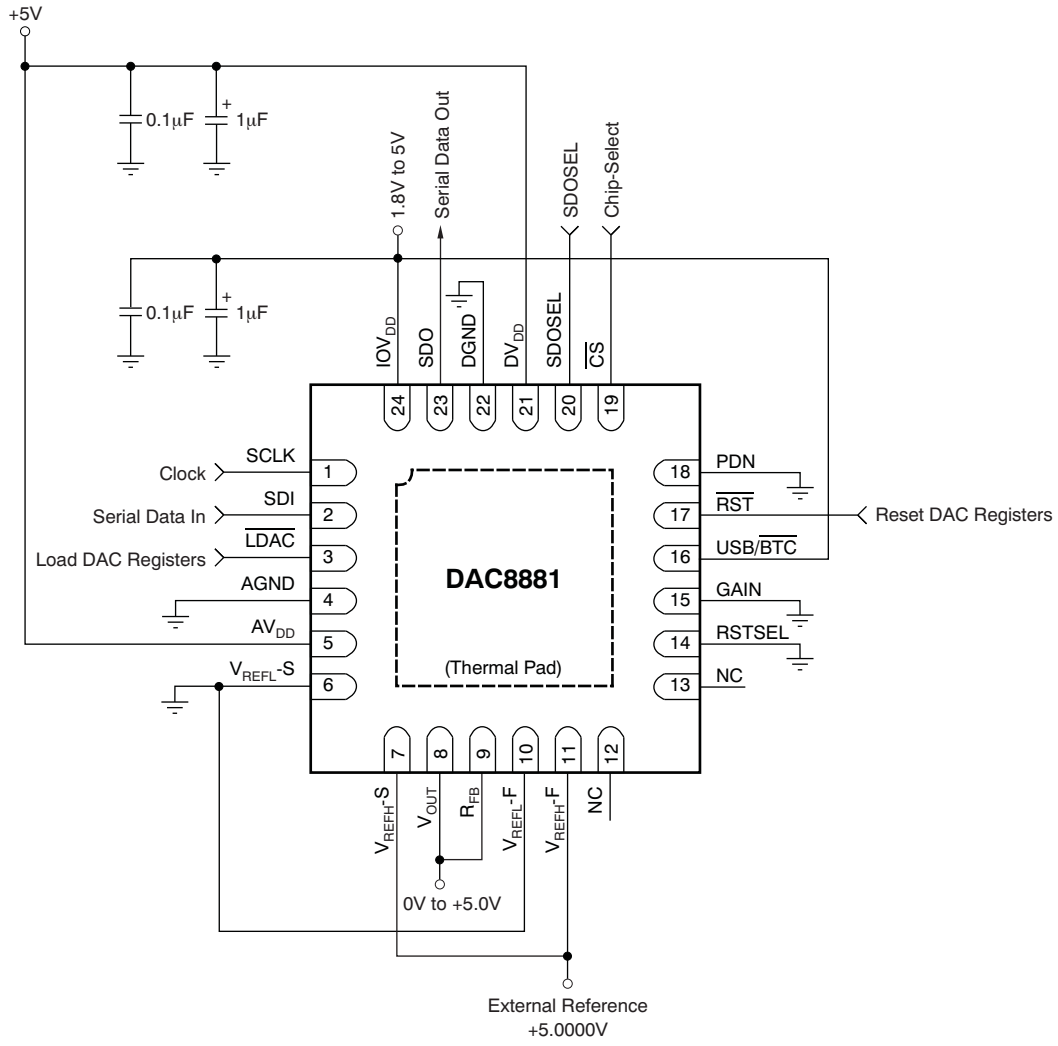
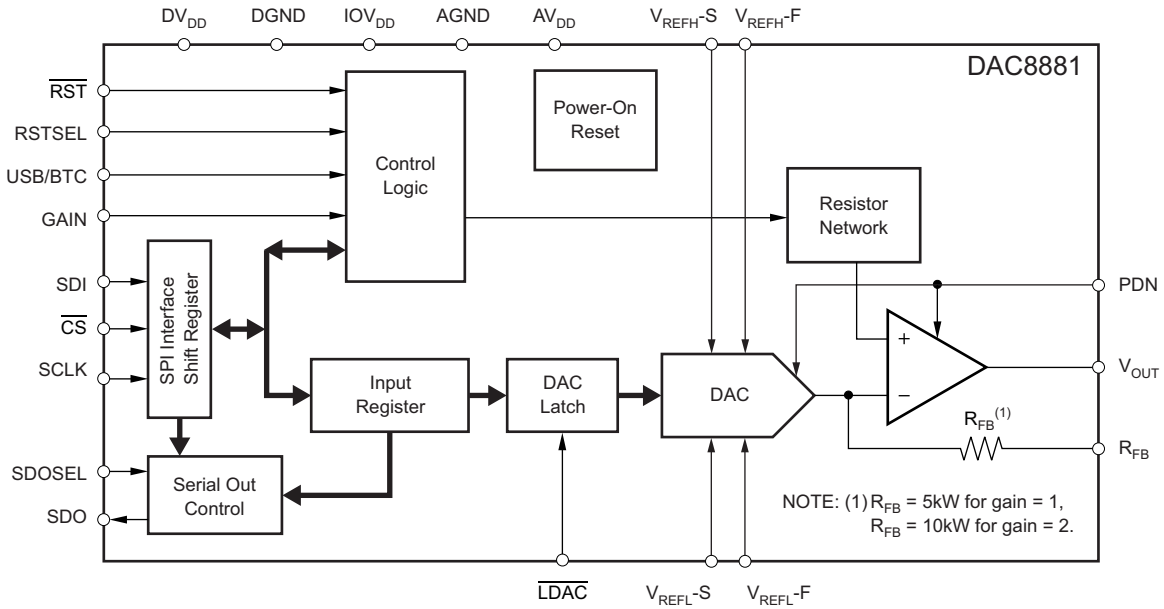


Figure 67. Basic Configuration

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Output

The DAC8881 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 68), thus ensuring an accurate output voltage. The output buffer V_{OUT} and R_{FB} pins are provided so that the output op amp buffer feedback can be connected at the load. Without a driven load, the DAC8881 output typically swings to within 15mV of the AGND and AV_{DD} supply rails. Because of the high accuracy of these DACs, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 5 V full-scale range has a 1 LSB value of 76 μV. With a load current of 1 mA, a series wiring and connector resistance of only 80mΩ (R_{W2}) causes a voltage drop of 80 μV. In terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board is 0.5mΩ per square. For a 1mA load, a 0.25 mm wide printed circuit conductor 25 mm long results in a voltage drop of 50 μV.

Feature Description (continued)

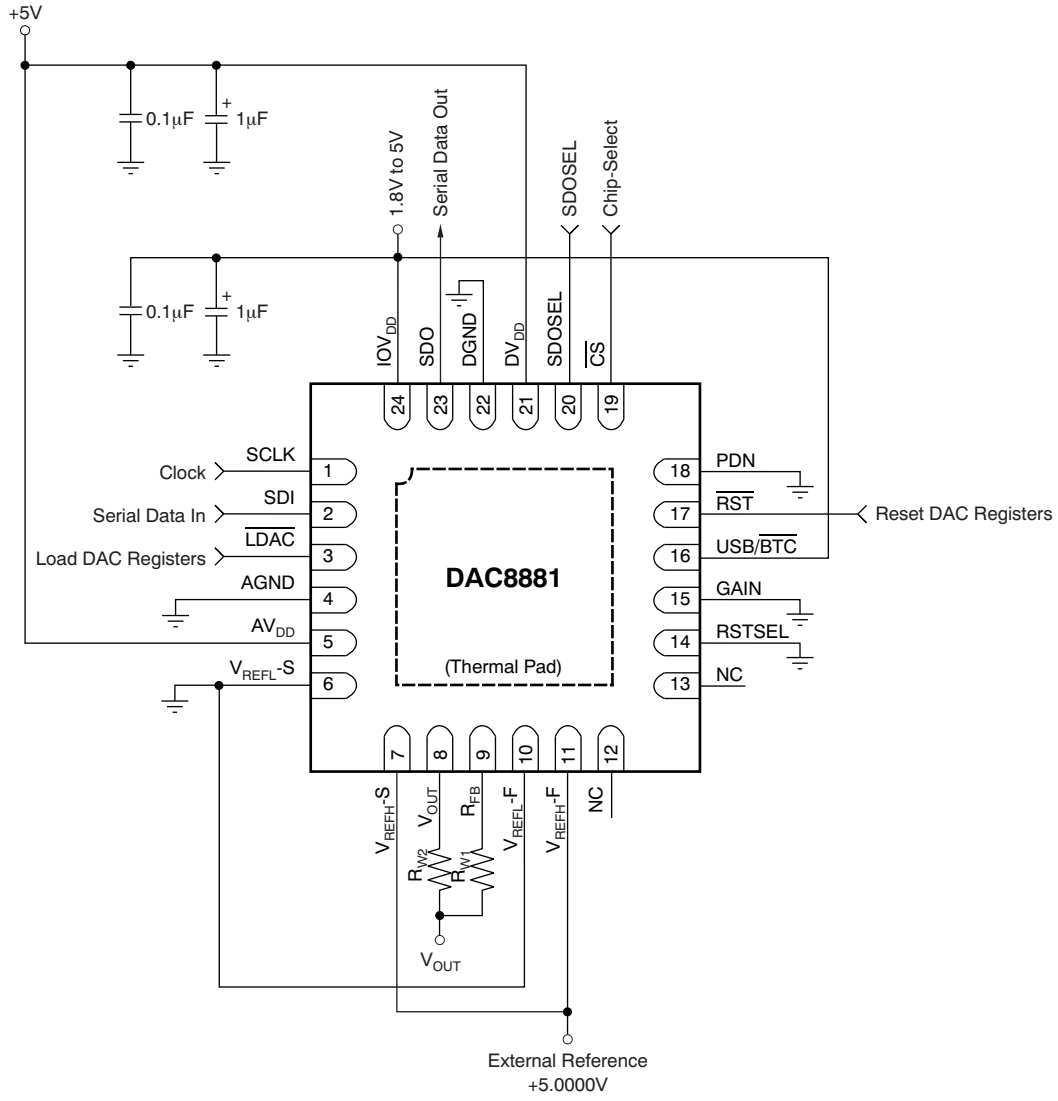


Figure 68. Analog Output Closed-Loop Configuration (R_{W1} and R_{W2} represent wiring resistance)

Feature Description (continued)

7.3.2 Reference Inputs

The reference high input, V_{REFH}, can be set to any voltage in the range of 1.25 V to AV_{DD}. The reference low input, V_{REFL}, can be set to any voltage in the range of –0.2 V to +0.2 V (to provide a small offset to the output of the DAC8881, if desired). The current into V_{REFH} and out of V_{REFL} depends on the DAC code, and can vary from approximately 0.5mA to 1mA in the gain = 1X mode of operation. The reference high and low inputs appear as varying loads to the external reference circuit. If the external references can source or sink the required current, and if low impedance connections are made to the V_{REFH} and V_{REFL} pins, external reference buffers are not required. Figure 67 shows a simple configuration of the DAC8881 using external references without force/sense reference buffers.

Kelvin sense connections for the reference high and low are included on the DAC8881. When properly used with external reference buffer op amps, these reference Kelvin sense pins ensure that the driven reference high and low voltages remain stable versus varying reference load currents. Figure 69 shows an example of a reference force/sense configuration of the DAC8881 operating from a single analog supply voltage. Both the V_{REFL} and V_{REFH} reference voltages are set to levels of 100 mV from the DAC8881 supply rails, and are derived from a 5-V external reference. Figure 71 and Figure 70 illustrate the effect of not using the reference force/sense buffers to drive the DAC8881 V_{REFL} and V_{REFH} pins. A slight degradation in INL and DNL performance of approximately 0.1 LSB may be seen without the use of the force/sense buffer configuration.

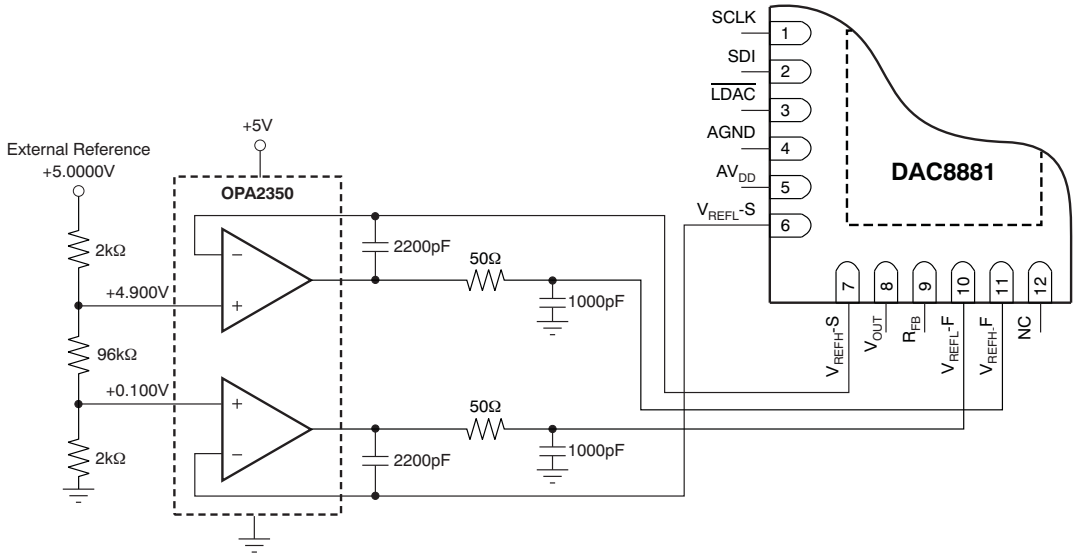


Figure 69. Buffered References (V_{REFH} = +4.900 V and V_{REFL} = 100 mV)

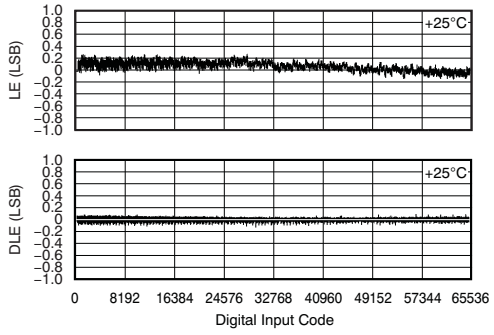


Figure 70. Linearity and Differential Linearity Error for Figure 67 without Reference Buffers

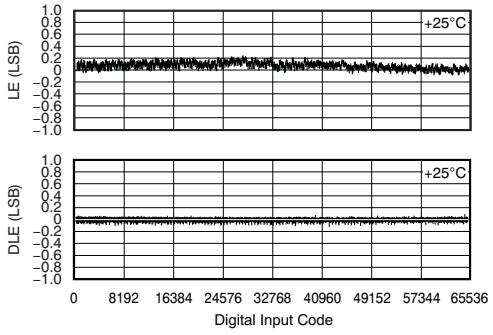


Figure 71. Linearity and Differential Linearity Error for Figure 69 with Reference Buffers

Feature Description (continued)

7.3.3 Output Range

The maximum output range of the DAC8881 is V_{REFL} to V_{REFH} × G, where *G* is the output buffer gain set by the GAIN pin. When the GAIN pin is connected to DGND, the output buffer gain = 1. When the GAIN pin is connected to IOV_{DD}, the output buffer gain = 2. The output range must not be greater than AV_{DD}; otherwise, output saturation occurs. The DAC8881 output transfer function is given in Equation 1:

$$V_{OUT} = \frac{V_{REFH} - V_{REFL}}{65536} \times CODE \times Buffer\ Gain + V_{REFL} \quad (1)$$

Where:

CODE = 0 to 65535. This is the digital code loaded to the DAC.
Buffer Gain = 1 or 2 (set by the GAIN pin).
V_{REFH} = reference high voltage applied to the device.
V_{REFL} = reference low voltage applied to the device.

7.3.4 Input Data Format

The USB/$\overline{BTC}$ pin defines the input data format.

When this pin is connected to IOV_{DD}, the input data format is straight binary, as shown in Table 1.

When this pin is connected to DGND, the input data format is twos complement, as shown in Table 2.

Table 1. Output vs Straight Binary Code

USB CODE	5 V RANGE	DESCRIPTION
FFFFh	+4.99992	+Full-Scale – 1LSB
C000h	+3.75000	3/4-Scale
8000h	+2.50000	Midscale
4000h	+1.25000	1/4-Scale
0000h	0.00000	Zero-Scale

Table 2. Output vs Twos Complement Code

$\overline{BTC}$ CODE	5 V RANGE	DESCRIPTION
7FFFh	+4.99992	+Full-Scale – 1LSB
4000h	+3.75000	3/4-Scale
0000h	+2.50000	Midscale
FFFFh	+2.49992	Midscale – 1LSB
C000h	+1.25000	1/4-Scale
8000h	0.00000	Zero-Scale

7.3.5 Hardware Reset

When the $\overline{RST}$ pin is low, the device is in hardware reset mode, and the input register and DAC latch are set to the value defined by the RSTSEL pin. After $\overline{RST}$ goes high, the device is in normal operating mode. When USB/$\overline{BTC}$ is connected to DGND, the device is in twos complement mode. In this case, the $\overline{LDAC}$ pin cannot be kept at logic level '0' or toggled when a hardware reset is issued before writing a valid DAC data.

7.3.6 Power-On Reset

The DAC8881 has a power-on reset function. After power-on, the value of the input register, the DAC latch, and the output from the V_{OUT} pin are set to the value defined by the RSTSEL pin.

7.3.7 Program Reset Value

After a power-on reset or a hardware reset, the output voltage from the V_{OUT} pin and the values of the input register and DAC latch are determined by the status of the RSTSEL pin and the input data format, as shown in Table 3.

Table 3. Reset Value

$\overline{LDAC}$ PIN	RSTSEL PIN	USB/$\overline{BTC}$ PIN	INPUT FORMAT	V_{OUT}	VALUE OF INPUT REGISTER AND DAC LATCH
DGND or IOV_{DD}	DGND	IOV_{DD}	Straight Binary	0	0000h
DGND or IOV_{DD}	IOV_{DD}	IOV_{DD}	Straight Binary	Midscale	8000h
IOV_{DD}	DGND	DGND	Twos Complement	0	0000h
IOV_{DD}	IOV_{DD}	DGND	Twos Complement	Midscale	8000h

7.3.8 Power Down

The DAC8881 has a hardware power-down function. When the PDN pin is high, the device is in power-down mode. The V_{OUT} pin is connected to ground through an internal 10-kΩ resistor, but the contents of the input register and the DAC latch do not change. In power-down mode, SPI communication is still active.

7.3.9 Double-Buffered Interface

The DAC8881 has a double-buffered interface consisting of two register banks: the input register and the DAC latch. The input register is connected directly to the input shift register and the digital code is transferred to the input register upon completion of a valid write sequence. The DAC latch contains the digital code used by the resistor R-2R ladder. The contents of the DAC latch defines the output from the DAC.

Access to the DAC register is controlled by the $\overline{LDAC}$ pin. When $\overline{LDAC}$ is high, the DAC register is latched and the input register can change state without affecting the contents of the DAC latch. When $\overline{LDAC}$ is low, however, the DAC latch becomes transparent and the contents of the input register is transferred to the DAC register.

7.3.10 Load DAC Pin ($\overline{LDAC}$)

$\overline{LDAC}$ transfers data from the input register to the DAC register and; therefore, updates the DAC output. The contents of the DAC latch (and the output from DAC) can be changed in two ways, depending on the status of $\overline{LDAC}$.

7.3.10.1 Synchronous Mode

When $\overline{LDAC}$ is tied low, the DAC register updates as soon as new data are transferred into the input register after the rising edge of $\overline{CS}$.

7.3.10.2 Asynchronous Mode

When $\overline{LDAC}$ is high, the DAC latch is latched. The DAC latch (and DAC output) is not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low, the DAC register updates with the contents of the input register.

7.3.11 1.8 V to 5.5 V Logic Interface

All digital input and output pins are compatible with any logic supply voltage between 1.8 V and 5.5 V. Connect the interface logic supply voltage to the IOV_{DD} pin. Although timing is specified down to 2.7 V (see the *Timing Characteristics*), IOV_{DD} can operate as low as 1.8 V, but with degraded timing and temperature performance. For the lowest power consumption, logic V_{IH} levels should be as close as possible to IOV_{DD}, and logic V_{IL} levels should be as close as possible to GND. Note that the DAC8881 core internal digital logic operates from the same voltage as the 2.7V to 5.5V AV_{DD} supply, so the DV_{DD} pin must also be connected to the AV_{DD} supply voltage.

7.4 Device Functional Modes

7.4.1 Serial Interface

The DAC8881 is controlled by a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP™ interface standards.

7.4.1.1 Input Shift Register

Data are loaded into the device as a 16-bit word under the control of the serial clock input, SCLK. The timing diagrams for this operation are shown in the *Timing Diagram* section.

The $\overline{CS}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while $\overline{CS}$ is low. To start the serial data transfer, $\overline{CS}$ should be taken low, observing the minimum $\overline{CS}$ falling edge to SCLK rising edge setup time, t_2. After $\overline{CS}$ goes low, serial data are clocked into the device input shift register on the rising edges of SCLK for 16 or more clock pulses. If a frame contains less than 16 bits of data, the frame is invalid. Invalid data are not written into the input register and DAC, although the input register and DAC will continue to hold data from the preceding valid data cycle. If more than 16 bits of data are transmitted in one frame, the last 16 bits are written into the shift register and DAC. $\overline{CS}$ may be taken high after the rising edge of the 16th SCLK pulse, observing the minimum SCLK rising edge to $\overline{CS}$ rising edge time, t_7. The contents of the shift register are transferred into the input register on the rising edge of $\overline{CS}$. When data have been transferred into the input register of the DAC, the corresponding DAC register and DAC output can be updated by taking the $\overline{LDAC}$ pin low.

7.4.1.1.1 Stand-Alone Mode

When the SDOSEL pin is tied to IOV_{DD}, the interface is in Stand-Alone mode. This mode provides serial readback for diagnostic purposes. The new input data (16 bits) are clocked into the device shift register and the existing data in the input register (16 bits) are shifted out from the SDO pin. If more than 16 SCLKs are clocked when $\overline{CS}$ is low, the contents of the input register are shifted out from the SDO pin, followed by zeroes; the last 16 bits of input data remain in the shift register. If less than 16 SCLKs are clocked while $\overline{CS}$ is low, the data from the SDO pin are part of the data in the input register and must be ignored. Refer to Figure 2 for further detail.

7.4.1.1.2 Daisy-Chain Mode

When the SDOSEL pin is tied to GND, the interface is in Daisy-Chain mode. For systems that contain several DACs, the SDO pin may be used to daisy-chain several devices together.

In Daisy-Chain mode, SCLK is continuously applied to the input shift register while $\overline{CS}$ is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. These data are clocked out on the falling edge of SCLK and are valid on the rising edge. By connecting this line to the DIN input on the next DAC in the chain, a multi-DAC interface is constructed. 16 clock pulses are required for each DAC in the system. Therefore, the total number of clock cycles must be equal to (16 x *N*), where *N* is the total number of devices in the chain. When the serial transfer to all devices is complete, $\overline{CS}$ should be taken high. This action prevents any further data from being clocked into the input shift register. The contents in the shift registers are transferred into the relevant input registers on the rising edge of the $\overline{CS}$ signal.

A continuous SCLK source may be used if $\overline{CS}$ can be held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles can be used and $\overline{CS}$ can be taken high some time later. When the transfer to all input registers is complete, a common $\overline{LDAC}$ signal updates all DAC registers, and all analog outputs update simultaneously.

8 Application and Implementation

NOTE

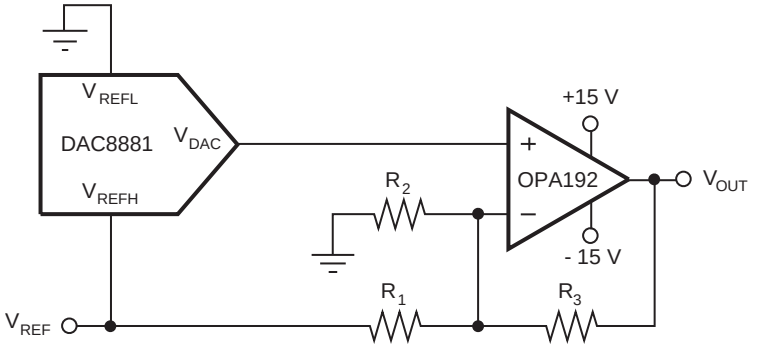
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The excellent linearity as well as low-noise and fast settling time makes the DAC8881 a strong performer in applications such as automatic test equipment, precision instrumentation and data acquisition systems. Additionally, the energy saving feature of the device, through the PDN pin, significantly reduces power dissipation -- this mode reduces current consumption, as low as 25 µA with a 5-V supply.

8.1.1 Bipolar Operation Using The DAC8881

The DAC8881 is designed for single-supply operation; however, a bipolar output is also possible using the circuit shown in Figure 72. This circuit gives a bipolar output voltage of VOUT. When GAIN = 1, VOUT can be calculated using Equation 2:



Some pins are omitted for clarity.

Figure 72. Bipolar Operation Using the DAC8881

$$V_{BIP}(CODE) = \left[1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}\right] \times \frac{CODE}{65536} - \frac{R_3}{R_1} \times V_{REF} \quad (2)$$

Where:

V_{BIP}(CODE) = bipolar output voltage versus CODE from the OPA211.

CODE = 0 to 262143. This is the digital code loaded to the DAC.

V_{REF} = reference high voltage applied to the DAC8881.

As an example, a ±8-V output span can be achieved by using values of 5 V, 6.25 kΩ, 16.67 kΩ, and 10 kΩ for Vref, R1, R2, and R3 respectively.

8.2 Typical Application

8.2.1 DAC8881 Sample Hold Circuit

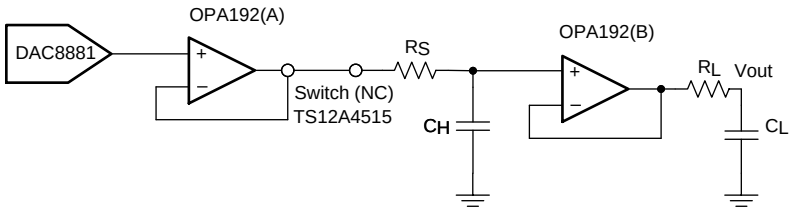


Figure 73. DAC8881 Sample and Hold Circuit

8.2.1.1 Design Requirements

The inherent architecture of the DAC8881, which consists of an R-2R architecture, enables great performance in regards to noise and accuracy, but at a cost of large glitch area. Glitch area, also known as glitch impulse area, is defined as the area associated with the overshoot or undershoot created by a code transition, and is generally quantified in Volt-seconds. Different code-to-code transitions produce different levels of glitch impulses. DACs with R-2R architectures produce large glitches during major-carry transitions.

There are two methods that can be used to reduce this glitch area:

1. Add an external RC Filter to the output of the DAC.
   - The low-pass filter helps attenuate high-frequency glitches that would normally propagate to the DAC output. Best practice is to use a small resistor value, as large resistance develops a large potential drop and reduces the voltage seen at the load. Capacitor values can be determined from the desired cutoff frequency of the low-pass filter, as well as settling time.
2. Another technique is to employ a Sample and Hold (S&H) circuit following the DAC output.
   - In its simplest form, the sample and hold circuit can be constructed from the following components: a capacitive element, output buffer, and switch. A schematic of the simplified S&H is shown in Figure 74.

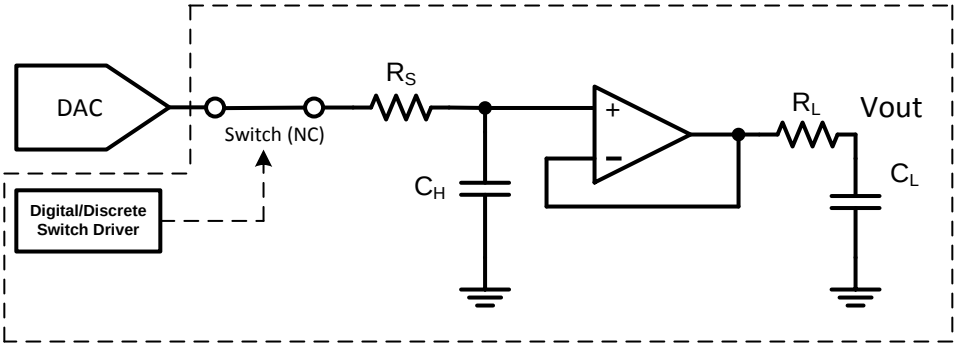


Figure 74. Simplified Sample and Hold Circuit

8.2.1.2 Detailed Design Procedure

The Sample/Track and Hold modes of operation correspond to the state of the switch, which connects the DAC output to the hold capacitor C_H. In sample mode – also referred to as track mode -- the switch is closed, allowing the capacitor to charge or discharge to the sampled DAC output voltage. The operational amplifier is configured as a buffer, which tracks and relays the voltage seen across C_H to the output of the circuit. In hold mode, the switch opens, disconnecting C_H from the DAC output. The DAC is updated while the circuit is in hold mode, preventing any DAC major carry glitches from propagating to the S&H output. The capacitor retains the previous sampled voltage, and this value is buffered to the output of the circuit. In real circuits, switch leakage and operational amplifier input bias current must be considered as it will impact circuit performance. The switch is generally controlled by an external discrete or digital driver.

Typical Application (continued)

Once the DAC glitch relays the switch closes and re-enters sample or track mode.

More information related to this circuit can be found in *Sample & Hold Glitch Reduction for Precision Outputs Design Guide* (TIDU022).

8.2.1.3 Application Curves

Glitch reduction and total unadjusted error (TUE) plots of the solution presented in *Sample & Hold Glitch Reduction for Precision Outputs Design Guide* (TIDU022) is shown in the following plots. The glitch area is reduced from 35.11 nVs to 2.01 nVs.

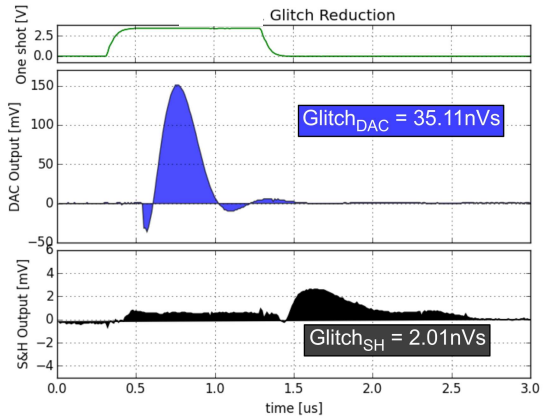
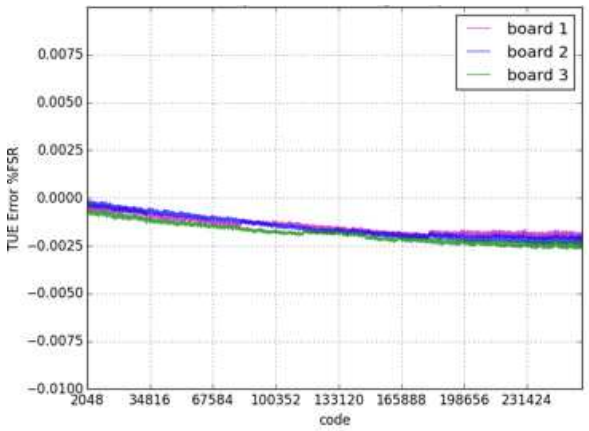


Figure 75. DAC8881 Sample and Hold TUE Error %FSR



C_H = 8.2 nF R_S = 14.7 Ω

Figure 76. Measured Glitch Area (20000h-1FFFFh 18-bit Data) (Top) Digital Signal One-Shot Pulse; (Middle) DAC Output Glitch; (Bottom) S&H Output Glitch

8.3 System Example

Figure 77 displays a typical serial interface that may be used when connecting the DAC8881 SPI serial interface to a (master) microcontroller. The setup for the interface is as follows: The microcontroller output SPI CLK drives the SCLK pin of the DAC8881, while the DAC8881 SDI pin is driven by the MOSI pin of the microcontroller. The $\overline{CS}$ pin of the DAC8881 can be asserted from a general program input/output pin of the microcontroller. When data are to be transmitted to the DAC8881, the $\overline{CS}$ pint is taken low. The data from the microcontroller is then transmitted to the DAC8881, totaling 24 bits latched into the DAC8881 device through the negative edge of SCLK. $\overline{CS}$ is then brought high after the completed write. The DAC8881 requires its data with the MSB as the first bit received.

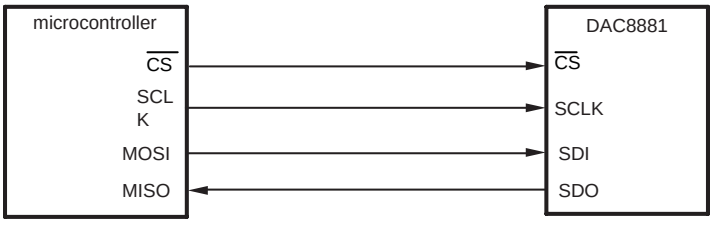


Figure 77. Simplified Sample and Hold Circuit

9 Power Supply Recommendations

The DAC8881 can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to AVDD should be well regulated and low noise. Switching power supplies and DC-DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. To further minimize noise from the power supply, a strong recommendation is to include a 1-µF to 10-µF capacitor and 0.1-µF bypass capacitor. The current consumption on the AVDD pin, the short-circuit current limit, and the load current for the device is listed in *Electrical Characteristics*. The power supply must meet the aforementioned current requirements.

10 Layout

10.1 Layout Guidelines

A precision analog component requires careful layout, the list below provides some insight into good layout practices.

- All Power Supply pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 to 0.22 µF ceramic with a X7R or NP0 dielectric.
- Power supplies and VrefH/L bypass capacitors should be placed close to terminals to minimize inductance and optimize performance.
- A high-quality ceramic type NP0 or X7R is recommended for its optimal performance across temperature, and very low dissipation factor.
- The digital and analog sections should have proper placement with respect to the digital pins and analog pins of the DAC8881 device. The separation of analog and digital blocks will allow for better design and practice as it will ensure less coupling into neighboring blocks, and will minimize the interaction between analog and digital return currents.

10.2 Layout Example

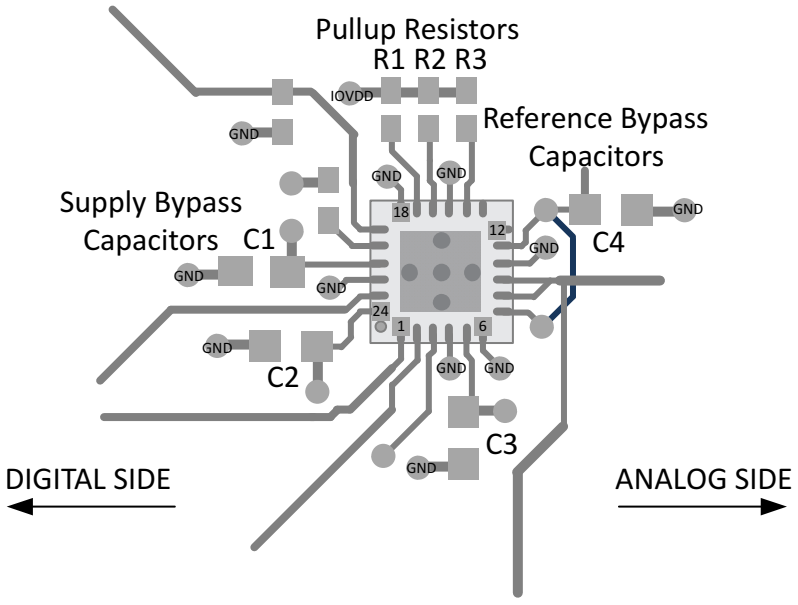


Figure 78. DAC8881 Basic Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- *『DAC8881評価モジュール』*(SLAU257)
- *『高精度出力のサンプル・アンド・ホールドのグリッチ低減設計ガイド』*(TIDU022)

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11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8881SRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC 8881	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

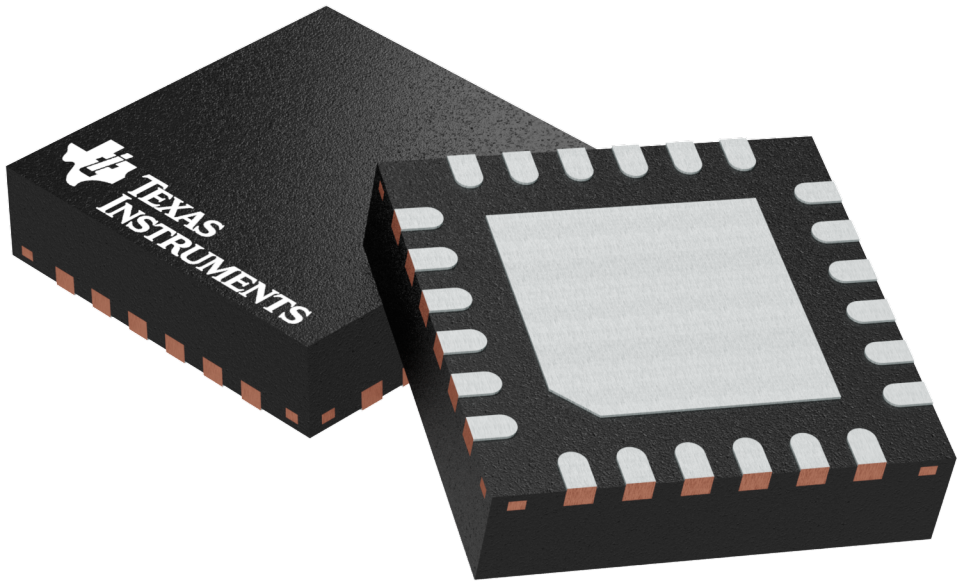
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

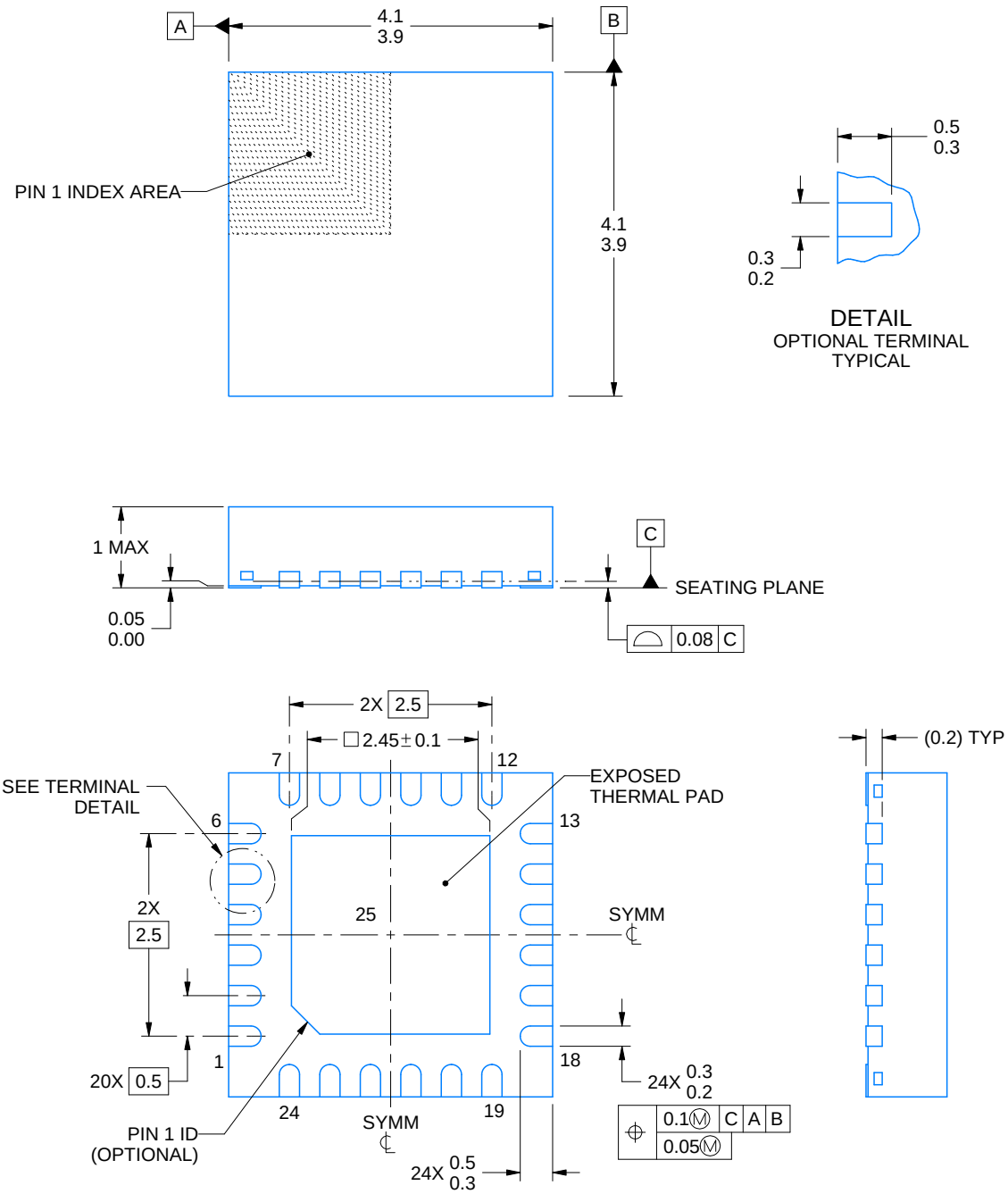
4204104/H

PACKAGE OUTLINE

RGE0024B

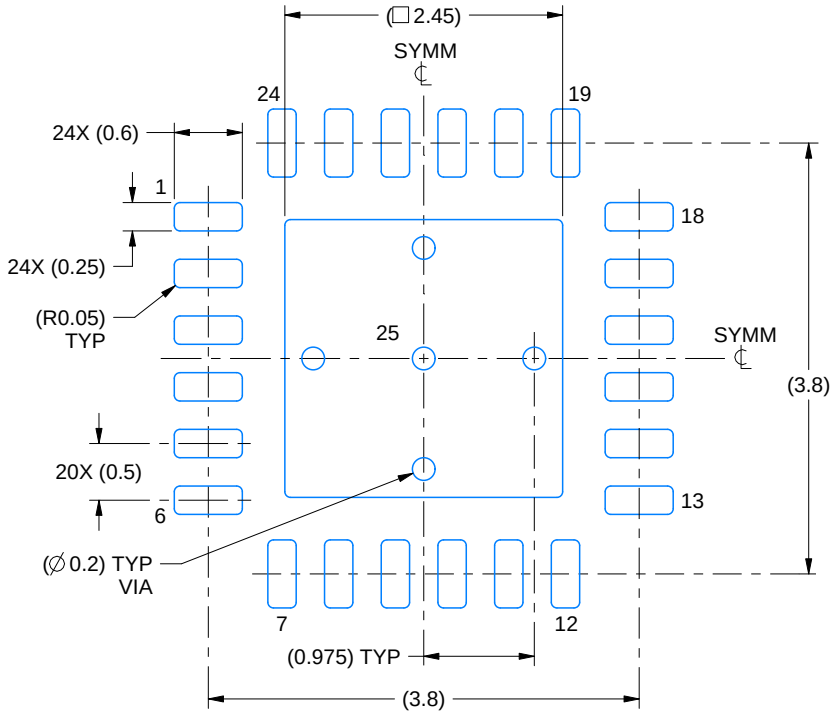
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

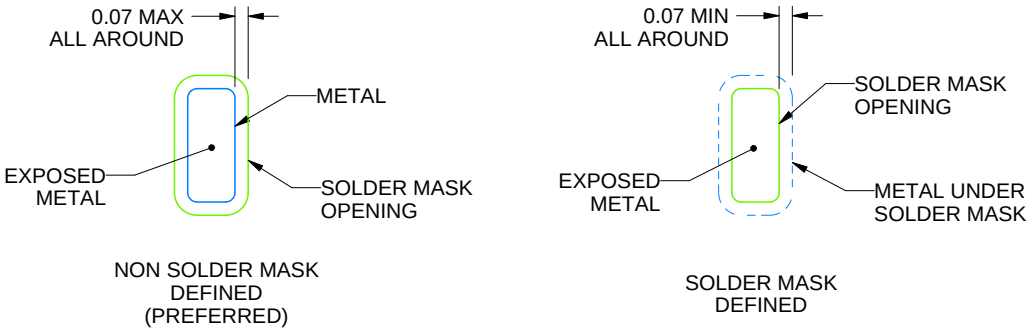


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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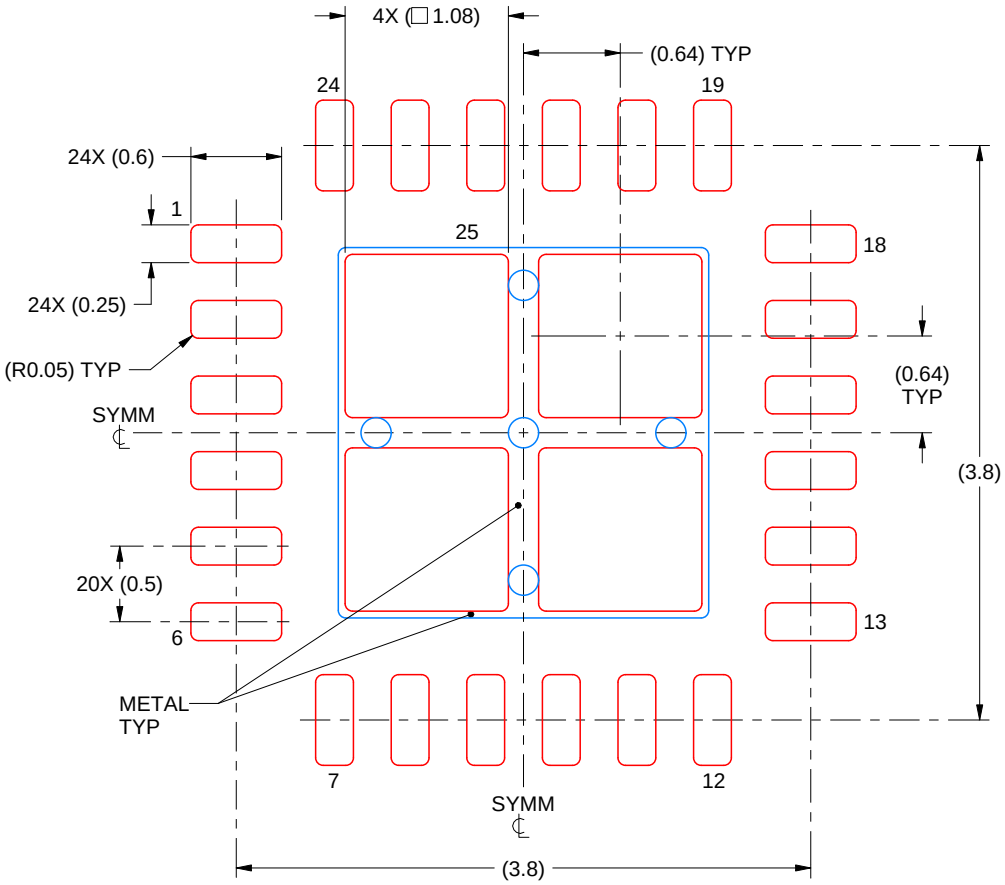
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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