参考資料

# CSD86336Q3D 同期整流降圧型NexFET™パワー・ブロック

## 1 特長

- ハーフ・ブリッジ・パワー・ブロック
- 12A時に93.0%のシステム効率
- 最大20Aで動作
- 高周波数での動作(最高1.5MHz)
- 高密度SON、占有面積3.3mm×3.3mm
- 5Vゲートの駆動に最適化
- 低いスイッチング損失
- インダクタンスの非常に低いパッケージ
- RoHS準拠
- ハロゲン不使用
- 鉛フリーの端子メッキ処理

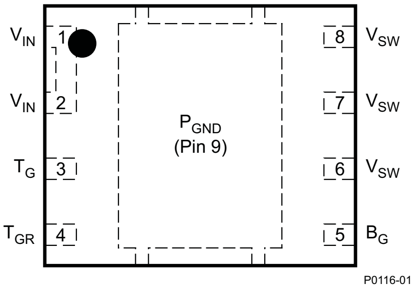
## 2 アプリケーション

- 同期整流降圧コンバータ
  - 高周波数のアプリケーション
  - 大電流、低いデューティ・サイクルのアプリケーション
- マルチフェーズの同期整流降圧コンバータ
- POL DC/DCコンバータ
- IMVP、VRM、VRDアプリケーション

## 3 概要

CSD86336Q3D NexFET™ パワー・ブロックは、同期整流降圧アプリケーション向けに最適化された設計で、大電流、高効率、高周波数の能力を小さな3.3mm×3.3mmの外形に収めています。この製品は5Vのゲート駆動アプリケーション用に最適化されており、外部のコントローラ/ドライバからの任意の5Vゲート・ドライブと組み合わせて、高密度の電源を実現できます。

**上面図**

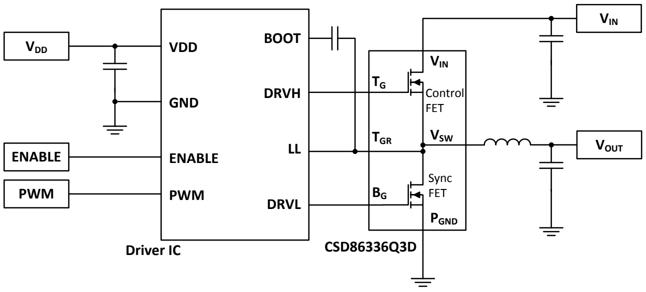


**製品情報[(1)]**

| デバイス | メディア | 数量 | パッケージ | 出荷 |
|---|---|---|---|---|
| CSD86336Q3D | 13インチ・リール | 2500 | SON<br>3.30mm×3.30mm<br>プラスチック・パッケージ | テープ・アンド・リール |
| CSD86336Q3DT | 7インチ・リール | 250 | | |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

**回路例**



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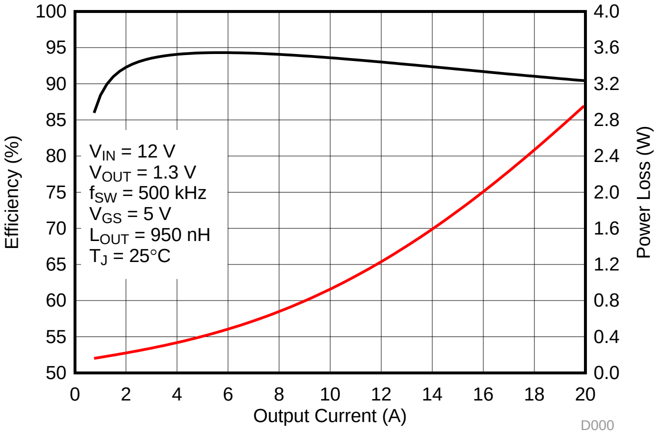
**標準的な電力ブロックの効率と電力損失との関係**



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# 目次

## 4 改訂履歴

| 日付 | 改訂内容 | 注 |
|---|---|---|
| 2018年3月 | * | 初版 |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

TA = 25°C (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ to $P_{GND}$ | | 25 | V |
| | $V_{SW}$ to $P_{GND}$ | | 25 | |
| | $V_{SW}$ to $P_{GND}$ (10 ns) | | 27 | |
| | $T_G$ to $T_{GR}$ | –8 | 10 | |
| | $B_G$ to $P_{GND}$ | –8 | 10 | |
| Pulsed current rating, IDM(2) | | | 60 | A |
| Power dissipation, $P_D$ | | | 6 | W |
| Avalanche energy, $E_{AS}$ | Sync FET, $I_D$ = 40 A, L = 0.1 mH | | 80 | mJ |
| | Control FET, $I_D$ = 26 A, L = 0.1 mH | | 34 | |
| $T_J$ and $T_{STG}$ | Operating junction and storage temperature | –55 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse duration = 50 µS. Duty cycle = 0.01.

## 5.2 Recommended Operating Conditions

$T_A$ = 25°C (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{GS}$ | Gate drive voltage | 4.5 | 8 | V |
| $V_{IN}$ | Input supply voltage(1) | | 22 | V |
| $f_{SW}$ | Switching frequency $C_{BST}$ = 0.1 µF (min) | | 1500 | kHz |
| | Operating current | | 20 | A |
| $T_J$ | Operating temperature | | 125 | °C |
| $T_{STG}$ | Storage temperature | | 125 | °C |

(1) Operating at high $V_{IN}$ can create excessive AC voltage overshoots on the switch node ($V_{SW}$) during MOSFET switching transients. For reliable operation, the switch node ($V_{SW}$) to ground voltage must remain at or below the *Absolute Maximum Ratings*.

## 5.3 Thermal Information

$T_A$ = 25°C (unless otherwise noted)

| THERMAL METRIC | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (min Cu)(1) | | 105 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (max Cu)(1) (2) | | 55 | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance (top of package)(1) | | 17 | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance ($P_{GND}$ pin)(1) | | 3.2 | °C/W |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in$^2$ (6.45-cm$^2$), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in$^2$ (6.45-cm$^2$) Cu.

## 5.4 Power Block Performance

$T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_{LOSS}$ | Power loss(1) | $V_{IN}$ = 12 V, $V_{GS}$ = 5 V, $V_{OUT}$ = 1.3 V, $I_{OUT}$ = 15 A, $f_{SW}$ = 500 kHz, $L_{OUT}$ = 950 nH, $T_J$ = 25°C | | 1.8 | | W |
| $I_{QVIN}$ | $V_{IN}$ quiescent current(1) | $T_G$ to $T_{GR}$ = 0 V, $B_G$ to $P_{GND}$ = 0 V, $V_{IN}$ = 12 V | | 10 | | µA |

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across $V_{IN}$ to $P_{GND}$ pins and using a high-current 5-V driver IC.

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## 5.5 Electrical Characteristics – Q1 Control FET

$T_j$ = 25 °C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0 V, $I_{DS}$ = 250 µA | 25 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = 20 V | | | 1 | µA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = +10 / –8 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250 µA | 1.1 | 1.5 | 1.9 | V |
| $Z_{DS(on)}$ | Effective AC on-impedance | $V_{IN}$ = 12 V, $V_{GS}$ = 5 V, $V_{OUT}$ = 1.3 V, $I_{OUT}$ = 20 A, $f_{SW}$ = 500 kHz, $L_{OUT}$ = 950 nH | | 9.1 | | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 2.5 V, $I_{DS}$ = 14 A | | 40 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{ISS}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 12.5 V, $f$ = 1 Mhz | | 380 | 494 | pF |
| $C_{OSS}$ | Output capacitance | | | 263 | 342 | pF |
| $C_{RSS}$ | Reverse transfer capacitance | | | 14.1 | 18.3 | pF |
| $R_G$ | Series gate resistance | | | 4.0 | 8.0 | Ω |
| $Q_g$ | Gate charge total (4.5 V) | $V_{DS}$ = 12.5 V, $I_{DS}$ = 14 A | | 2.9 | 3.8 | nC |
| $Q_{gd}$ | Gate charge – gate-to-drain | | | 0.6 | | nC |
| $Q_{gs}$ | Gate charge – gate-to-source | | | 1.4 | | nC |
| $Q_{g(th)}$ | Gate charge at $V_{th}$ | | | 0.6 | | nC |
| $Q_{OSS}$ | Output charge | $V_{DS}$ = 12.5 V, $V_{GS}$ = 0 V | | 5.4 | | nC |
| $t_{d(on)}$ | Turn on delay time | $V_{DS}$ = 12.5 V, $V_{GS}$ = 4.5 V, $I_{DS}$ = 14 A, $R_G$ = 0 Ω | | 5 | | ns |
| $t_r$ | Rise time | | | 10 | | ns |
| $t_{d(off)}$ | Turn off delay time | | | 7 | | ns |
| $t_f$ | Fall time | | | 2 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_{DS}$ = 14 A, $V_{GS}$ = 0 V | | 0.86 | 1.0 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DS}$ = 12.5 V, $I_F$ = 14 A, di/dt = 300 A/µs | | 14.7 | | nC |
| $t_{rr}$ | Reverse recovery time | | | 15 | | ns |

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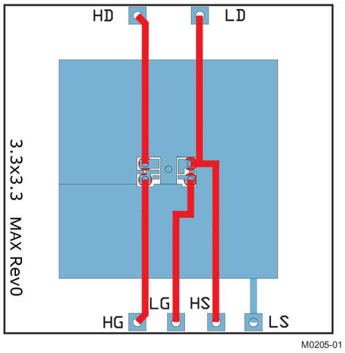
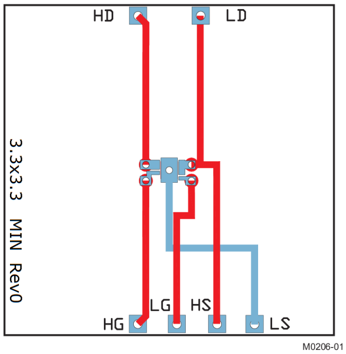
## 5.6 Electrical Characteristics – Q2 Sync FET

$T_j$ = 25 °C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0 V, $I_{DS}$ = 250 µA | 25 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = 20 V | | | 1 | µA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = +10 / –8 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250 µA | 1.0 | 1.3 | 1.6 | V |
| $Z_{DS(on)}$ | Effective AC on-impedance | $V_{IN}$ = 12 V, $V_{GS}$ = 5 V, $V_{OUT}$ = 1.3 V,<br>$I_{OUT}$ = 20 A, $f_{SW}$ = 500 kHz,<br>$L_{OUT}$ = 950 nH | | 3.4 | | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 2.5 V, $I_{DS}$ = 14 A | | 57 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{ISS}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 12.5 V, $f$ = 1 Mhz | | 728 | 970 | pF |
| $C_{OSS}$ | Output capacitance | | | 501 | 664 | pF |
| $C_{RSS}$ | Reverse transfer capacitance | | | 26 | 33 | pF |
| $R_G$ | Series gate resistance | | | 0.65 | 1.3 | Ω |
| $Q_g$ | Gate charge total (4.5 V) | $V_{DS}$ = 12.5 V, $I_{DS}$ = 14 A | | 5.7 | 7.4 | nC |
| $Q_{gd}$ | Gate charge – gate-to-drain | | | 1.2 | | nC |
| $Q_{gs}$ | Gate charge – gate-to-source | | | 2.1 | | nC |
| $Q_{g(th)}$ | Gate charge at $V_{th}$ | | | 1.0 | | nC |
| $Q_{OSS}$ | Output charge | $V_{DS}$ = 12.5 V, $V_{GS}$ = 0 V | | 10.3 | | nC |
| $t_{d(on)}$ | Turn on delay time | $V_{DS}$ = 12.5 V, $V_{GS}$ = 4.5 V, $I_{DS}$ = 14 A,<br>$R_G$ = 0 Ω | | 4 | | ns |
| $t_r$ | Rise time | | | 10 | | ns |
| $t_{d(off)}$ | Turn off delay time | | | 8 | | ns |
| $t_f$ | Fall time | | | 2 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_{DS}$ = 14 A, $V_{GS}$ = 0 V | | 0.82 | 0.95 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DS}$ = 12.5 V, $I_F$ = 14 A, di/dt = 300 A/µs | | 25.4 | | nC |
| $t_{rr}$ | Reverse recovery time | | | 18 | | ns |



Max $R_{\theta JA}$ = 55°C/W when mounted on 1 $in^2$ ($6.45\ cm^2$) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 105°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

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## 5.7 Typical Power Block Device Characteristics

Test conditions: $V_{IN}$ = 12 V, $V_{DD}$ = 5 V, $f_{SW}$ = 500 kHz, $V_{OUT}$ = 1.3 V, $L_{OUT}$ = 0.95 µH, $I_{OUT}$ = 20 A, $T_J$ = 125°C, unless stated otherwise.

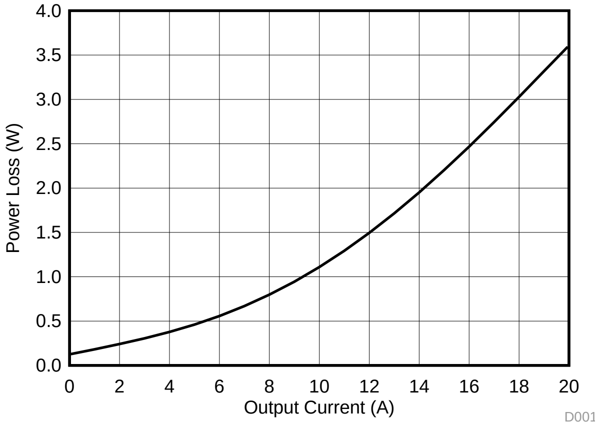

図 1. Power Loss vs Output Current

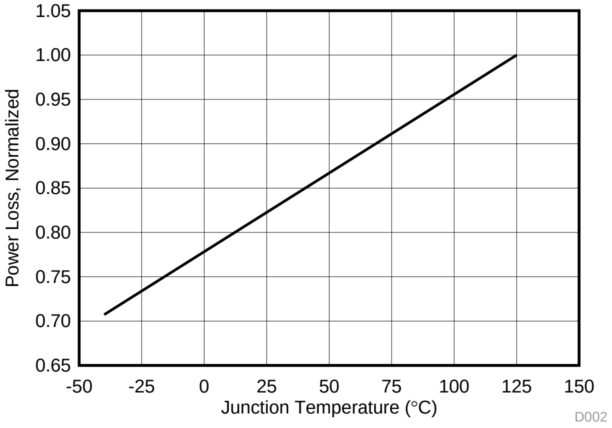

図 2. Power Loss vs Temperature

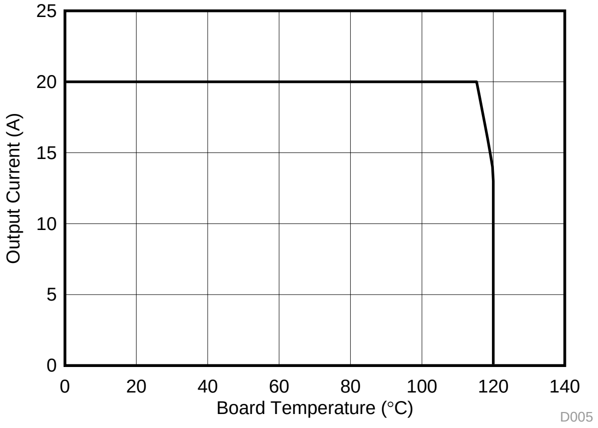

図 3. Typical Safe Operating Area (SOA) (1)

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(1) The Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See *Application and Implementation* section for detailed explanation.

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## Typical Power Block Device Characteristics (continued)

Test conditions: $V_{IN}$ = 12 V, $V_{DD}$ = 5 V, $f_{SW}$ = 500 kHz, $V_{OUT}$ = 1.3 V, $L_{OUT}$ = 0.95 µH, $I_{OUT}$ = 20 A, $T_J$ = 125°C, unless stated otherwise.

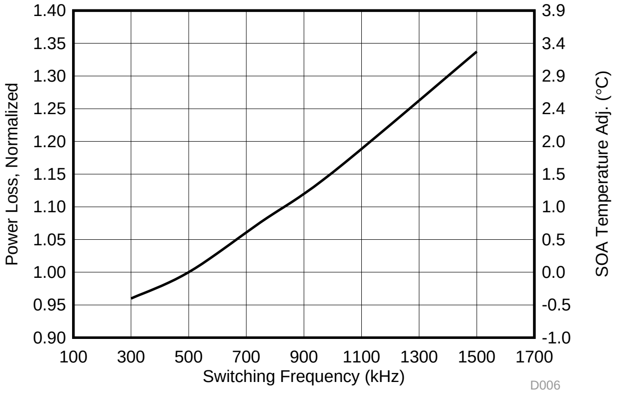


図 4. Normalized Power Loss vs Switching Frequency

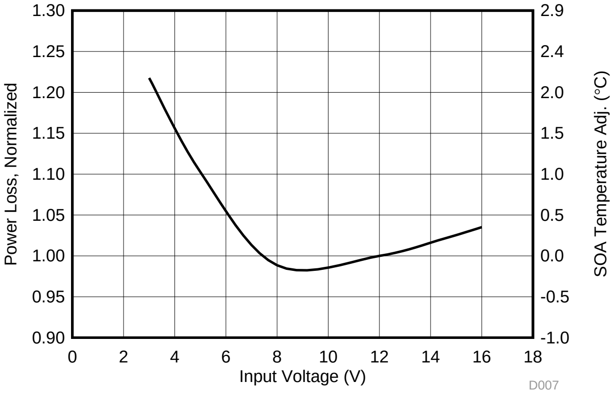


図 5. Normalized Power Loss vs Input Voltage

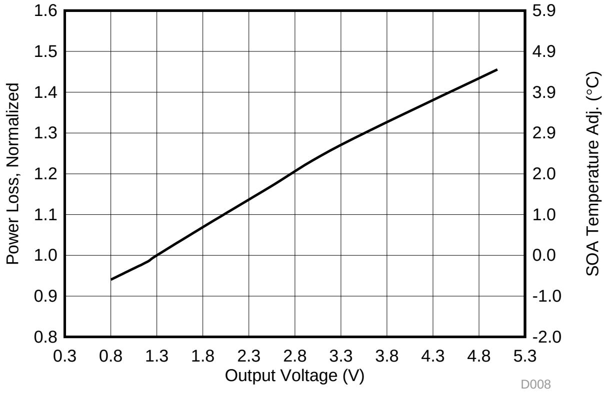


図 6. Normalized Power Loss vs Output Voltage

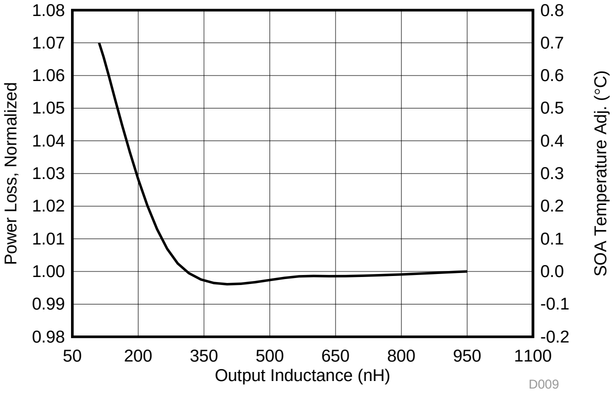


図 7. Normalized Power Loss vs Output Inductance

## 5.8 Typical Power Block MOSFET Characteristics

$T_A$ = 25°C, unless stated otherwise.

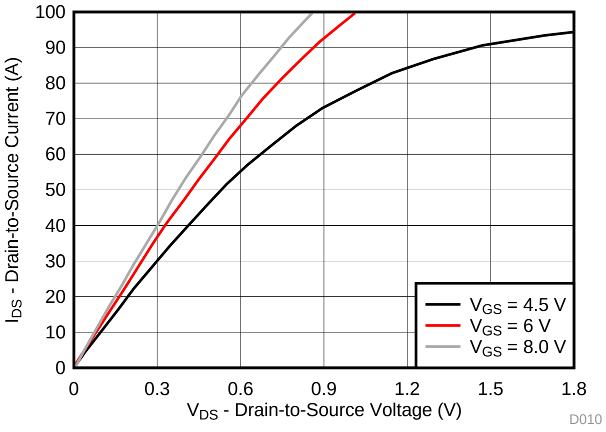


図 8. Control MOSFET Saturation

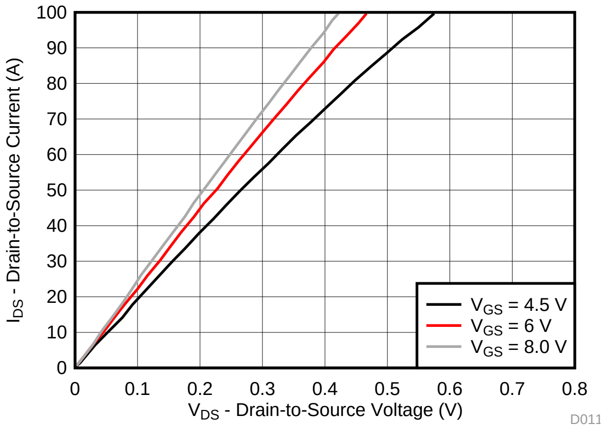
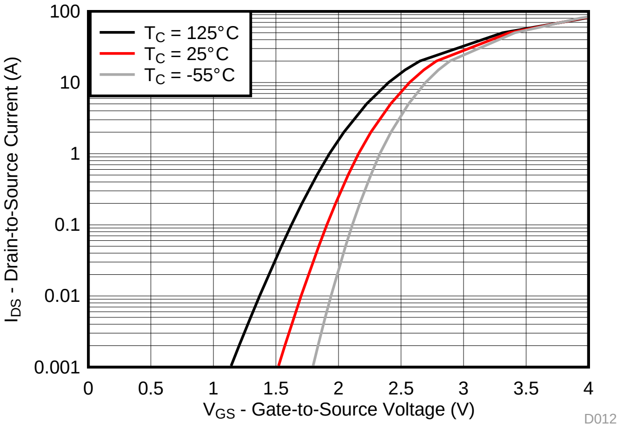
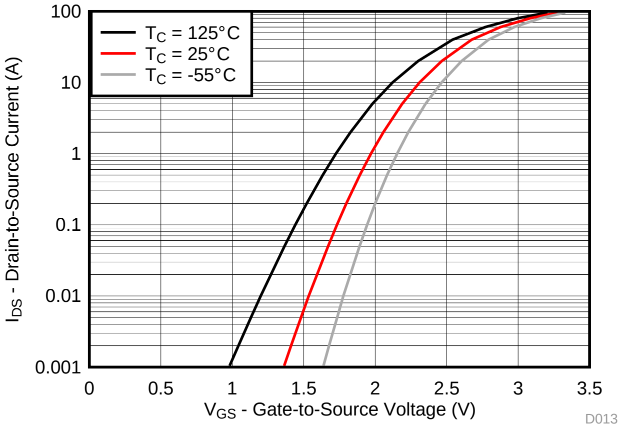


図 9. Sync MOSFET Saturation



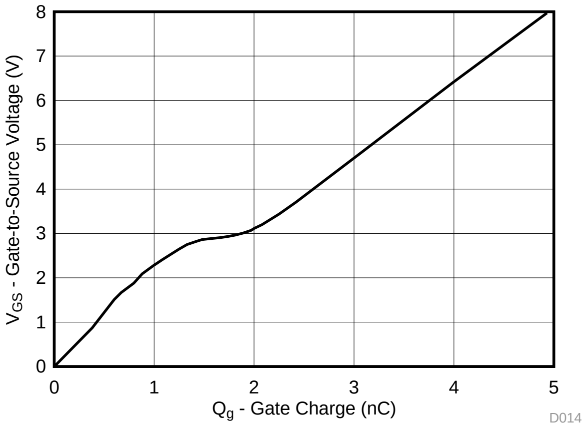
$V_{DS}$ = 5 V

図 10. Control MOSFET Transfer



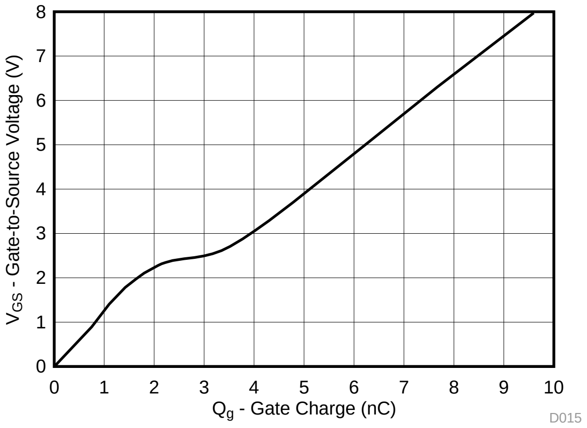
$V_{DS}$ = 5 V

図 11. Sync MOSFET Transfer



$I_D$ = 14 A $V_{DD}$ = 12.5 V

図 12. Control MOSFET Gate Charge



$I_D$ = 14 A $V_{DD}$ = 12.5 V

図 13. Sync MOSFET Gate Charge

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## Typical Power Block MOSFET Characteristics (continued)

$T_A$ = 25°C, unless stated otherwise.

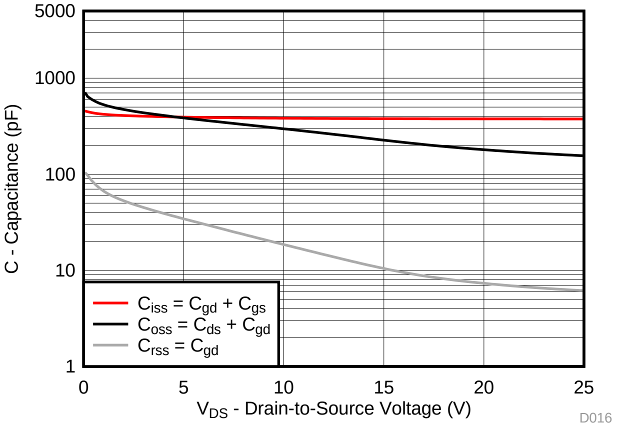


**図 14. Control MOSFET Capacitance**

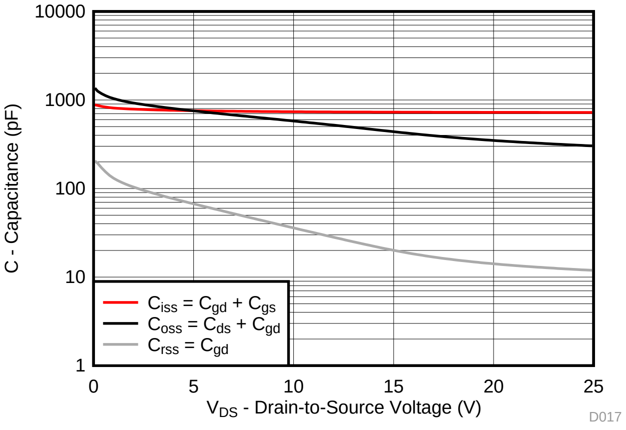
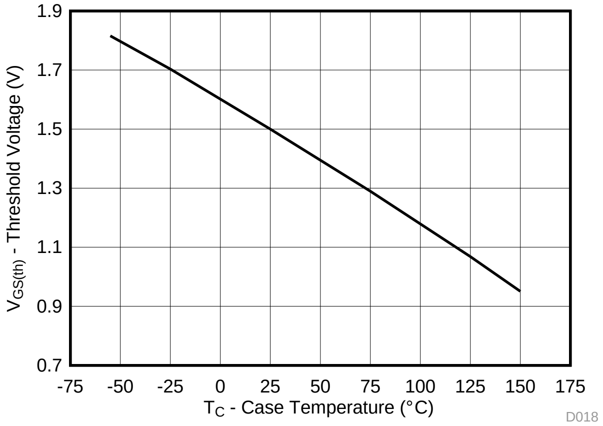
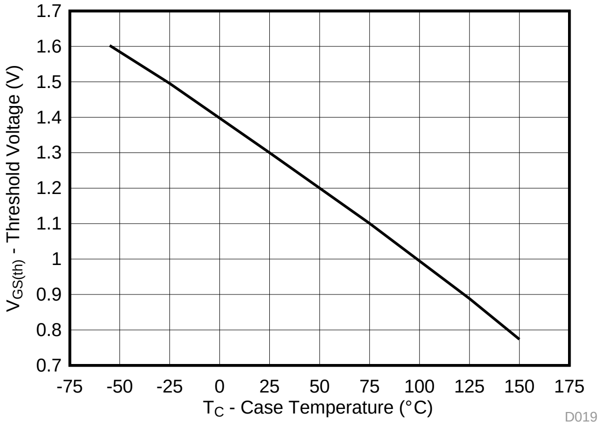


**図 15. Sync MOSFET Capacitance**



$I_D$ = 250 µA

**図 16. Control MOSFET $V_{GS(th)}$**



$I_D$ = 250 µA

**図 17. Sync MOSFET $V_{GS(th)}$**

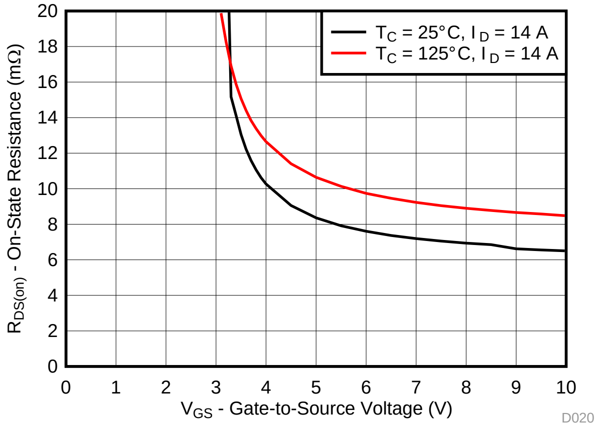


**図 18. Control MOSFET $R_{DS(on)}$ vs $V_{GS}$**

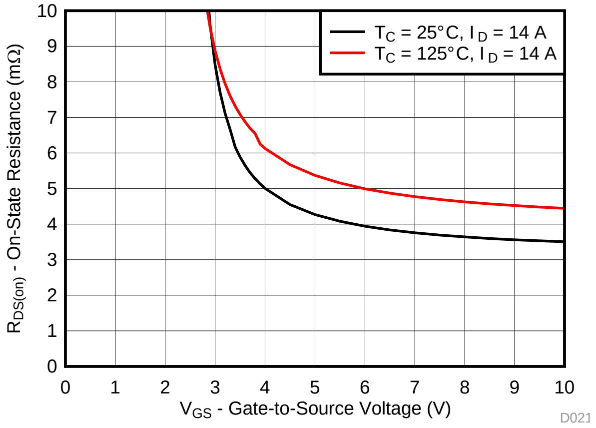
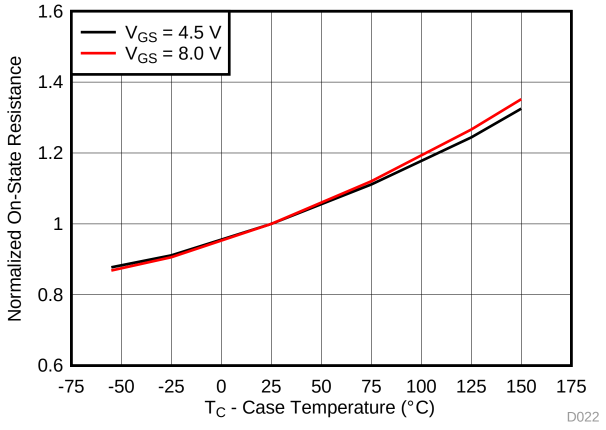


**図 19. Sync MOSFET $R_{DS(on)}$ vs $V_{GS}$**

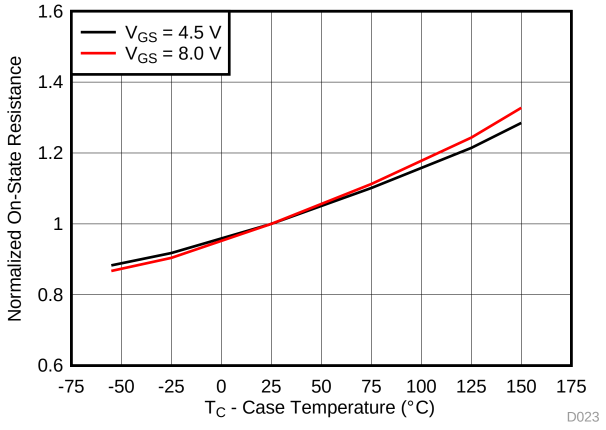
## Typical Power Block MOSFET Characteristics (continued)

$T_A$ = 25°C, unless stated otherwise.



$I_D$ = 14 A $V_{GS}$ = 4.5 V

**図 20. Control MOSFET Normalized $R_{DS(on)}$**



$I_D$ = 14 A $V_{GS}$ = 4.5 V

**図 21. Sync MOSFET Normalized $R_{DS(on)}$**

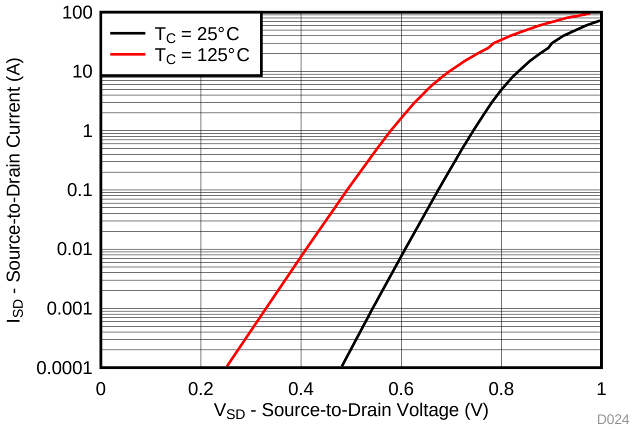


**図 22. Control MOSFET Body Diode**

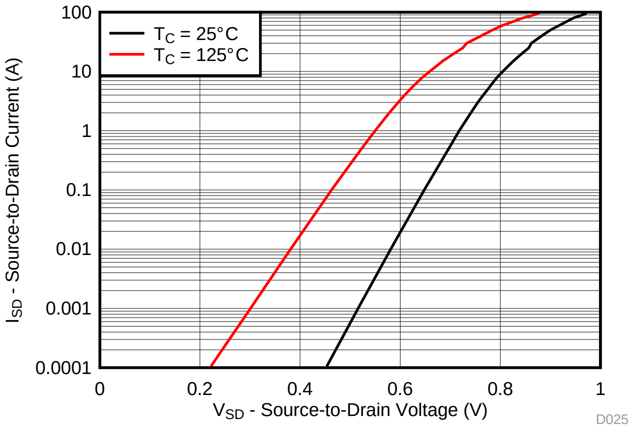


**図 23. Sync MOSFET Body Diode**

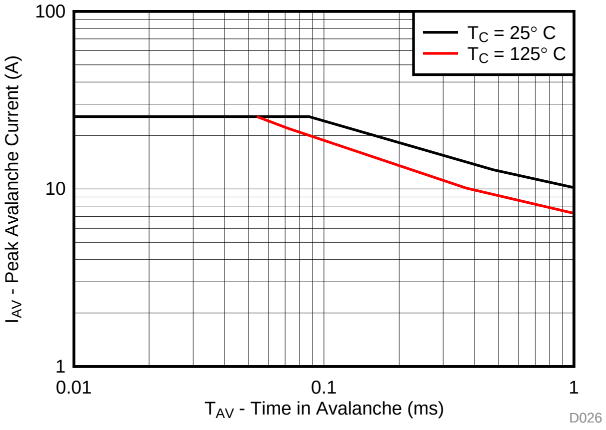


**図 24. Control MOSFET Unclamped Inductive Switching**

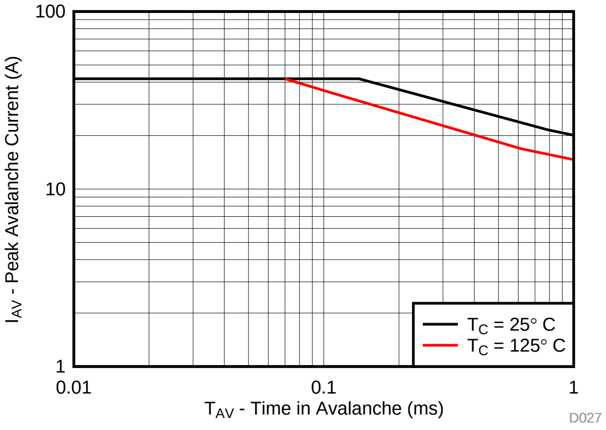


**図 25. Sync MOSFET Unclamped Inductive Switching**

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# 6 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 6.1 Application Information

### 6.1.1 Equivalent System Performance

Many of today's high-performance computing systems require low-power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's synchronous buck topology. In particular, there has been an emphasis in improving the performance of the critical power semiconductor in the power stage of this application (see 図 26). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

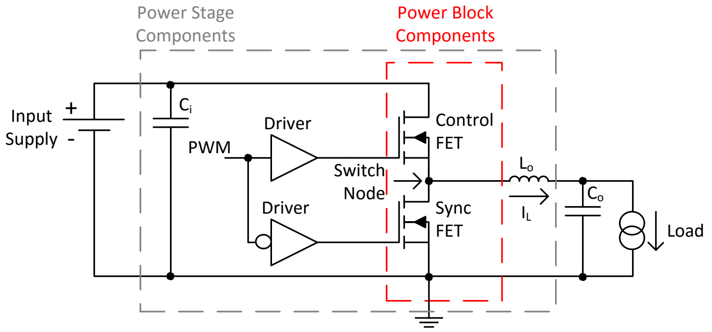

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**図 26. Synchronous Buck Topology**

The CSD86336Q3D is part of TI's power block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with $Q_{GD}$, $Q_{GS}$, and $Q_{RR}$. Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the control FET and sync FET connections (see 図 27). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in *Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters* (SLPA009).

## Application Information (continued)

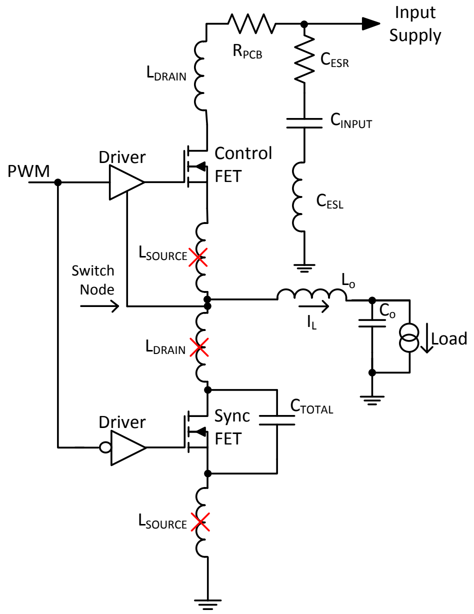

**図 27. Elimination of Common Source Inductance**

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. 図 28 and 図 29 compare the efficiency and power loss performance of the CSD86336Q3D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD86336Q3D clearly highlights the importance of considering the effective AC on-impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's power block technology.

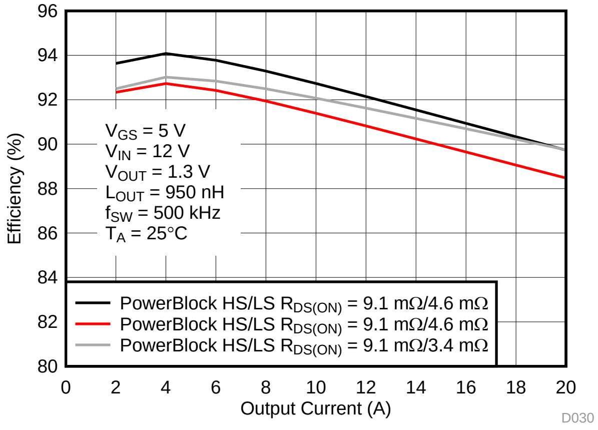

**図 28. Efficiency**

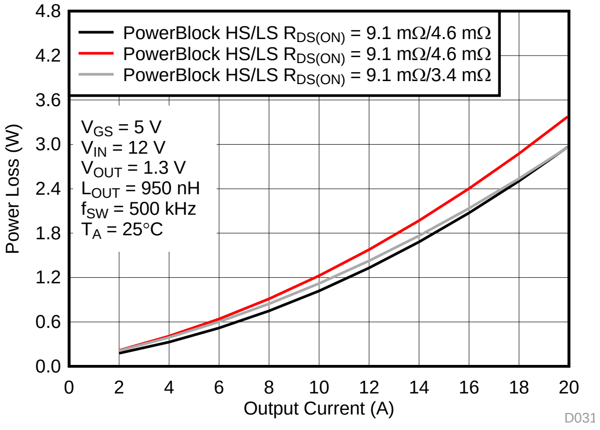

**図 29. Power Loss**

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## Application Information (continued)

表 1 compares the traditional DC measured $R_{DS(ON)}$ of CSD86336Q3D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's power block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to the $Z_{DS(ON)}$ value of CSD86336Q3D in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

**表 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$**

| PARAMETER | HS |  | LS |  |
|---|---|---|---|---|
|  | TYP | MAX | TYP | MAX |
| Effective AC on-impedance $Z_{DS(ON)}$ ($V_{GS}$ = 5 V) | 9.1 | — | 3.4 | — |
| DC measured $R_{DS(ON)}$ ($V_{GS}$ = 4.5 V) | 9.1 | 11.4 | 4.6 | 5.7 |

The CSD86336Q3D NexFET™ power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, safe operating area (SOA), and normalized graphs allow engineers to predict the product performance in the actual application.

### 6.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and $Q_{gd}$ are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. 図 1 plots the power loss of the CSD86336Q3D as a function of load current. This curve is measured by configuring and running the CSD86336Q3D as it would be in the final application (see 図 30). The measured power loss is the CSD86336Q3D loss and consists of both input conversion loss and gate drive loss. 式 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{power loss} \quad (1)$$

The power loss curve in 図 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

### 6.3 Safe Operating Area (SOA) Curves

The SOA curve in the CSD86336Q3D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. 図 3 outlines the temperature conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

### 6.4 Normalized Curves

The normalized curves in the CSD86336Q3D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

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## Normalized Curves (continued)

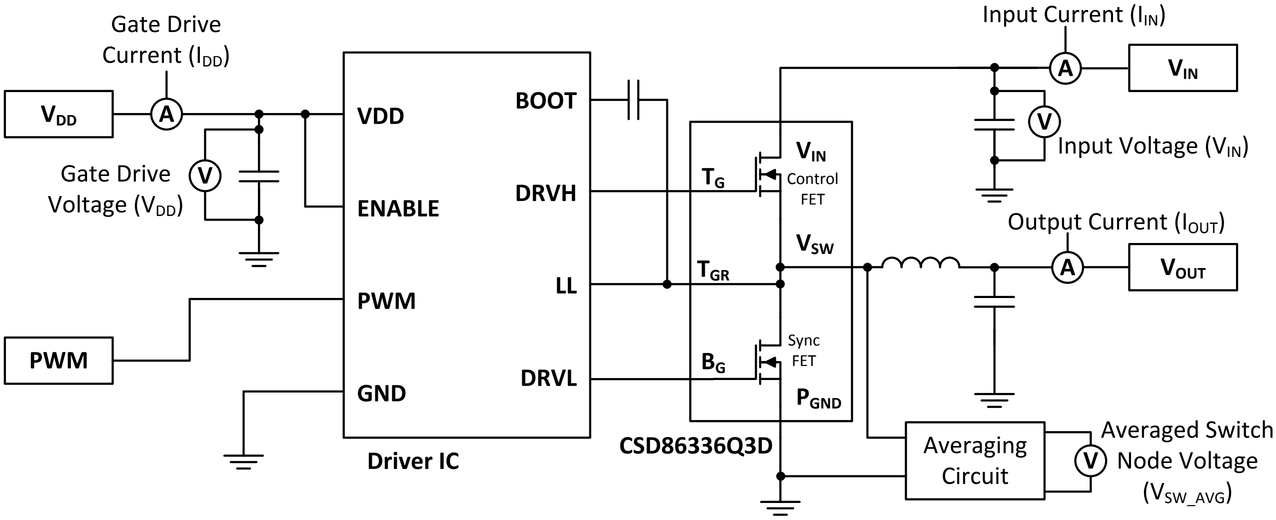

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図 30. Typical Application

## 6.5 Calculating Power Loss and Safe Operating Area (SOA)

The user can estimate power loss and SOA boundaries by arithmetic means (see *Design Example*). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

### 6.5.1 Design Example

Operating conditions:

- Output current = 18.0 A
- Input voltage = 5.0 V
- Output voltage = 1.8 V
- Switching frequency = 750 kHz
- Inductor = 290 nH

### 6.5.2 Calculating Power Loss

- Power loss at 18 A = 3.03 W (図 1)
- Normalized power loss for input voltage ≈ 1.1 (図 5)
- Normalized power loss for output voltage ≈ 1.07 (図 6)
- Normalized power loss for switching frequency ≈ 1.08 (図 4)
- Normalized power loss for output inductor ≈ 1.0 (図 7)
- **Final calculated power loss = 3.03 W × 1.1 × 1.07 × 1.08 × 1.0 ≈ 3.85 W**

### 6.5.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 1.0°C (図 5)
- SOA adjustment for output voltage ≈ 0.68°C (図 6)
- SOA adjustment for switching frequency ≈ 0.75°C (図 4)
- SOA adjustment for output inductor ≈ 0.02°C (図 7)
- **Final calculated SOA adjustment = 1.0 + 0.68 + 0.75 + 0.02 ≈ 2.45°C**

## Calculating Power Loss and Safe Operating Area (SOA) (continued)

In the design example above, the estimated power loss of the CSD86336Q3D would increase to 3.85 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 2.45°C. 図 31 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 2.45°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

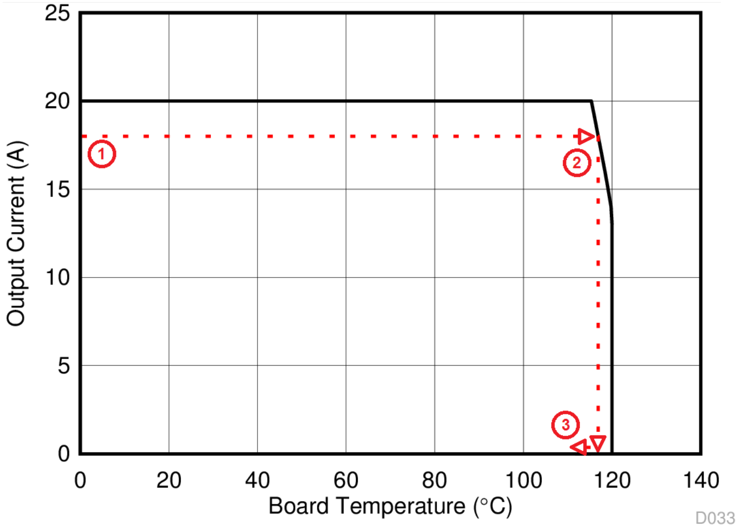

図 31. Power Block SOA

# 7 Layout

## 7.1 Recommended Schematic Overview

There are several critical components that must be used in conjunction with this power block device. 図 32 shows a portion of a schematic with the critical components needed for proper operation.

- C22: Bypass capacitor for $V_{IN}$ to help with ringing reduction
- C20: Bootstrap capacitor
- C21: Bypass capacitor for $V_{DD}$
- C7-C14: Bypass capacitors for $V_{IN}$ (minimum of 40 µF)
- C15: Electrolytic capacitor for $V_{IN}$
- R14, R16: Place holder for gate resistor (optional)
- R15: Place holder for bootstrap resistor (optional)
- R17, C16: Place holder for snubber (optional)

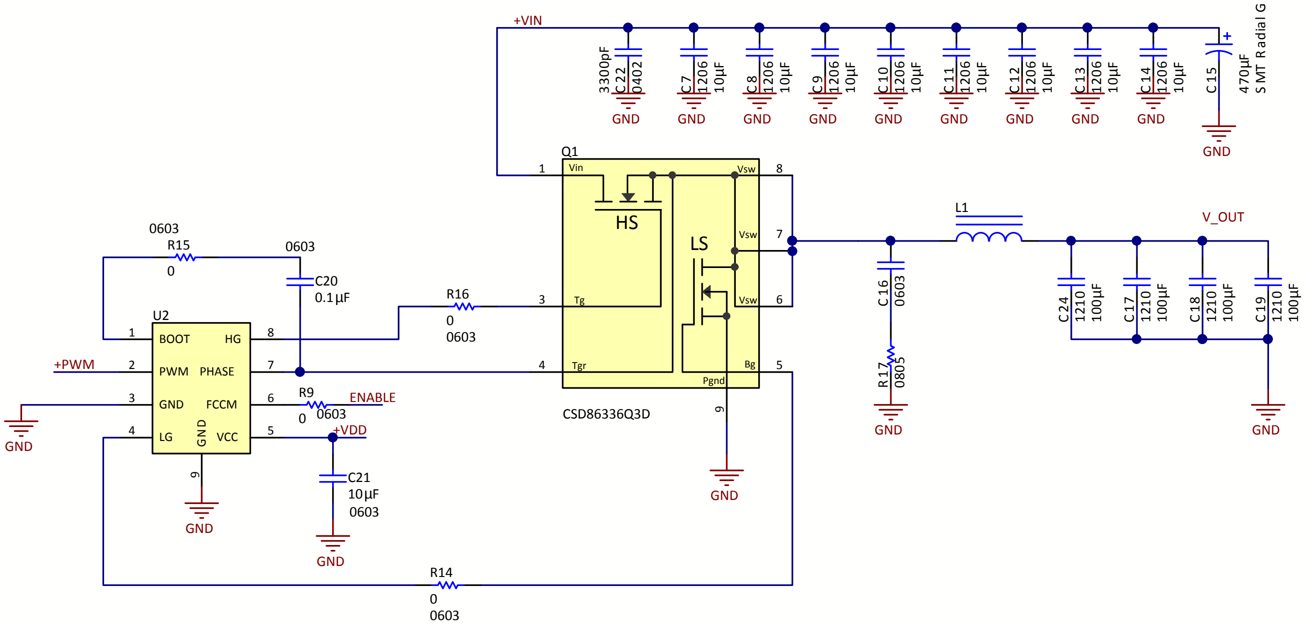

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**図 32. Recommended Schematic**

## 7.2 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter follows.

### 7.2.1 Electrical Performance

The power block has the ability to switch at voltage rates greater than 10 kV/µs. Special care must be taken with the PCB layout design and placement of the input capacitors, inductor, driver IC and output capacitors.

- The placement of the input capacitors relative to the power block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see 図 33). It is recommended that one 3.3-nF (or similar), 0402, 50-V ceramic capacitor be placed on the top side of the board as close as possible to VIN and PGND pins. In addition, a minimum of 40 µF of bulk ceramic capacitance should be placed as close as possible to the power block in a design. For high-density design, some of these ceramic capacitors can be placed on the bottom layer of PCB with appropriate number of vias interconnecting both layers.
- The driver IC should be placed relatively close to the power block gate pins. $T_G$ and $B_G$ should connect to the outputs of the driver IC. The $T_{GR}$ pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended boost resistor value will range between 1.0 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Please refer to *Snubber Circuits: Theory, Design and Application* (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the VSW node and PGND (see 図 33 and 図 34).(1)

---

(1) Keong W. Kam, David Pommerenke, “EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis”, University of Missouri – Rolla

## Recommended PCB Design Overview (continued)

### 7.2.2 Thermal Performance

The power block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The examples in 図 33 and 図 34 use vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user’s PCB design rules and manufacturing capabilities.

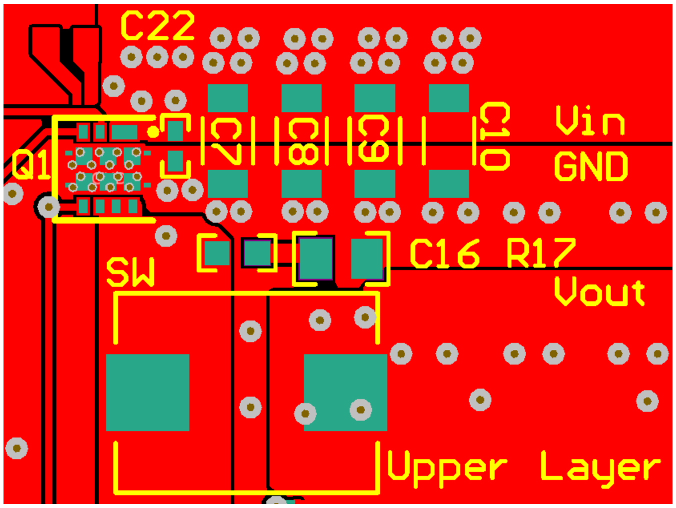

図 33. Recommended PCB Layout (Top Down View)

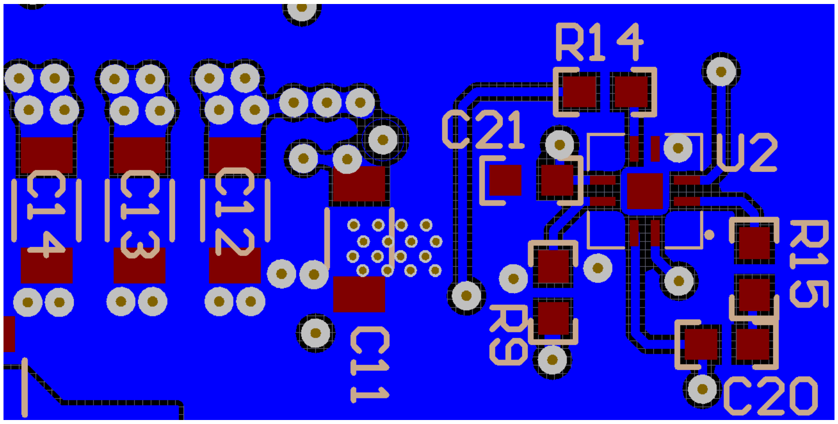

図 34. Recommended PCB Layout (Bottom View)

# 8 デバイスおよびドキュメントのサポート

## 8.1 ドキュメントの更新通知を受け取る方法

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## 8.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**設計サポート** ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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## 8.5 Glossary

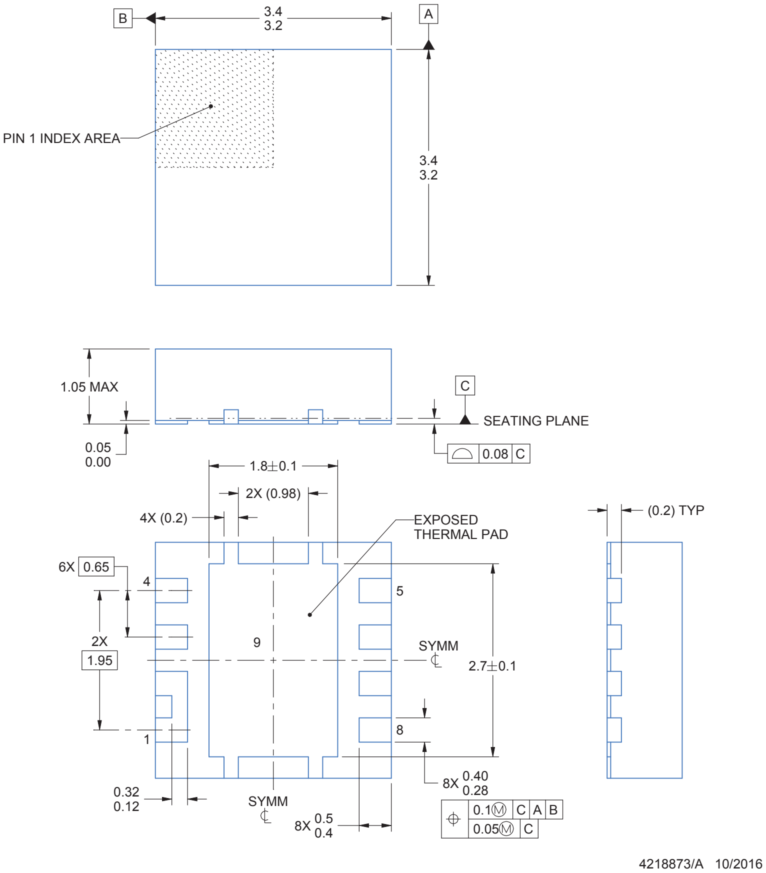
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## 9.1 Q3Dパッケージの寸法



1. すべての直線寸法はミリメートル(mm)単位です。括弧内のすべての寸法は、参照のみを目的としたものです。寸法と許容誤差は、ASME Y14.5M準拠です。
2. この図面は、予告なく変更される可能性があります。
3. 最良の熱特性および機械的な性能を実現するため、パッケージのサーマル・パッドはプリント基板にハンダ付けする必要があります。

## 9.2 ピン構成

| 位置 | 機能 |
|---|---|
| ピン1 | $V_{IN}$ |
| ピン2 | $V_{IN}$ |
| ピン3 | $T_G$ |
| ピン4 | $T_{GR}$ |
| ピン5 | $B_G$ |
| ピン6 | $V_{SW}$ |
| ピン7 | $V_{SW}$ |
| ピン8 | $V_{SW}$ |
| ピン9 | $P_{GND}$ |

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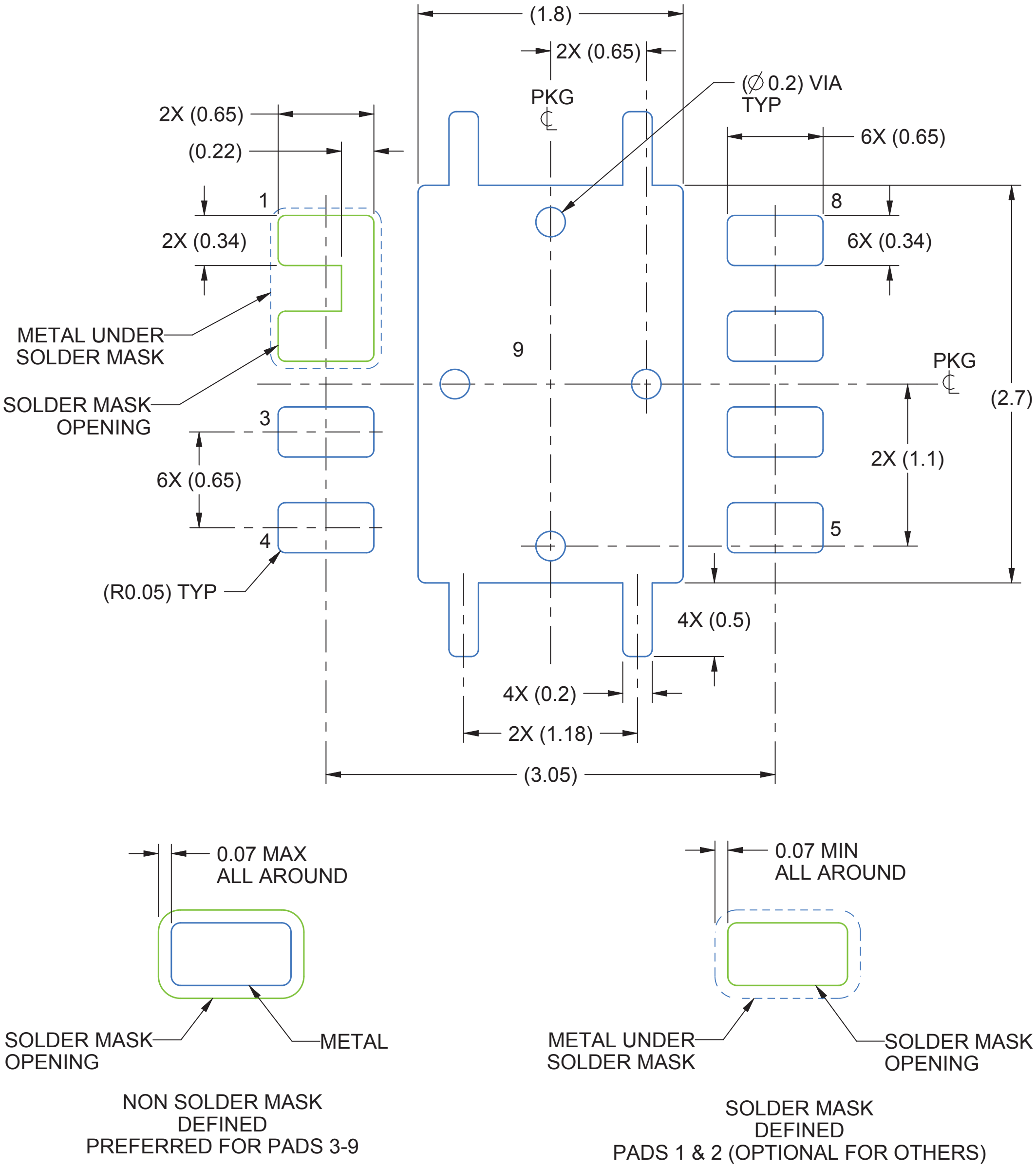
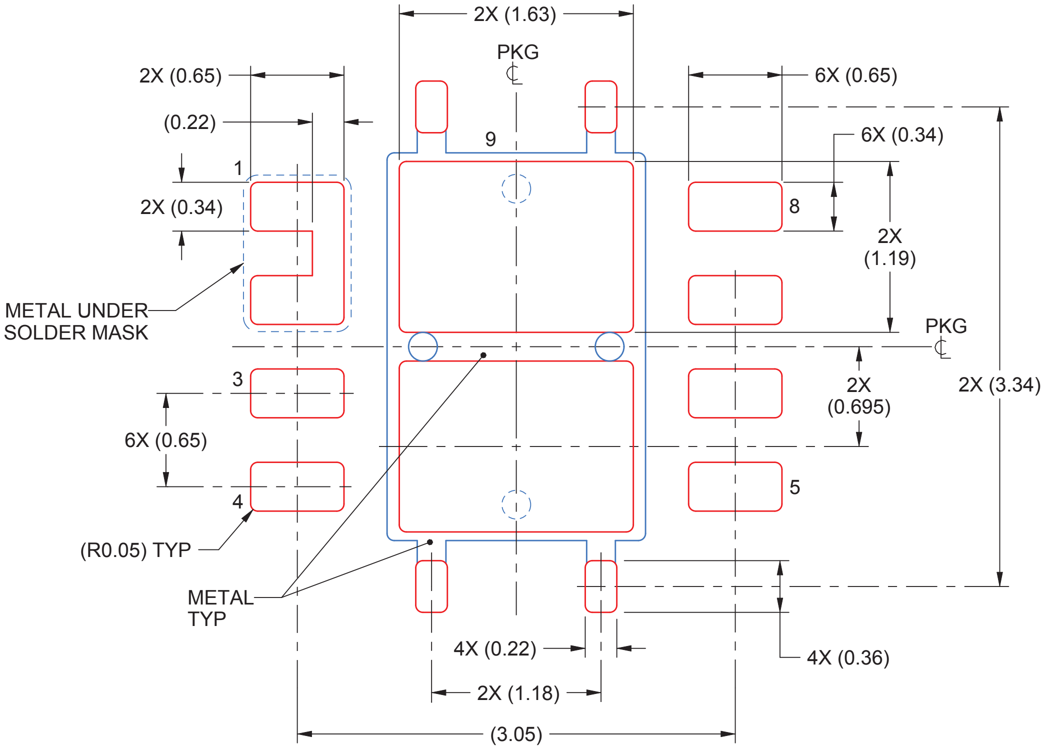
## 9.3 推奨ランド・パターン



1. すべての直線寸法はミリメートル(mm)単位です。括弧内のすべての寸法は、参照のみを目的としたものです。寸法と許容誤差は、ASME Y14.5M準拠です。
2. このパッケージは、基板上のサーマル・パッドにハンダ付けされるよう設計されています。詳細については、*『QFN/SON PCBアタッチメント』*(SLUA271)を参照してください。
3. ビアはアプリケーションに応じてのオプションです。デバイスのデータシートを参照してください。一部またはすべてを実装する場合に推奨されるビアの場所が示されています。

## 9.4 推奨ステンシル



1. すべての直線寸法はミリメートル(mm)単位です。括弧内のすべての寸法は、参照のみを目的としたものです。寸法と許容誤差は、ASME Y14.5M準拠です。
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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD86336Q3D | ACTIVE | VSON-CLIP | DPB | 8 | 2500 | RoHS-Exempt & Green | SN | Level-1-260C-UNLIM | -55 to 150 | 86336D | Samples |
| CSD86336Q3DT | ACTIVE | VSON-CLIP | DPB | 8 | 250 | RoHS-Exempt & Green | SN | Level-1-260C-UNLIM | -55 to 150 | 86336D | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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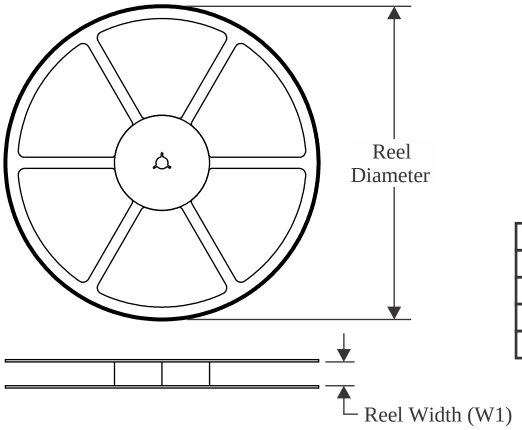
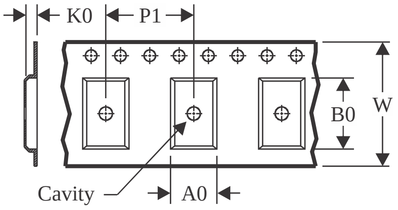
REEL DIMENSIONS

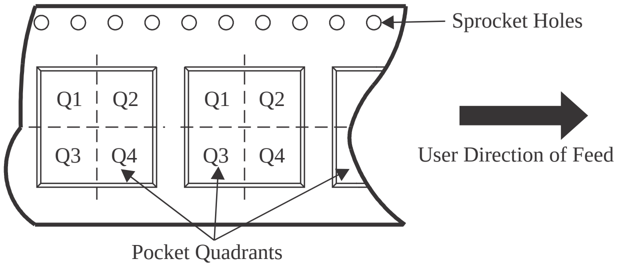


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

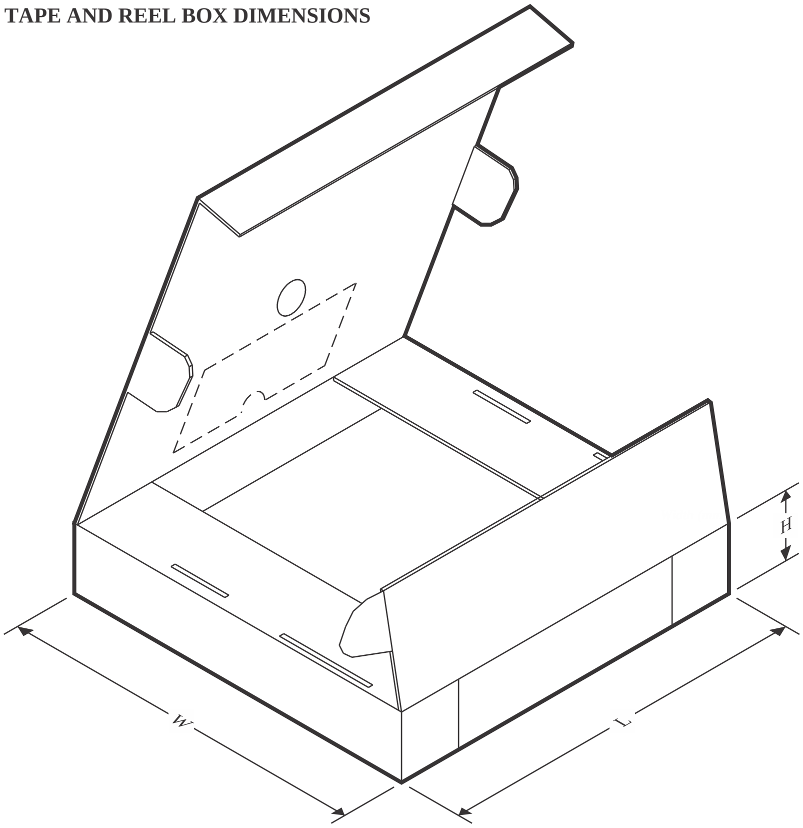
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

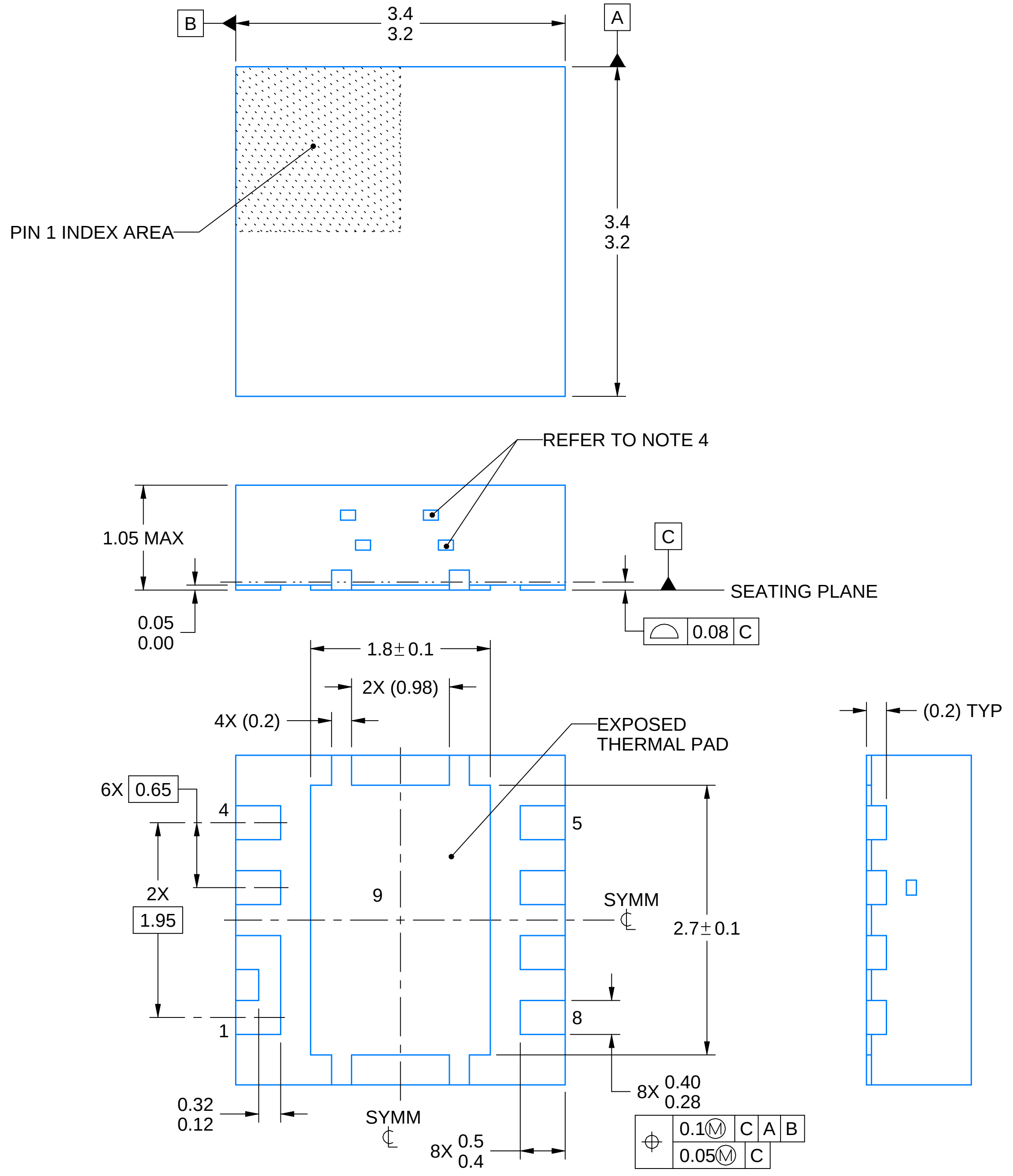
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD86336Q3D | VSON-CLIP | DPB | 8 | 2500 | 330.0 | 12.4 | 3.6 | 3.6 | 1.2 | 8.0 | 12.0 | Q1 |
| CSD86336Q3DT | VSON-CLIP | DPB | 8 | 250 | 330.0 | 12.4 | 3.6 | 3.6 | 1.2 | 8.0 | 12.0 | Q1 |

## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD86336Q3D | VSON-CLIP | DPB | 8 | 2500 | 336.6 | 336.6 | 41.3 |
| CSD86336Q3DT | VSON-CLIP | DPB | 8 | 250 | 336.6 | 336.6 | 41.3 |



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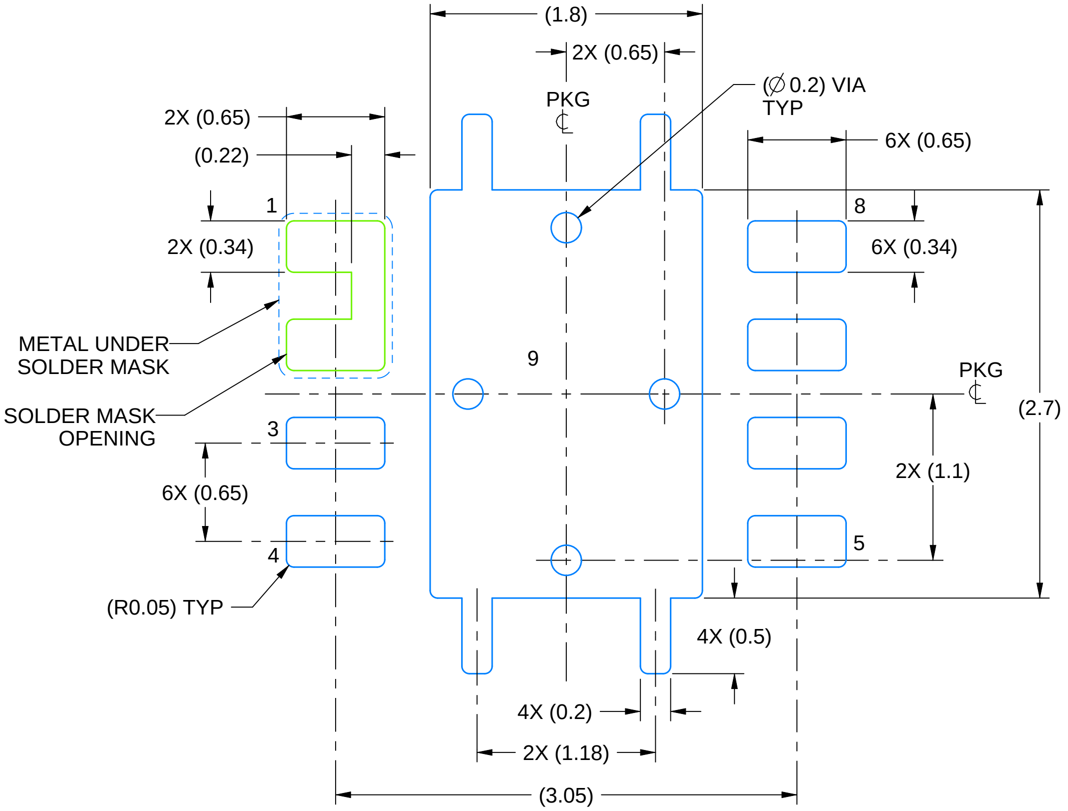
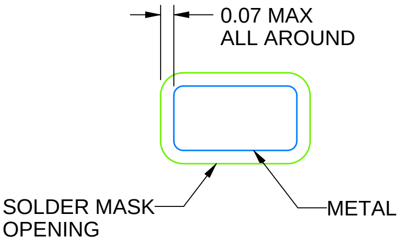
NOTES:

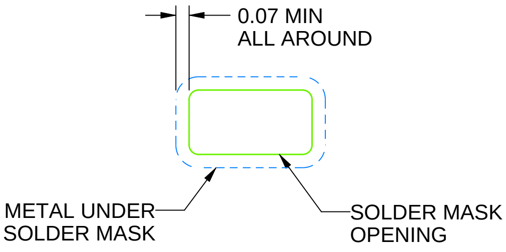
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance
4. Exposed metals on side wall may vary & not visible.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
PREFERRED FOR PADS 3-9



SOLDER MASK
DEFINED
PADS 1 & 2 (OPTIONAL FOR OTHERS)

SOLDER MASK DETAILS

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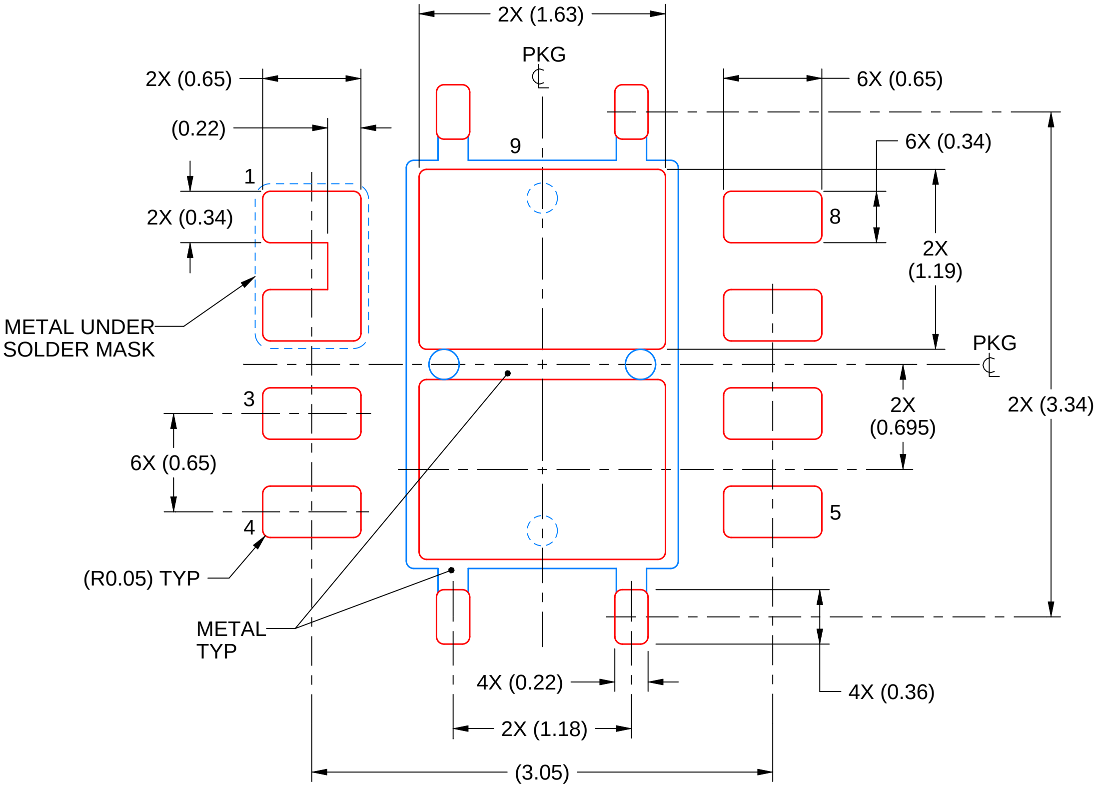
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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