

## CSD13380F3 12V N チャネル FemtoFET™ MOSFET

### 1 特長

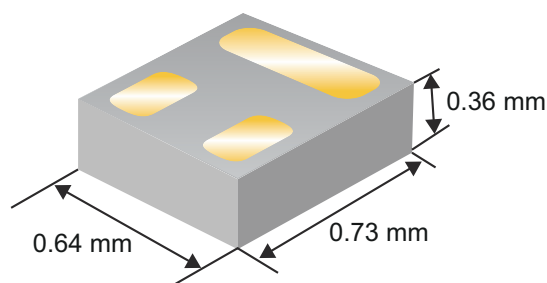
- 低いオン抵抗
- 非常に低い  $Q_g$  および  $Q_{gd}$
- 大きな動作時ドレイン電流
- 極めて小さいフットプリント
  - $0.73\text{mm} \times 0.64\text{mm}$
- 薄型
  - 最大高  $0.36\text{mm}$
- ESD 保護ダイオード搭載
  - HBM 定格  $3\text{kV}$  超
  - CDM 定格  $2\text{kV}$  超
- 鉛およびハロゲン不使用
- RoHS 準拠

### 2 アプリケーション

- ロード・スイッチ・アプリケーションに最適
- 汎用スイッチング・アプリケーションに最適
- バッテリー・アプリケーション
- ハンドヘルドおよびモバイル・アプリケーション

### 3 概要

この  $63\text{m}\Omega$ 、 $12\text{V}$  N チャネル FemtoFET™ MOSFET は、さまざまなハンドヘルドおよびモバイル・アプリケーション向けに、フットプリントを最小化するように設計され、最適化されています。標準の小信号 MOSFET をこのテクノロジーに置き換えて、フットプリントを大幅に減らすことができます。



標準的な部品寸法

### 製品概要

$T_A = 25^\circ\text{C}$		標準値	単位
$V_{DS}$	ドレイン - ソース間電圧	12	V
$Q_g$	ゲートの合計電荷 (4.5V)	0.91	nC
$Q_{gd}$	ゲート電荷、ゲート - ドレイン間	0.15	nC
$R_{DS(on)}$	ドレイン - ソース間オン抵抗	$V_{GS} = 1.8\text{V}$	96
		$V_{GS} = 2.5\text{V}$	73
		$V_{GS} = 4.5\text{V}$	63
$V_{GS(th)}$	スレッショルド電圧	0.85	V

### 製品情報(1)

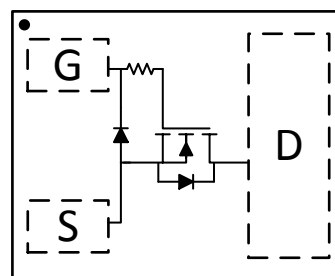
デバイス	数量	メディア	パッケージ	出荷形態
CSD13380F3	3000	7 インチ・リール	Femto $0.73\text{mm} \times 0.64\text{mm}$ LGA (Land Grid Array)	テープ および リール
CSD13380F3T	250			

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 絶対最大定格

$T_A = 25^\circ\text{C}$ (特に記述のない限り)		値	単位
$V_{DS}$	ドレイン - ソース間電圧	12	V
$V_{GS}$	ゲート - ソース間電圧	8	V
$I_D$	連続ドレイン電流(1)	3.6	A
	連続ドレイン電流(2)	2.1	
$I_{DM}$	パルス・ドレイン電流(2) (3)	13.5	A
$P_D$	消費電力(1)	1.4	W
	消費電力(2)	0.5	
$V_{(ESD)}$	人体モデル (HBM)	3	kV
	デバイス帯電モデル (CDM)	2	
$T_J$ , $T_{stg}$	動作時の接合部温度、 保存温度	$-55 \sim 150$	$^\circ\text{C}$

- (1)  $R_{\theta JA} = 90^\circ\text{C}/\text{W}$  (標準値、最大 Cu: 厚さ  $0.06$  インチ ( $1.52\text{mm}$ ) の FR4 PCB 上の面積  $1$  平方インチ ( $6.45\text{cm}^2$ )、厚さ  $2\text{oz}$  ( $0.071\text{mm}$ ) の Cu パッドに実装した場合)
- (2)  $R_{\theta JA} = 255^\circ\text{C}/\text{W}$  (標準値、最小 Cu: 最小限の Cu 取り付け領域を持つ基板に実装した場合)
- (3) パルス幅  $\leq 100\mu\text{s}$ 、デューティ・サイクル  $\leq 1\%$



上面図



## Table of Contents

<b>1 特長</b> .....	<b>1</b>	<b>6 Device and Documentation Support</b> .....	<b>7</b>
<b>2 アプリケーション</b> .....	<b>1</b>	6.1 Receiving Notification of Documentation Updates.....	7
<b>3 概要</b> .....	<b>1</b>	6.2 Trademarks.....	7
<b>4 Revision History</b> .....	<b>2</b>	<b>7 Mechanical, Packaging, and Orderable Information</b> ...8	
<b>5 Specifications</b> .....	<b>3</b>	7.1 Mechanical Dimensions.....	8
5.1 Electrical Characteristics.....	3	7.2 Recommended Minimum PCB Layout.....	9
5.2 Thermal Information.....	3	7.3 Recommended Stencil Pattern.....	9
5.3 Typical MOSFET Characteristics.....	4		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision * (October 2016) to Revision A (February 2022)</b>	<b>Page</b>
• 超薄型の簡条書き項目を、高さ 0.35mm から 0.36mm に変更。.....	1
• 超薄型の画像の高さを 0.35mm から 0.36mm に更新。.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	8
• Added FemtoFET Surface Mount Guide note.....	9

## 5 Specifications

### 5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	12			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 9.6\text{ V}$			50	nA
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 8\text{ V}$			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.55	0.85	1.30	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 1.8\text{ V}, I_{DS} = 0.1\text{ A}$		96	135	m $\Omega$
		$V_{GS} = 2.5\text{ V}, I_{DS} = 0.4\text{ A}$		73	92	
		$V_{GS} = 4.5\text{ V}, I_{DS} = 0.4\text{ A}$		63	76	
$g_{fs}$	Transconductance	$V_{DS} = 1.2\text{ V}, I_{DS} = 0.4\text{ A}$		4.3		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 6\text{ V},$ $f = 1\text{ MHz}$		120	156	pF
$C_{oss}$	Output capacitance			81	105	pF
$C_{riss}$	Reverse transfer capacitance			9.6	12.5	pF
$R_G$	Series gate resistance			16		$\Omega$
$Q_g$	Gate charge total (4.5 V)	$V_{DS} = 6\text{ V}, I_{DS} = 0.4\text{ A}$		0.91	1.2	nC
$Q_{gd}$	Gate charge gate-to-drain			0.15		nC
$Q_{gs}$	Gate charge gate-to-source			0.19		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			0.15		nC
$Q_{oss}$	Output charge	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$		0.81		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V},$ $I_{DS} = 0.4\text{ A}, R_G = 2\ \Omega$		4		ns
$t_r$	Rise time			4		ns
$t_{d(off)}$	Turnoff delay time			11		ns
$t_f$	Fall time			3		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 0.4\text{ A}, V_{GS} = 0\text{ V}$		0.71	1	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 6\text{ V}, I_F = 0.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		2.1		nC
$t_{rr}$	Reverse recovery time			8		ns

### 5.2 Thermal Information

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

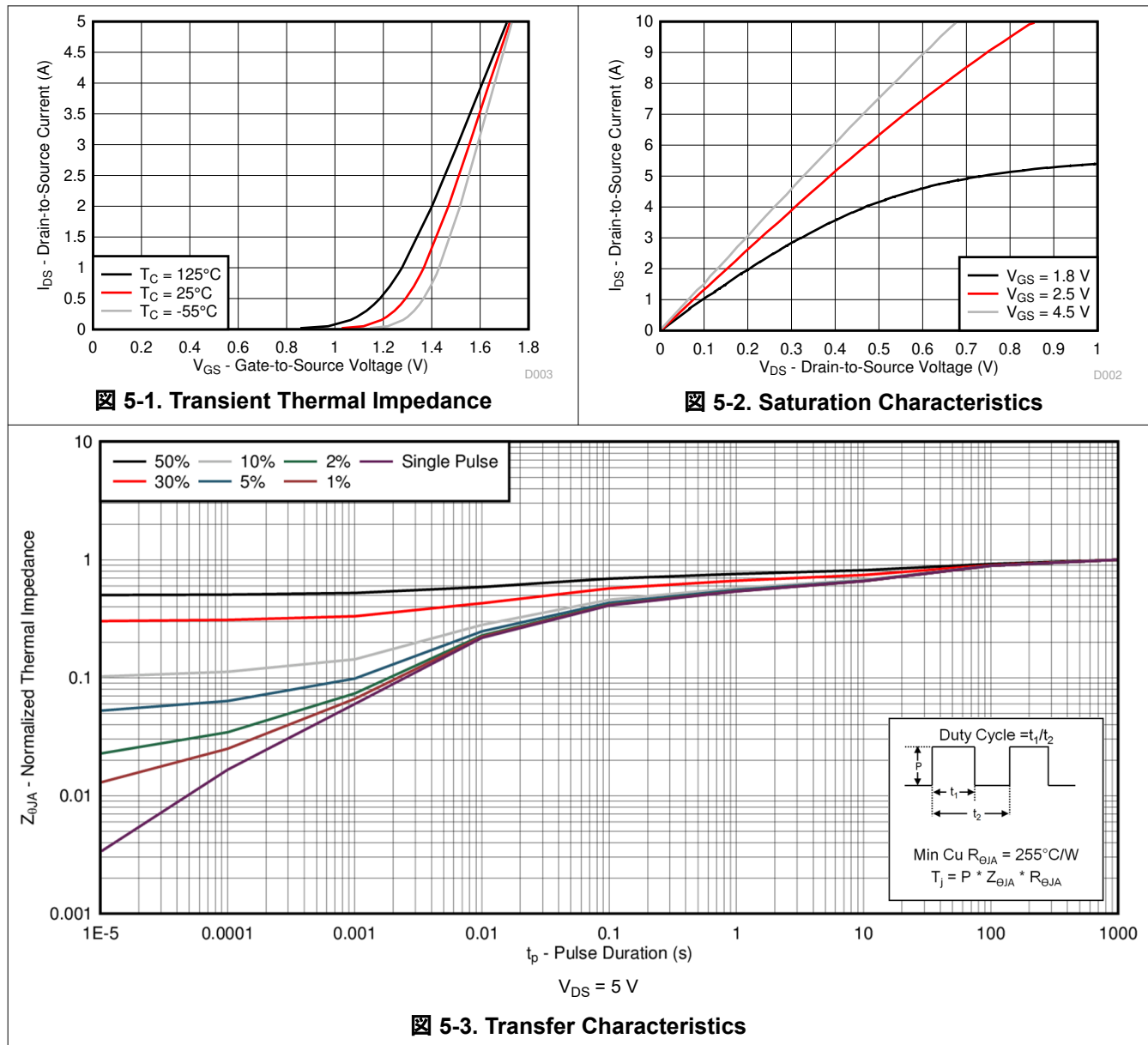
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>		90		$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance <sup>(2)</sup>		255		

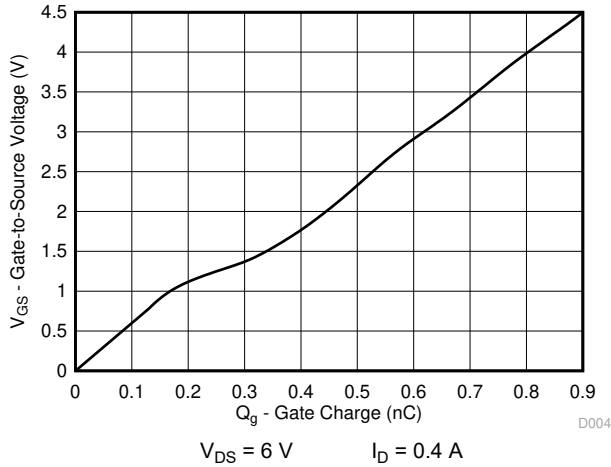
(1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

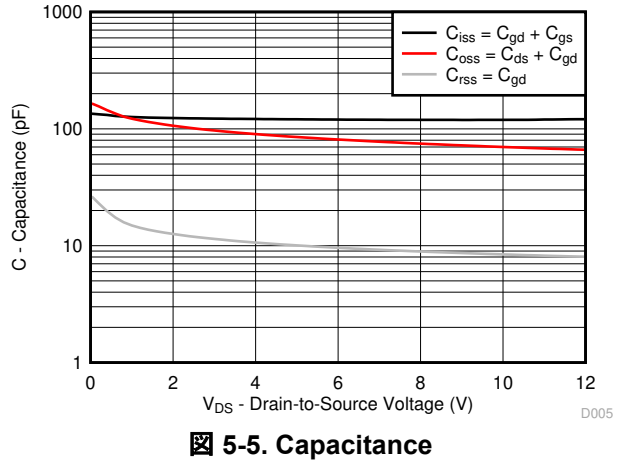
### 5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

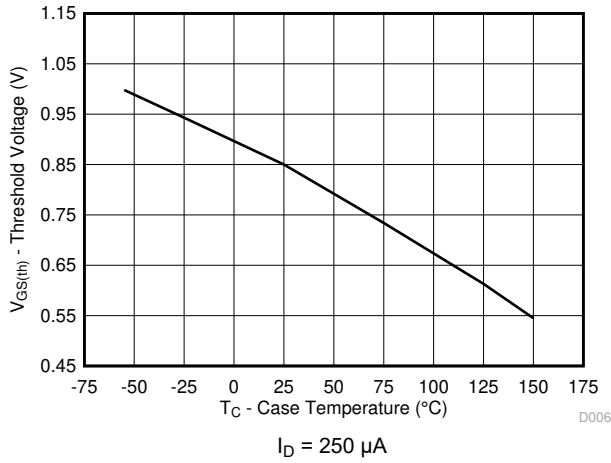




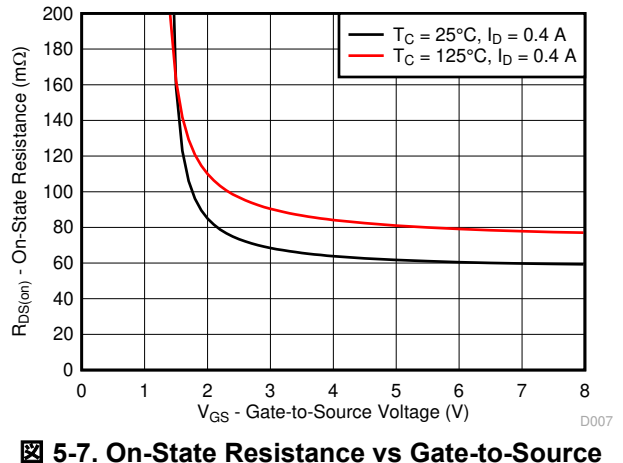
**5-4. Gate Charge**



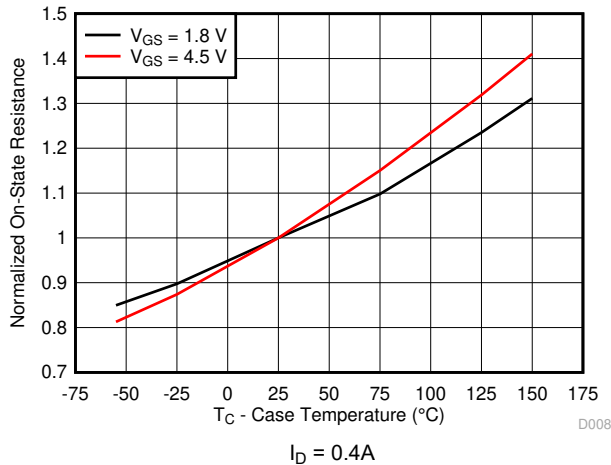
**5-5. Capacitance**



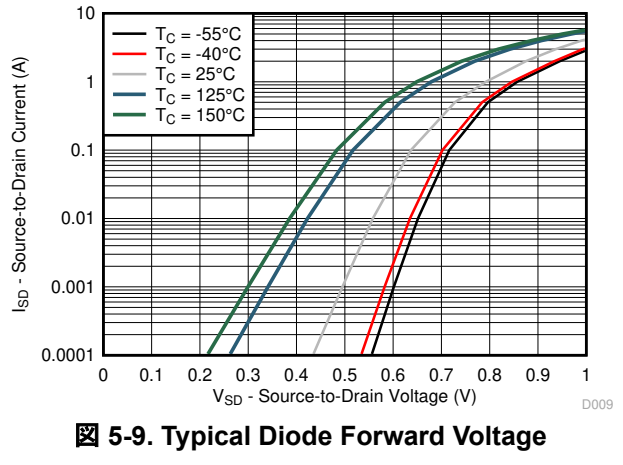
**5-6. Threshold Voltage vs Temperature**



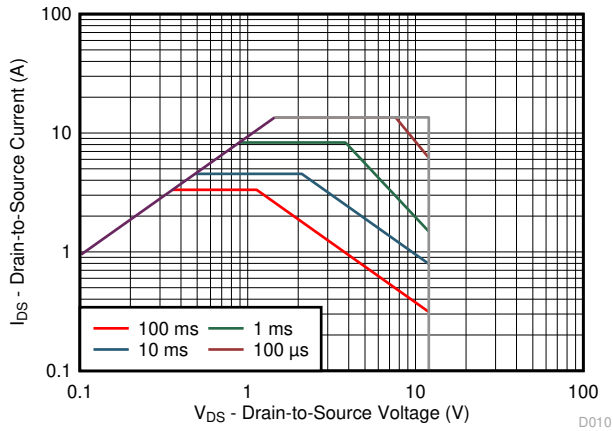
**5-7. On-State Resistance vs Gate-to-Source Voltage**



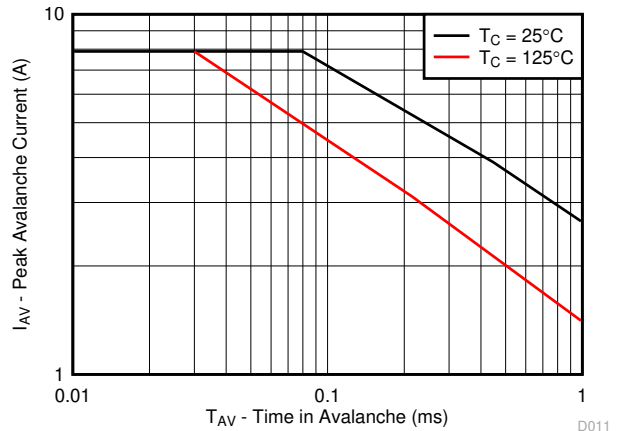
**5-8. Normalized On-State Resistance vs Temperature**



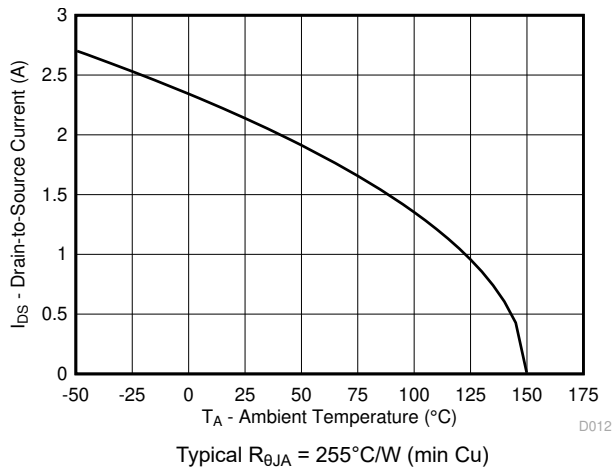
**5-9. Typical Diode Forward Voltage**



**5-10. Maximum Safe Operating Area**



**5-11. Single Pulse Unclamped Inductive Switching**



**5-12. Maximum Drain Current vs Temperature**

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Trademarks

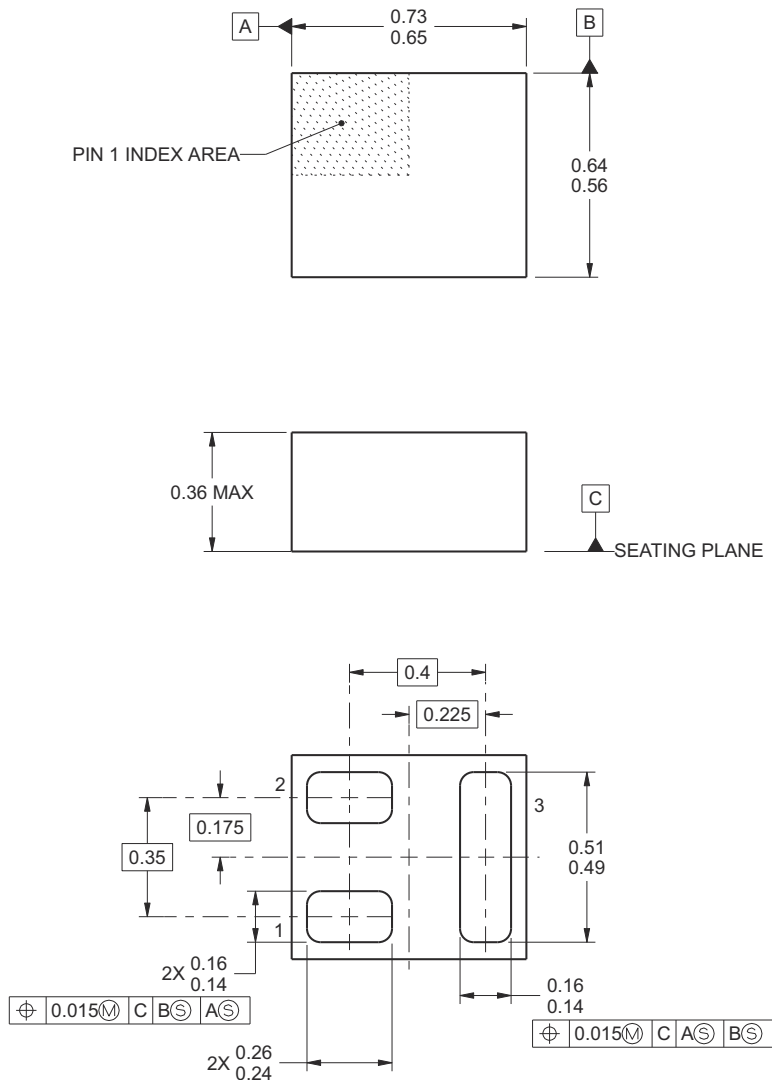
FemtoFET™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Mechanical Dimensions



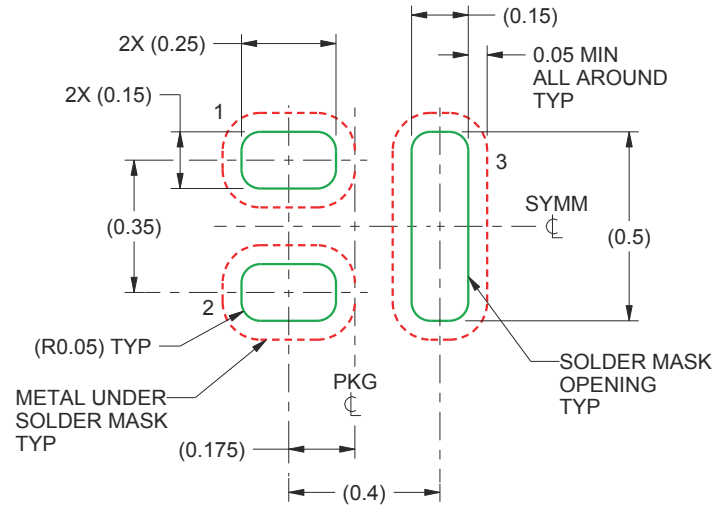
- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a PB-free solder land design.

**表 7-1. Pin Configuration**

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

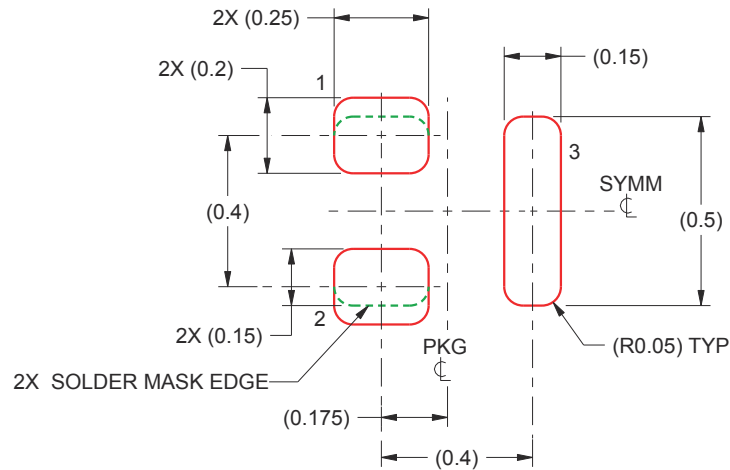


## 7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- A. For more information, see [FemtoFET Surface Mount Guide \(SLRA003D\)](#).

## 7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13380F3	ACTIVE	PICOSTAR	YJM	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	D	<a href="#">Samples</a>
CSD13380F3T	ACTIVE	PICOSTAR	YJM	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	D	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

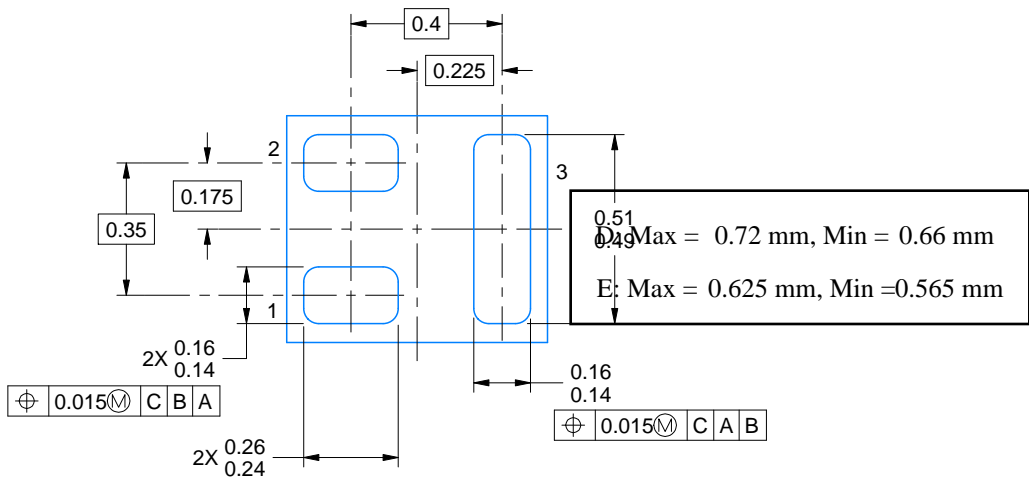
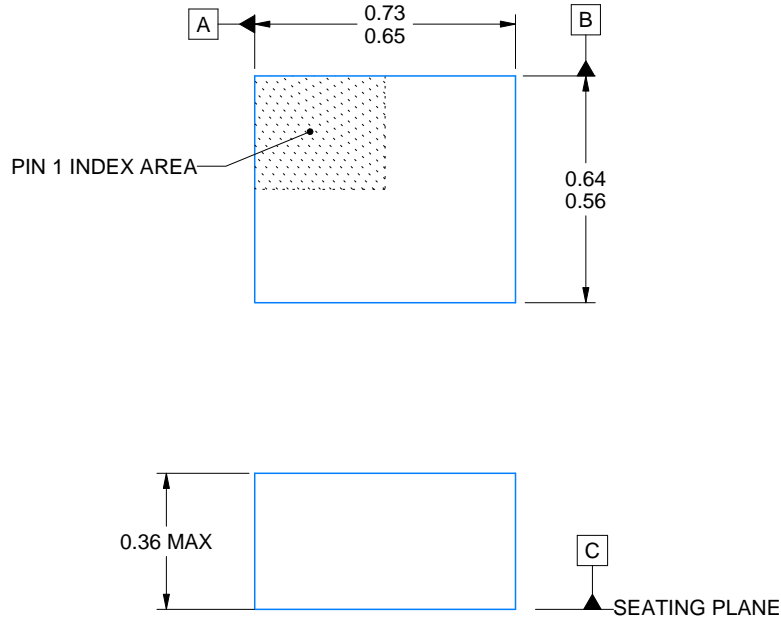
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13380F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD13380F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13380F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD13380F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0



4222304/B 03/2022

NOTES:

PicoStar is a trademark of Texas Instruments.

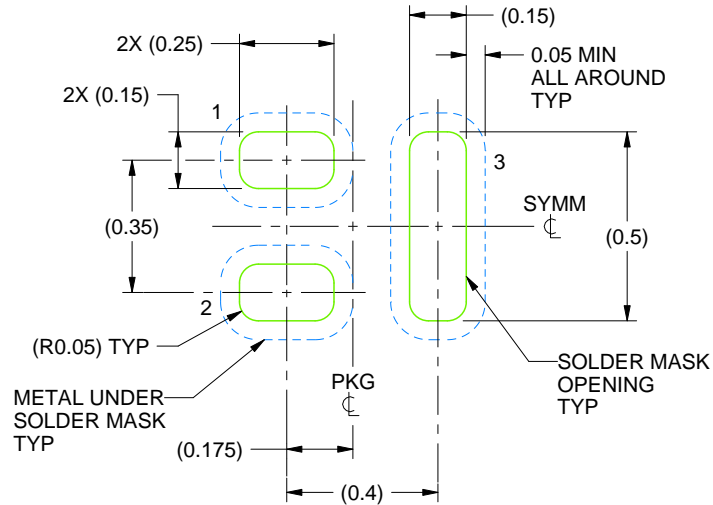
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

# EXAMPLE BOARD LAYOUT

YJM0003A

PicoStar™ - 0.36 mm max height

PicoStar™

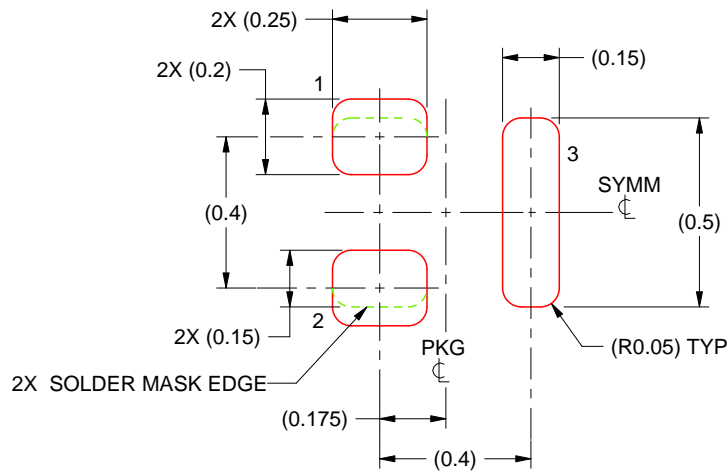


LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).



**SOLDER PASTE EXAMPLE**  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated