

CD4027B CMOS デュアル J-K フリップ・フロップ

1 特長

- セット・リセット機能
- 静的フリップ・フロップ動作: クロックが **HIGH** または **LOW** レベルの間は状態を継続して維持
- 中程度の速度での動作: 10V で 16MHz (標準値) のクロック・トグル・レート
- 標準化された対称出力特性
- 20V で静止電流を 100% テスト済み
- パッケージの温度範囲全体にわたって 18V 時に最大入力電流 1 μ A、25°C では 18V 時に 100nA
- ノイズ・マージン (パッケージの全温度範囲にわたって):
 - $V_{DD} = 5V$ で 1V
 - $V_{DD} = 10V$ で 2V
 - $V_{DD} = 15V$ で 2.5V
- 5V、10V、15V のパラメータ定格
- JEDEC 暫定標準 No. 138 『standard specifications for description of 'B' series CMOS devices』のすべての要求事項に適合

2 アプリケーション

- レジスタ、カウンタ、制御回路

3 概要

CD4027B は、2 つの同一の相補対称型 J-K フリップ・フロップを搭載した、シングル・モノリシック・チップ IC です。各フリップ・フロップは、J、K、セット、リセット、クロックの入力信号を備えています。バッファ付きの Q 信号および \bar{Q} 信号を出力として備えています。この入出力構成により、RCA-CD4013B デュアル D タイプ・フリップ・フロップとの共存動作が可能です。

CD4027B は、制御、レジスタ、トグルの機能を実行するときに便利です。J および K 入力のロジック・レベルと、内部の自己制御によって各フリップ・フロップの状態が決まります。フリップ・フロップの状態は、クロック・パルスの立ち上がり時に同期して変化します。セットおよびリセット機能は、クロックとは独立しており、セットまたはリセット入力に **HIGH** レベル信号が印加されたときに動作を開始します。

CD4027B タイプは、16 リードのハーメチック・デュアル・インライン・セラミック・パッケージ (F3A サフィックス)、16 リードのデュアル・インライン・プラスチック・パッケージ (E サフィックス)、16 リードのスマート・アウトライン・パッケージ (M、M96、MT、NSR サフィックス)、16 リードのシン・シュリンク・スマート・アウトライン・パッケージ (PW および PWR サフィックス) で供給されます。

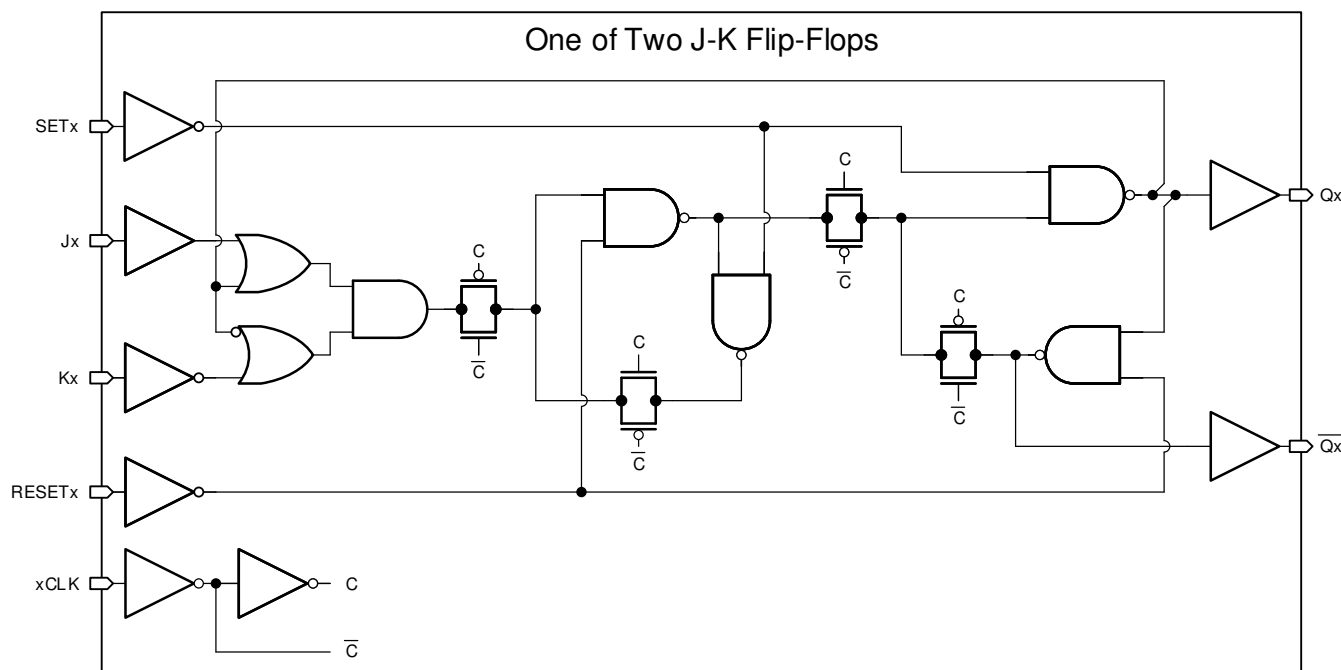


図 3-1. ロジック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2003) to Revision D (July 2021)

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5 Pin Configuration and Functions

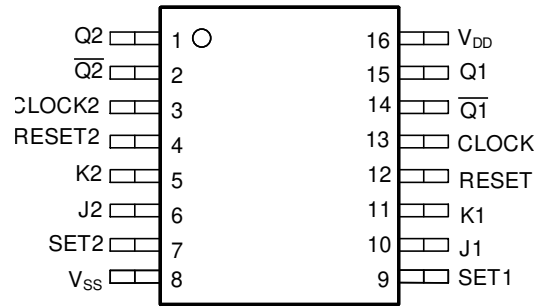


图 5-1. Terminal Assignment

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK1	13	I	Clock input for channel 1
CLOCK2	3	I	Clock input for channel 2
J1	10	I	J input for channel 1
J2	6	I	J input for channel 2
K1	11	I	K input for channel 1
K2	5	I	K input for channel 2
Q1	15	O	Q output for channel 1
Q1	14	O	Inverted Q output for channel 1
Q2	1	O	Q output for channel 2
Q2	2	O	Inverted Q output for channel 2
RESET1	12	I	Reset input for channel 1
RESET2	4	I	Reset input for channel 2
SET1	9	I	Set input for channel 1
SET2	7	I	Set input for channel 2
V _{DD}	16	—	Supply
V _{SS}	8	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V _{DD}	DC Supply Voltage Range	Voltages referenced to V _{SS} Terminal	-0.5	20	V
All Inputs	Input Voltage Range		-0.5	V _{DD} + 0.5	V
Any One Input	DC Input Current			±10	mA
P _D	Power Dissipation per Package	For T _A = -55°C to +100°C		500	mW
		For T _A = +100°C to +125°C	12mW/°C	200	mW
	Device Dissipation per Output Transistor	For T _A = Full package-temperature range (all package types)		100	mW
T _A	Operating- Temperature Range		-55	125	°C
T _{stg}	Storage temperature		-65	150	°C
	Lead Temperature (During Soldering)	At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max		265	°C

6.2 Recommended Operating Conditions

at T_A = 25°C, except as noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC			V _{DD} (V)	LIMITS		UNIT
				ALL PACKAGES		
				MIN	MAX	
	Supply-Voltage Range	For T _A = Full Package Temperature Range		3	18	V
t _S	Data Setup Time		5	200		ns
			10	75		
			15	50		
t _W	Clock Pulse Width		5	140		ns
			10	60		
			15	40		
f _{CL}	Clock Input Frequency (Toggle Mode)		5	3.5		MHz
			10	dc	8	
			15		12	
t _{rCL} , t _{fCL} ⁽¹⁾	Clock Rise or Fall Time		5	45		µs
			10	5		
			15	2		
t _W	Set or Reset Pulse Width		5	180		ns
			10	80		
			15	50		

- (1) If more than one unite is cascaded in a parallel clocked operation, t_{rCL} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

6.3 Static Electrical Characteristics

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNIT
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25		
								MIN	TYP	
Quiescent		0, 5	5	1	1	30	30	0.02		µa
Device		0, 10	10	2	2	60	60	0.02		
Current		0, 15	15	4	4	120	120	0.02		
I _{DD} Max.		0, 20	20	20	20	600	600	0.04		
Output Low (Sink)	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	mA
Current	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	
I _{OL} Min.	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	
Output High	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	mA
(Source)	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	
Current	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	
I _{OH} Min.	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	
Output Voltage		0, 5	5	0.05			0 0.05			V
Low-Level		0, 10	10	0.05			0 0.05			
V _{OL} Max.		0, 15	15	0.05			0 0.05			
Output Voltage		0, 5	5	4.95			4.95 5			V
High-Level		0, 10	10	9.95			9.95 10			
V _{OH} Min.		0, 15	15	14.95			14.95 15			
Input Low	0.5, 4.5		5	1.5			1.5			V
Voltage	1, 9		10	3			3			
V _{IL} Max.	1.5, 13.5		15	4			4			
Input High	0.5, 4.5		5	3.5			3.5			V
Voltage	1, 9		10	7			7			
V _{IH} Min.	1.5, 13.5		15	11			11			
Input Current, V _{IH} Max.		0, 18	18	±0.1	±0.1	±1	±1	±10 ⁻⁵ ±0.1		µA

6.4 Dynamic Electrical Characteristics

at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V _{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Propagation Delay Time	5	150 300			ns
Clock to Q or \bar{Q} Outputs	10	65 130			
t _{PHL} , t _{PLH}	15	45 90			
Set to Q or Reset to \bar{Q} , t _{PLH}	5	150 300			ns
	10	65 130			
	15	45 90			
Set to \bar{Q} or Reset to Q, t _{PHL}	5	200 400			ns
	10	85 170			
	15	60 120			
Transition Time	5	100 200			ns
t _{THL} , t _{TLH}	10	50 100			
	15	40 80			

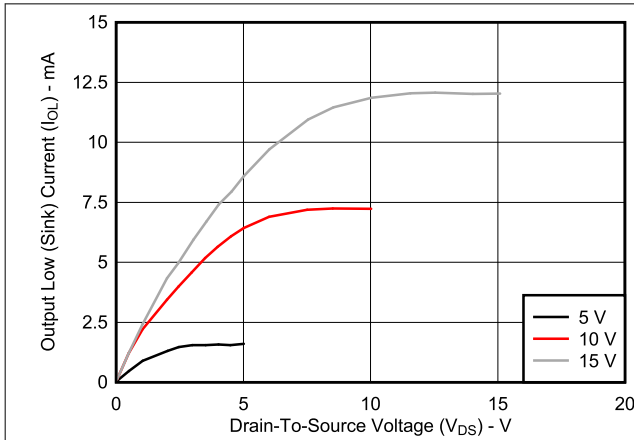
6.4 Dynamic Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

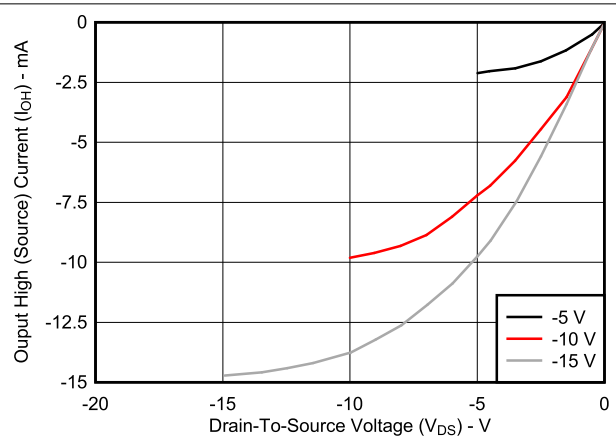
CHARACTERISTIC	V_{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Maximum Clock Input Frequency (Toggle Mode) ⁽¹⁾	5	3.5	7	MHz	
f_{CL}	10	8	16		
	15	12	24		
Minimum Clock Pulse Width, t_W	5		70	140	
	10		30	60	
	15		20	40	
Minimum Set or Reset Pulse Width, t_W	5		90	180	ns
	10		40	80	
	15		25	50	
Minimum Data Setup Time, t_S	5		100	200	ns
	10		35	75	
	15		25	50	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5			45	μs
	10			5	
	15			2	
Input Capacitance, C_I			5	7.5	pF

(1) Input $t_r, t_f = 5\text{ ns}$

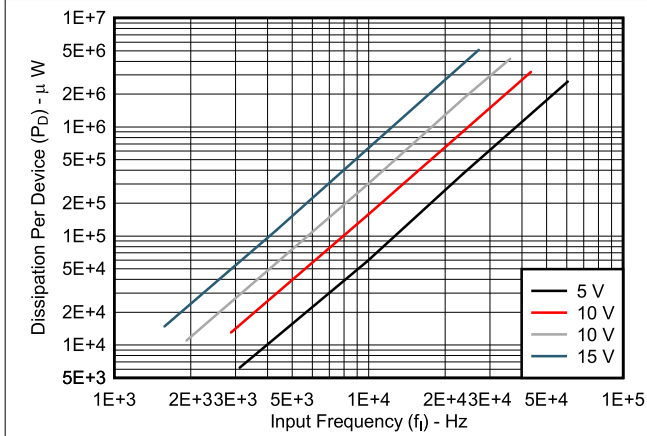
6.5 Typical Characteristics



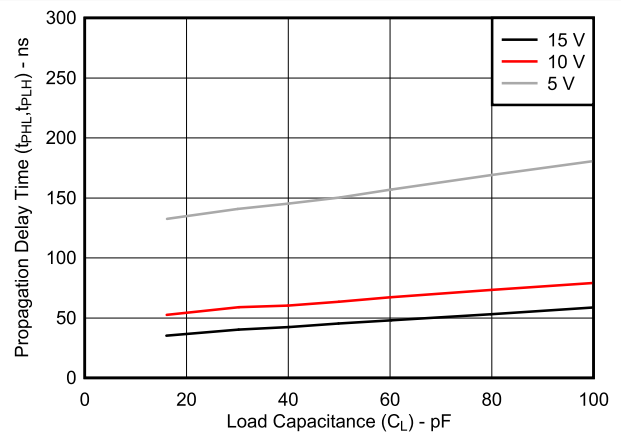
6-1. Typical Output Low (Sink) Current Characteristics



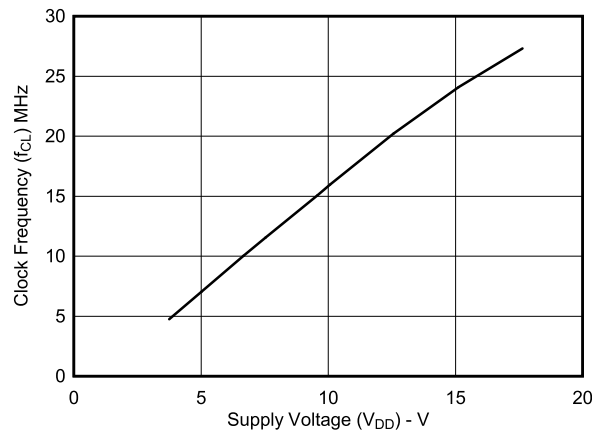
6-2. Typical Output High (Source) Current Characteristics



6-3. Typical Power Dissipation vs Frequency

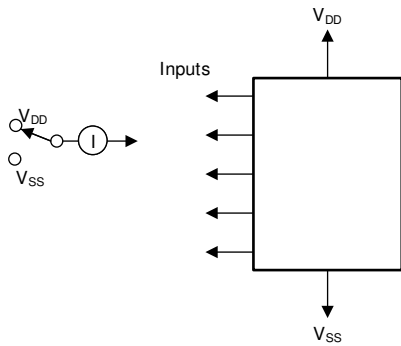


6-4. Typical Propagation Delay Time vs Load Capacitance (Clock or Set to Q, Clock or Reset to Q)

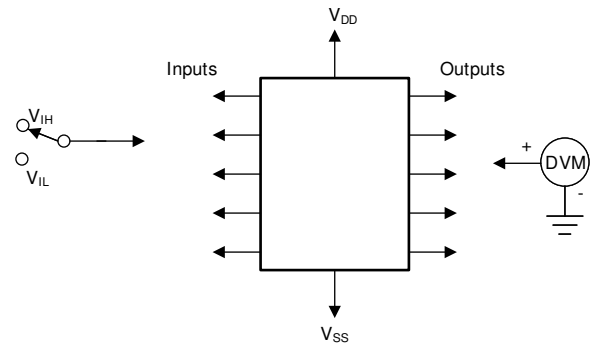


6-5. Typical Maximum Clock Frequency vs Supply Voltage (Toggle Mode)

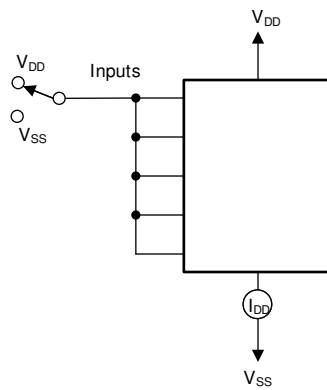
7 Parameter Measurement Information



7-1. Input Current Test Circuit



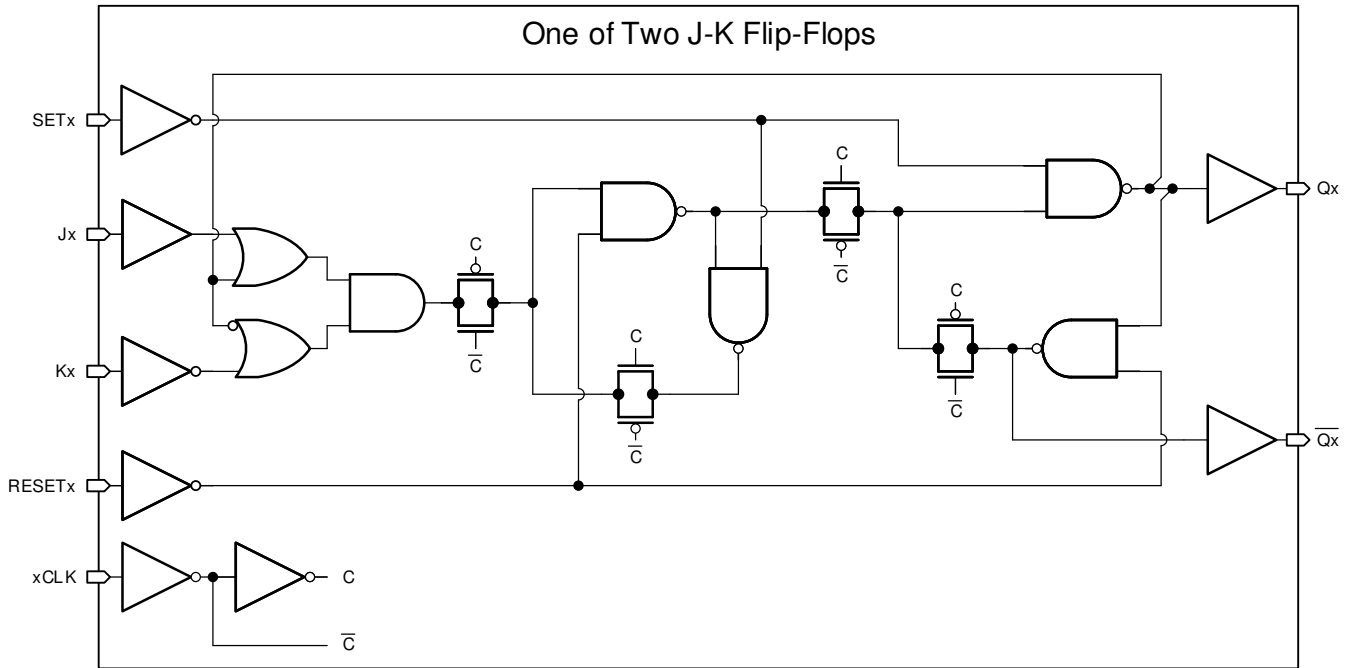
7-2. Input-Voltage Test Circuit









7-3. Quiescent Device Current Test Circuit

8 Detailed Description

8.1 Functional Block Diagram



8.2 Device Functional Modes⁽¹⁾

PRESENT STATE					CL ⁽²⁾	NEXT STATE	
INPUTS				OUTPUT		OUTPUTS	
J	K	S	R	O		O	\bar{O}
I	X	O	O	O		I	O
X	O	O	O	I		I	O
O	X	O	O	O		O	I
X	I	O	O	I		O	I
X	X	O	O	X		No change	No change
X	X	I	O	X	X	I	O
X	X	O	I	X	X	O	I
X	X	I	I	X	X	I	I

(1) Logic I = High Level, Logic O = Low Level, X = Do not care
 (2) Level change

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4027BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4027BE	Samples
CD4027BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4027BE	Samples
CD4027BF	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4027BF	Samples
CD4027BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4027BF3A	Samples
CD4027BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4027BM	
CD4027BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BM96E4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BMT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4027BM	
CD4027BNSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B	Samples
CD4027BPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM027B	
CD4027BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B	Samples
JM38510/05152BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05152BEA	Samples
M38510/05152BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05152BEA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4027B, CD4027B-MIL :

● Catalog : [CD4027B](#)

● Military : [CD4027B-MIL](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4027BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4027BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4027BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4027BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4027BNSR	SOP	NS	16	2000	356.0	356.0	35.0
CD4027BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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