TEXAS INSTRUMENTS
BQ25731
JAJSL33A – JUNE 2020 – REVISED JANUARY 2021

BQ25731 I²C 1～5 セル、昇降圧バッテリ充電コントローラ、USB-C PD 3.0 OTG 出力搭載

1 特長

- コスト削減と高効率を実現するバッテリ MOSFET はありません
- 400kHz/800kHz のプログラム可能なスイッチング周波数により、高効率と高い電力密度を実現
- USB-C パワー・デリバリ (PD) インターフェイス・プラットフォーム向け昇降圧 チャージャ
  - 1～5 セル・バッテリを充電するための 3.5V～26V 入力範囲
  - 5mΩ/10mΩ のセンシング抵抗に基づく分解能 128mA/64mA の最大 16.2A/8.1A の充電電流
  - 5mΩ/10mΩ のセンシング抵抗に基づく分解能 100mA/50mA の最大 10A/6.35A の入力電流制限
  - USB 2.0、USB 3.0、USB 3.1、USB パワー・デリバリ (PD) をサポート
  - 入力電流オプティマイザ (ICO) により、アダプタの過負荷を引き起こさずに最大入力電力を抽出
  - 降圧、昇降圧、および昇圧動作間のシームレスな遷移
  - ソース過負荷に対する入力電流および電圧のレギュレーション (IINDPM および VINDPM)
- EMI ノイズ低減を実現するためのテキサス・インスツルメンツによる特許申請中のスイッチング周波数ディザリング・パターン
- システムの電力効率向上とバッテリの高速充電を実現し、99% の効率を達成するためのテキサス・インスツルメンツによる特許申請中のパス・スルー・モード (PTM)。
- 専用ピンによる入力およびバッテリ電流モニタ
- 内蔵 8 ビット ADC により電圧、電流、電力を監視
- 専用ピンを使用した独立コンパレータ・ロジックをサポート
- バッテリから USB ポートへ電源供給 (USB OTG)
  - 分解能 8mV の 3V～24V OTG
  - 5mΩ/10mΩ のセンシング抵抗に基づく分解能 100mA/50mA の最大 12.7A/6.35A の出力電流制限
- I²C ホスト制御インターフェイスにより、柔軟なシステム構成が可能
- 高精度のレギュレーションと監視
  - ±0.5% の充電電圧レギュレーション
  - ±3% の充電電流レギュレーション
  - ±2.5% の入力電流レギュレーション
  - ±2% の入力 / 充電電流監視
- 安全
  - サーマル・シャットダウン
  - 入力、システム、バッテリの過電圧保護
  - 入力、MOSFET、インダクタの過電流保護
- パッケージ:32 ピン、4.0mm × 4.0mm WQFN

2 アプリケーション

- コードレス電動工具
- バッテリ・パック:コードレス電動工具
- 家電製品:バッテリ・チャージャ、パワー・バンク

3 概要

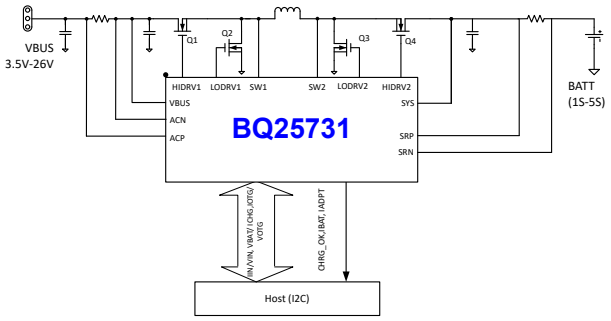
BQ25731 は、同期整流 昇降圧バッテリ充電コントローラであり、USB アダプタ、高電圧 USB-C パワー・デリバリ (PD) ソース、従来型のアダプタなど、多様な入力ソースから 1～5 セル・バッテリを充電します。スペースに制約のある 1～5 セルのバッテリ充電アプリケーション向けに、部品点数が少なく高効率のソリューションを実現します。

電源投入時に、充電器は入力電源およびバッテリの状況に基づいてコンバータを降圧、昇圧、昇降圧型のいずれかの構成に設定します。充電器はホストの制御なしに、降圧、昇圧、昇降圧型の動作モードをシームレスに遷移します。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
BQ25731	WQFN (32)	4.00mm × 4.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2020) to Revision A (January 2021)	Page
• 「事前情報」から「量産データ」に変更	1

5 Description (continued)

During power up, the charger sets the converter to a buck, boost, or buck-boost configuration based on the input source and battery conditions. The charger seamlessly transitions between the buck, boost, and buck-boost operation modes without host control.

In the absence of an input source, the BQ25731 supports the USB On-the-Go (OTG) function from a 1- to 5-cell battery to generate an adjustable 3-V to 24-V output on VBUS with 8-mV resolution. The OTG output voltage transition slew rate can be configured to comply with the USB-PD 3.0 PPS specification.

The latest version of the USB-C PD specification includes Fast Role Swap (FRS) to ensure power role swapping occurs in a timely fashion so that the device(s) connected to the dock can avoid experiencing momentary power loss or glitching. This device integrates FRS in compliance with the PD specification.

TI patented switching frequency dithering pattern can significantly reduce EMI noise over the whole conductive EMI frequency range (150 kHz to 30 MHz). Multiple dithering scale options are available to provide flexibility for different applications to simplify EMI noise filter design.

The charger can be operated in the TI patented Pass Through Mode (PTM) to improve efficiency over the full load range. In PTM, input power is directly passed through the charger to the system. Switching losses of the MOSFETs and inductor core loss can be saved for high efficiency operation.

The BQ25731 is available in a 32-pin 4 mm × 4 mm WQFN package.

6 Device Comparison Table

	BQ25710	BQ25713	BQ25792	BQ25731
Interface	SMBus	I^2C	I^2C	I^2C
Device address	09h	6Bh	6Bh	6Bh
Integrated MOSFET/Controller	Controller	Controller	Integrated MOSFET	Controller
Maximum Charge Current	8.128 A	8.128 A	5 A	16.256 A
Cell Count	1S~4S	1S~4S	1S~4S	1S~5S
Switching Frequency (Hz)	800 k/1.2 M	800 k/1.2 M	750 k/1.5 M	400 k/800 k
Input Current Sense Resistor	10 mΩ/20 mΩ	10 mΩ/20 mΩ	Integrated	5 mΩ/10 mΩ
Independent Comparator Latch	Non Latch	Non Latch	NA	Latch/Non latch (default)
VSYS_UVP	2.4 V	2.4 V	2.2 V	1.6 V
OTG Voltage Range	3.0 V - 20.8 V	3.0 V - 20.8 V	2.8 V - 22 V	3.0 V - 24 V
Frequency Dithering	No	No	No	Yes
BATFET Power Path	Yes	Yes	Yes	No

7 Pin Configuration and Functions

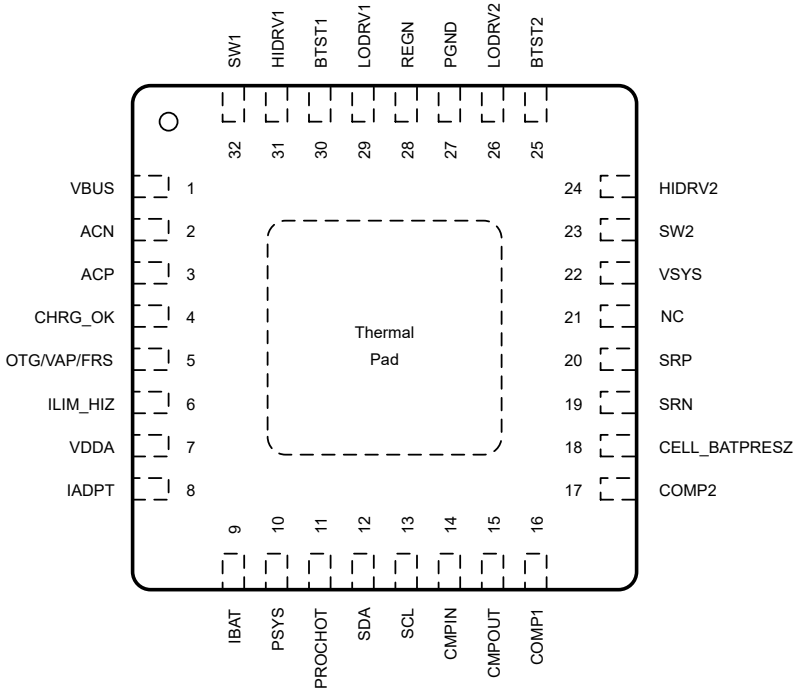


図 7-1. RSN Package 32-Pin WQFN Top View

表 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
ACN	2	PWR	Input current sense amplifier negative input. The leakage on ACP and ACN are matched. A RC low-pass filter is required to be placed between the sense resistor and the ACN pin to suppress the high frequency noise in the input current signal. Refer to セクション 10.2.2.2 for ACP/ACN filter design.
ACP	3	PWR	Input current sense amplifier positive input. The leakage on ACP and ACN are matched. A RC low-pass filter is required to be placed between the sense resistor and the ACP pin to suppress the high frequency noise in the input current signal. Refer to セクション 10.2.2.2 for ACP/ACN filter design.
NC	21	NA	Not in use, this pin must be floating
BTST1	30	PWR	Buck mode high-side power MOSFET driver power supply. Connect a 0.047-µF capacitor between SW1 and BTST1. The bootstrap diode between REGN and BTST1 is integrated.
BTST2	25	PWR	Boost mode high-side power MOSFET driver power supply. Connect a 0.047-µF capacitor between SW2 and BTST2. The bootstrap diode between REGN and BTST2 is integrated.
CELL_BATPRESZ	18	I	Battery cell selection pin for 1- to 5- cell battery setting. CELL_BATPRESZ pin is biased from VDDA through a resistor divider. CELL_BATPRESZ pin also sets SYSOVP thresholds to 5 V for 1-cell, 12 V for 2-cell and 19.5 V for 3-cell/4-cell and 25V for 5s. CELL_BATPRESZ pin is pulled below $V_{CELL\_BATPRESZ\_FALL}$ to indicate battery removal. After battery is removed the charge voltage register REG0x05/04h() goes back to default. No external cap is allowed at CELL_BATPRESZ pin. The device exits LEARN mode and disables charge when CELL_BATPRESZ pin is pulled low (upon battery removal).
CHRG_OK	4	O	Open drain active high indicator to inform the system good power source is connected to the charger input. Connect to the pullup rail via 10-kΩ resistor. When VBUS rises above 3.5 V and falls below 25.8 V, CHRG_OK is HIGH after 50-ms deglitch time. When VBUS falls below 3.2 V or rises above 26.8 V, CHRG_OK is LOW. When one of SYSOVP, SYSUVP, ACOC, TSHUT, BATOVP, BATOC or force converter off faults occurs, CHRG_OK is asserted LOW.

表 7-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CMPIN	14	I	Input of independent comparator. The independent comparator compares the voltage sensed on CMPIN pin with internal reference, and its output is on CMPOUT pin. Internal reference, output polarity and deglitch time is selectable by the I²C host. With polarity HIGH (CMP_POL = 1b), place a resistor between CMPIN and CMPOUT to program hysteresis. With polarity LOW (CMP_POL = 0b), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN to ground.
CMPOUT	15	O	Open-drain output of independent comparator. Place a pullup resistor from CMPOUT to pullup supply rail. Internal reference, output polarity and deglitch time are selectable by the I²C host. If the independent comparator is not in use, float CMPOUT pin.
COMP2	17	I	Buck boost converter compensation pin 2. Refer to セクション 9.3.12 for COMP2 pin RC network.
COMP1	16	I	Buck boost converter compensation pin 1. Refer to セクション 9.3.12 for COMP1 pin RC network.
OTG/VAP/FRS	5	I	Active HIGH to enable OTG or FRS modes. 1) When OTG_VAP_MODE=1b and EN_OTG=1b, pulling high this pin can enable OTG mode. 2) When OTG_VAP_MODE=1b and EN_FRS=1b, pulling high this pin can enable FRS mode in forward operation.
HIDRV1	31	O	Buck mode high-side power MOSFET (Q1) driver. Connect to high-side n-channel MOSFET gate.
HIDRV2	24	O	Boost mode high-side power MOSFET(Q4) driver. Connect to high-side n-channel MOSFET gate.
IADPT	8	O	The adapter current monitoring output pin. V_{IADPT} = 20 or 40 × (V_{ACP} – V_{ACN}) with ratio selectable through IADPT_GAIN bit. This pin is also used to program the inductance used in the application. Refer to セクション 9.3.11 for selecting resistor from the IADPT pin to ground . For a 4.7-µH inductance, the resistor is 191-kΩ or 187-kΩ standard value. Place a 100-pF or less ceramic decoupling capacitor from IADPT pin to ground. IADPT output voltage is clamped below 3.3 V.
IBAT	9	O	The battery current monitoring output pin. V_{IBAT} = 8 or 16 × (V_{SRP} – V_{SRN}) for charge current, or V_{IBAT} = 8 or 16 × (V_{SRN} – V_{SRP}) for discharge current, with ratio selectable through IBAT_GAIN bit. Place a 100-pF or less ceramic decoupling capacitor from IBAT pin to ground. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V.
ILIM_HIZ	6	I	Input current limit setting pin. Program ILIM_HIZ voltage by connecting a resistor divider from VDDA rail to ground. The pin voltage is calculated as: $V_{(ILIM\_HIZ)}$ = 1 V + 40 × IDPM × Rac, in which IDPM is the target input current limit. When EN_EXTILIM = 1b the input current limit used by the charger is the lower setting of ILIM_HIZ pin and IIN_HOST register. When EN_EXTILIM = 0b input current limit is only determined by IIN_HOST register. When the pin voltage is below 0.4 V, the device enters high impedance (HIZ) mode with low quiescent current. When the pin voltage is above 0.8 V, the device is out of HIZ mode. The ILIM_HIZ pin voltage is continuous read and used for updating current limit setting (If EN_EXTILIM=1b), this allows dynamic change input current limit setting by adjusting this pin voltage.
LODRV1	29	O	Buck mode low side power MOSFET (Q2) driver. Connect to low side n-channel MOSFET gate.
LODRV2	26	O	Boost mode low side power MOSFET (Q3) driver. Connect to low side n-channel MOSFET gate.
PGND	27	GND	Device power ground.
$\overline{\text{PROCHOT}}$	11	O	Active low open drain output indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the $\overline{\text{PROCHOT}}$ profile is triggered, a pulse is asserted. The minimum pulse width is adjustable through PROCHOT_WIDTH bits.
PSYS	10	O	Current mode system power monitor. The output current is proportional to the total power from the adapter and the battery. The gain is selectable through I²C. Place a resistor from PSYS to ground to generate output voltage. This pin can be floating if not in use. Its output voltage is clamped at 3.3 V. Place a capacitor in parallel with the resistor for filtering.
REGN	28	PWR	6-V linear regulator output supplied from VBUS or VSYS. The LDO is active when VBUS above V_{VBUS_CONVEN}. Connect a 2.2- or 3.3-µF ceramic capacitor from REGN to power ground. REGN pin output is for power stage gate drive.

表 7-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
SCL	13	I	I^2C clock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to specifications.
SDA	12	I/O	I^2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to I^2C specifications.
SRN	19	PWR	Charge current sense amplifier negative input. SRN pin is for battery voltage sensing as well. Connect a 0.1-µF filter cap cross battery charging sensing resistor and use 10-Ω contact resistor between SRN pin and battery charging sensing resistor. The leakage current on SRP and SRN are matched.
SRP	20	PWR	Charge current sense amplifier positive input. Connect a 0.1-µF filter cap cross battery charging sensing resistor and use 10-Ω contact resistor between SRP pin and battery charging sensing resistor. The leakage current on SRP and SRN are matched.
SW1	32	PWR	Buck mode switching node. Connect to the source of the buck half bridge high side n-channel MOSFET.
SW2	23	PWR	Boost mode switching node. Connect to the source of the boost half bridge high side n-channel MOSFET.
VBUS	1	PWR	Charger input voltage. An input low pass filter of 1 Ω and 0.47 µF (minimum) is recommended.
VDDA	7	PWR	Internal reference bias pin. Connect a 10-Ω resistor from REGN to VDDA and a 1-µF ceramic capacitor from VDDA to power ground.
VSYS	22	PWR	Charger system voltage sensing.
Thermal pad	–	–	Exposed pad beneath the IC. Always solder thermal pad to the board, and have vias on the thermal pad plane connecting to power ground planes. It serves as a thermal pad to dissipate the heat.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	SRN, SRP, ACN, ACP, VBUS, VSYS	–0.3	32	V
	SW1, SW2	–2	32	
	BTST1, BTST2, HIDRV1, HIDRV2,	–0.3	38	
	LODRV1, LODRV2 (25nS)	–4	7	
	HIDRV1, HIDRV2 (25nS)	–4	38	
	SW1, SW2 (25nS)	–4	32	
	SDA, SCL, REGN, PSYS, CHRG_OK, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP2, CMPIN, CMPOUT,OTG/VAP/FRS,	–0.3	7	
	$\overline{\text{PROCHOT}}$	–0.3	5.5	
	IADPT, IBAT, COMP1	–0.3	3.6	
Differential Voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	–0.3	7	V
	SRP-SRN, ACP-ACN	–0.5	0.5	
Temperature	Junction temperature range, T_J	–40	150	°C
Temperature	Storage temperature, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	ACN, ACP, VBUS	0		26	V
	SRN, SRP, VSYS	0		23.15	
	SW1, SW2	–2		26	
	BTST1, BTST2, HIDRV1, HIDRV2,	0		32	
	SDA, SCL, REGN, PSYS, CHRG_OK, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP2, CMPIN, CMPOUT,OTG/VAP/FRS	0		6.5	
	$\overline{\text{PROCHOT}}$	0		5.3	
	IADPT, IBAT, COMP1	0		3.3	
Differential Voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	0		6.5	V
	SRP-SRN, ACP-ACN	–0.5		0.5	
	BATDRV-VSYS	0		10.8	

8.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Temperature	Junction temperature range, T_J	–20		125	°C
	Storage temperature, T_{stg}	–20		85	

8.4 Thermal Information

THERMAL METRIC[1]		BQ25731 RSN (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[1])	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics(BQ25731)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUSOV\_FALL}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INPUT_OP}	Input voltage operating range		3.5		26	V
CHARGE VOLTAGE REGULATION						
V_{BAT_RNG}	Battery voltage regulation		1.024		23.00	V
$V_{BAT\_REG\_ACC}$	Battery voltage regulation accuracy (0°C to 85°C)	REG0x05/04() = 0x5208H		21		V
			–0.5%		0.5%	
$V_{BAT\_REG\_ACC}$	Battery voltage regulation accuracy (0°C to 85°C)	REG0x05/04() = 0x41A0H		16.8		V
			–0.5%		0.5%	
		REG0x05/04() = 0x3138H		12.6		V
			–0.5%		0.5%	
		REG0x05/04() = 0x20D0H		8.4		V
			–0.6%		0.6%	
		REG0x05/04() = 0x1068H		4.2		V
			–1.1%		1.45%	
CHARGE CURRENT REGULATION IN FAST CHARGE						
$V_{IREG\_CHG\_RNG}$	Charge current regulation differential voltage range	$V_{IREG\_CHG} = V_{SRP} – V_{SRN}$	0		81.28	mV

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CHRG\_REG\_ACC}$	Charge current regulation accuracy 5-mΩ R_{SR} sensing resistor, VBAT above VSYS_MIN(0°C to 85°C)	REG0x03/02() = 0x1000H		8192		mA
			–3.0%		3.0%	
		REG0x03/02() = 0x0800H		4096		mA
			–5.0%		6.0%	
		REG0x03/02() = 0x0400H		2048		mA
			–12%		13.5%	
		REG0x03/02() = 0x0200H		1024		mA
			–18%		21.5%	
CHARGE CURRENT REGULATION IN LOW BATTERY VOLTAGE						
I_{CLAMP}	current clamp under low battery voltage	CELL(≥2 S),VSRN < VSYS_MIN		384		mA
		CELL 1 S, VSRN < 3 V		384		mA
		CELL 1 S, 3 V < VSRN < 3.6V		2		A
$I_{LEAK\_SRP\_SRN}$	SRP, SRN leakage current mismatch (0°C to 85°C)		–13.5		10.0	µA
INPUT CURRENT REGULATION						
$V_{IREG\_DPM\_RNG}$	Input current regulation differential voltage range with 10-mΩ R_{AC} sensing resistor	V_{IREG_DPM} = V_{ACP} – V_{ACN}	0.5		64	mV
$I_{IIN\_DPM\_REG\_ACC}$	Input current regulation accuracy (-40°C to 105°C) with 5-mΩ R_{AC} sensing resistor	REG0x0F/0E() = 0x4E00H	7600	7800	8000	mA
		REG0x0F/0E() = 0x3A00H	5600	5800	6000	mA
		REG0x0F/0E() = 0x1C00H	2600	2800	3000	mA
		REG0x0F/0E() = 0x0800H	600	800	1000	mA
$I_{LEAK\_ACP\_ACN}$	ACP, ACN leakage current mismatch		–16		10	µA
$V_{IREG\_DPM\_RNG\_ILIM}$	Voltage range for input current regulation (ILIM_HIZ Pin)		1.15		4	V
$I_{IIN\_DPM\_REG\_ACC\_ILIM}$	Input Current Regulation Accuracy on ILIM_HIZ pin V_{ILIM_HIZ} = 1 V + 40 × I_{DPM} × R_{AC}, with 5-mΩ R_{AC} sensing resistor	V_{ILIM_HIZ} = 2.6 V	7600	8000	8400	mA
		V_{ILIM_HIZ} = 2.2 V	5600	6000	6400	mA
		V_{ILIM_HIZ} = 1.6 V	2600	3000	3400	mA
		V_{ILIM_HIZ} = 1.2 V	600	1000	1400	mA
I_{LEAK_ILIM}	ILIM_HIZ pin leakage current		–1		1	µA
INPUT VOLTAGE REGULATION						
V_{DPM_RNG}	Input voltage regulation range	Voltage on VBUS	3.2		19.52	V
$V_{DPM\_REG\_ACC}$	Input voltage regulation accuracy	REG0x0B/0A()=0x3C80H		18688		mV
			–3.5%		2%	
		REG0x0B/0A()=0x1E00H		10880		mV
			–4.5%		3%	
		REG0x0B/0A()=0x0500H		4480		mV
			–8%		5.5%	

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTG CURRENT REGULATION						
$V_{IOTG\_REG\_RNG}$	OTG output current regulation differential voltage range	V_{IOTG_REG} = V_{ACP} – V_{ACN}	0		81.28	mV
I_{OTG_ACC}	OTG output current regulation accuracy with 100-mA LSB and 5-mΩ ACP/ACN series resistor	REG0x09/08() = 0x3C00H	5600	6000	6400	mA
		REG0x09/08() = 0x1E00H	2600	3000	3400	mA
		REG0x09/08() = 0x0A00H	600	1000	1400	mA
OTG VOLTAGE REGULATION						
$V_{OTG\_REG\_RNG}$	OTG voltage regulation range(OOA disabled)	Voltage on VBUS	3		24.00	V
$V_{OTG\_REG\_ACC}$	OTG voltage regulation accuracy(OOA disabled)	REG0x07/06()=0x2CECH		23.00		V
			–2%		2%	
		REG0x07/06()=0x1770H		12.00		V
			–2%		2%	
		REG0x07/06()=0x09C4H		5.00		V
			–4%		3.5%	
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage (0 mA – 60 mA)	V_{VBUS} = 10 V	5.7	6	6.3	V
$V_{DROPOUT}$	REGN voltage in drop out mode	V_{VBUS} = 5 V, I_{LOAD} = 20 mA	3.8	4.3	4.6	V
I_{REGN_LIM}	REGN current limit when converter is enabled	V_{VBUS} = 10 V, force V_{REGN} =4 V	50	65		mA
QUIESCENT CURRENT						
$I_{BAT\_\_ON}$	System powered by battery. . I_{SRN} + I_{SRP} + I_{SW2} + I_{BTST2} + I_{SW1} + I_{BTST1} + I_{ACP} + I_{ACN} + I_{VBUS} + I_{VSYS}	VBAT = 18 V, REG0x01[7] = 1,REG0x31[6] = 0b, in low-power mode, Disable PSYS		22	45	µA
		VBAT = 18 V, REG0x01[7] = 1, REG0x31[6] = 1b, REG0x31[5:4] = 11b,REGN off, Disable PSYS, Enable low power $\overline{\text{PROCHOT}}$		35	60	µA
		VBAT = 18 V, REG0x01[7]= 0,REG0x31[5:4]= 11b, REGN on, Disable PSYS, In performance mode		880	1170	µA
		VBAT = 18 V, REG0x01[7] = 0, REG0x31[5:4] = 00b, REGN on, Enable PSYS, In performance mode		980	1270	µA
$I_{AC\_SW\_LIGHT\_buck}$	Input current during PFM in buck mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST} + I_{SW2} + I_{BTST2}	VIN = 20 V, VBAT = 12.6 V, 3s, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.2		mA
$I_{AC\_SW\_LIGHT\_boost}$	Input current during PFM in boost mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST2} + I_{SW2} + I_{BTST2}	VIN = 5 V, VBAT = 8.4 V, 2s, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.7		mA

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{AC\_SW\_LIGHT\_buckboost}$	Input current during PFM in buck boost mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	VIN = 12 V, VBAT = 12 V, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.4		mA
$I_{OTG\_STANDBY}$	Quiescent current during PFM in OTG mode, EN_OOA=0b, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST2} + I_{SW2} + I_{BTST2}	VBAT = 8.4 V, VBUS = 5 V, 800 kHz switching frequency, MOSFET Qg = 4nC		3		mA
		VBAT = 8.4 V, VBUS = 12 V, 800 kHz switching frequency, MOSFET Qg = 4nC		4.2		mA
		VBAT = 8.4 V, VBUS = 20 V, 800 kHz switching frequency, MOSFET Qg = 4nC		6.2		mA
CURRENT SENSE AMPLIFIER						
$V_{ACP\_ACN\_OP}$	Input common mode range	Voltage on ACP/ACN	3.8		26	V
V_{IADPT_CLAMP}	I_{ADPT} output clamp voltage		3.1	3.2	3.3	V
I_{IADPT}	I_{ADPT} output current				1	mA
A_{IADPT}	Input current sensing gain	$V_{(IADPT)}$ / $V_{(ACP-ACN)}$, REG0x00[4] = 0		20		V/V
		$V_{(IADPT)}$ / $V_{(ACP-ACN)}$, REG0x00[4] = 1		40		V/V
V_{IADPT_ACC}	Input current monitor accuracy	$V_{(ACP-ACN)}$ = 40.96 mV	–2%		2%	
		$V_{(ACP-ACN)}$ = 20.48 mV	–3%		3%	
		$V_{(ACP-ACN)}$ =10.24 mV	–6%		6%	
		$V_{(ACP-ACN)}$ = 5.12 mV	–10%		10%	
C_{IADPT_MAX}	Maximum capacitance at IADPT Pin				100	pF
$V_{SRP\_SRN\_OP}$	Battery common mode range	Voltage on SRP/SRN	2.5		23.15	V
V_{IBAT_CLAMP}	IBAT output clamp voltage		3.05	3.2	3.3	V
I_{IBAT}	IBAT output current				1	mA
A_{IBAT}	Charge and discharge current sensing gain on IBAT pin	$V_{(IBAT)}$ / $V_{(SRN-SRP)}$, REG0x00[3] = 0,		8		V/V
		$V_{(IBAT)}$ / $V_{(SRN-SRP)}$, REG0x00[3] = 1,		16		V/V
$I_{IBAT\_CHG\_ACC}$	Charge and discharge current monitor accuracy on IBAT pin	$V_{(SRN-SRP)}$ = 40.96 mV	–2%		2%	
		$V_{(SRN-SRP)}$ = 20.48 mV	–4%		4%	
		$V_{(SRN-SRP)}$ =10.24 mV	–7%		7%	
		$V_{(SRN-SRP)}$ = 5.12 mV	–15%		15%	
C_{IBAT_MAX}	Maximum capacitance at IBAT Pin				100	pF
SYSTEM POWER SENSE AMPLIFIER						
V_{PSYS}	PSYS output voltage range		0		3.3	V
I_{PSYS}	PSYS output current		0		160	µA
A_{PSYS}	PSYS system gain	$I_{(PSYS)}$ / ($P_{(IN)}$ +$P_{(BAT)}$), REG0x31[5:4] = 00b;REG0x31[1] = 1b		1		µA/W
A_{PSYS}	PSYS system gain	$I_{(PSYS)}$ / $P_{(IN)}$, REG0x31[5:4]= 01b;REG0x31[1] = 1b		1		µA/W

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PSYS_ACC}	PSYS gain accuracy (REG0x30[13:12] = 00b)	Adapter only with system power = 19.5 V / 45 W, TA = 0 to 85°C	–4%		4%	
		Battery only with system power = 11 V / 44 W, TA = 0 to 85°C	–3%		3%	
	PSYS gain accuracy (REG0x30[13:12] = 01b)	Adapter only with system power = 19.5 V / 45 W, TA = 0 to 85°C	–4%		4%	
V_{PSYS_CLAMP}	PSYS clamp voltage		3		3.3	V
VSYS UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{SYS_UVLOZ}	VSYS undervoltage rising threshold(≥1S)	VSYS rising	1.5	1.7	1.85	V
V_{SYS_UVLO}	VSYS undervoltage falling threshold(≥1S)	VSYS falling	1.4	1.6	1.75	V
$V_{SYS\_UVLO\_HYST}$	VSYS undervoltage hysteresis(≥1S)			100		mV
VBUS UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{VBUS_UVLOZ}	VBUS undervoltage rising threshold	VBUS rising	2.35	2.55	2.80	V
V_{VBUS_UVLO}	VBUS undervoltage falling threshold	VBUS falling	2.2	2.4	2.6	V
$V_{VBUS\_UVLO\_HYST}$	VBUS undervoltage hysteresis			150		mV
V_{VBUS_CONVEN}	VBUS converter enable rising threshold	VBUS rising	3.2	3.5	3.9	V
$V_{VBUS\_CONVENZ}$	VBUS converter enable falling threshold	VBUS falling	2.9	3.2	3.5	V
$V_{VBUS\_CONVEN\_HYST}$	VBUS converter enable hysteresis			300		mV
BATTERY UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{VBAT_UVLOZ}	VBAT undervoltage rising threshold	VSRN rising	2.35	2.55	2.80	V
V_{VBAT_UVLO}	VBAT undervoltage falling threshold	VSRN falling	2.2	2.4	2.6	V
$V_{VBAT\_UVLO\_HYST}$	VBAT undervoltage hysteresis			150		mV
V_{VBAT_OTGEN}	VBAT OTG enable rising threshold	VSRN rising	3.25	3.55	3.85	V
V_{VBAT_OTGENZ}	VBAT OTG enable falling threshold	VSRN falling	2.15	2.4	2.65	V
$V_{VBAT\_OTGEN\_HYST}$	VBAT OTG enable hysteresis			1150		mV
VBUS UNDER VOLTAGE COMPARATOR (OTG MODE)						
$V_{VBUS\_OTG\_UV}$	VBUS undervoltage falling threshold	As percentage of REG0x07/06()		85%		
$t_{VBUS\_OTG\_UV}$	VBUS time undervoltage deglitch			7		ms
VBUS OVER VOLTAGE COMPARATOR (OTG MODE)						
$V_{VBUS\_OTG\_OV}$	VBUS overvoltage rising threshold	As percentage of REG0x07/06()		110%		

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VBUS\_OTG\_OV}$	VBUS Time Overvoltage Deglitch			10		ms
BATTERY LOW VOLTAGE COMPARATOR (Charge current 384mA clamp corresponding battery voltage threshold for 1S)						
V_{BATLV_FALL}	BATLOWV falling threshold			2.8		V
V_{BATLV_RISE}	BATLOWV rising threshold			3		V
V_{BATLV_RHYST}	BATLOWV hysteresis			200		mV
INPUT OVER-VOLTAGE COMPARATOR (ACOV)						
V_{VBUSOV_RISE}	VBUS overvoltage rising threshold	VBUS rising	26.0	26.8	27.7	V
V_{VBUSOV_FALL}	VBUS overvoltage falling threshold	VBUS falling	25.0	25.8	26.7	V
V_{VBUSOV_HYST}	VBUS overvoltage hysteresis			1.0		V
$t_{VBUSOV\_RISE\_DEG}$	VBUS deglitch overvoltage rising	VBUS converter rising to stop converter		100		us
$t_{VBUSOV\_FALL\_DEG}$	VBUS deglitch overvoltage falling	VBUS converter falling to start converter		1		ms
INPUT OVER CURRENT COMPARATOR (ACOC)						
V_{ACOC}	ACP to ACN rising threshold, w.r.t. ILIM2_VTH	Voltage across input sense resistor rising, Reg0x32[2]= 1	180%	200%	220%	
V_{ACOC_FLOOR}	Measure between ACP and ACN	Set IIN_DPM to minimum	44	50	56	mV
$V_{ACOC\_CEILING}$	Measure between ACP and ACN	Set IIN_DPM to maximum	172	180	188	mV
$t_{ACOC\_DEG\_RISE}$	Rising deglitch time	Deglitch time to trigger ACOC		250		us
t_{ACOC_RELAX}	Relax time	Relax time before converter starts again		250		ms
SYSTEM OVER-VOLTAGE COMPARATOR (SYSOVP)						
V_{SYSOVP_RISE}	System overvoltage rising threshold to turnoff converter	1 s	5.8	6	6.1	V
		2 s	11.7	12	12.2	V
		3 s	19	19.5	20	V
		4 s	19	19.5	20	V
		5 s	24	25	26	V
V_{SYSOVP_FALL}	System overvoltage falling threshold	1 s		5.5		V
		2 s		11.7		V
		3 s		19.3		V
		4 s		19.3		V
		5 s		24.5		V
I_{SYSOVP}	Discharge current when SYSOVP stop switching was triggered	on VSYS pin		20		mA
BAT OVER-VOLTAGE COMPARATOR (BATOVP)						
V_{BATOVP_RISE}	Overvoltage rising threshold as percentage of VBAT_REG in REG0x05/04h()	1 s	102.3%	104%	106%	
		≥2 s	102.3%	104%	105%	

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATOVP_FALL}	Overvoltage falling threshold as percentage of VBAT_REG in REG0x05/04h()	1 s	100%	102%	104%	
		≥2 s	100%	102%	103%	
V_{BATOVP_HYST}	Overvoltage hysteresis as percentage of VBAT_REG in REG0x05/04h()	1 s		2%		
		≥2 s		2%		
I_{BATOVP}	Discharge current during BATOVP	Discharge current through VSYS pin		20		mA
CONVERTER OVER-CURRENT COMPARATOR (Q2)						
$V_{OCP\_lim\_Q2}$	Converter Over-Current Limit across Q2 MOSFET drain to source voltage	Reg0x32[5]=1b		150		mV
		Reg0x32[5]=0b		210		mV
$V_{OCP\_lim\_SYSSHRT\_Q2}$	System Short or SRN < 2.4 V	Reg0x32[5]=1b		45		mV
		Reg0x32[5]=0b		60		mV
CONVERTER OVER-CURRENT COMPARATOR (ACX)						
$V_{OCP\_lim\_ACX}$	Converter Over-Current Limit across ACP-ACN input current sensing resistor	Reg0x32[4]=1b; RSNS_RAC=0b		150		mV
		Reg0x32[4]=1b; RSNS_RAC=1b		100		mV
		Reg0x32[4]=0b;RSNS_RAC=0b		280		mV
		Reg0x32[4]=0b; RSNS_RAC=1b		200		mV
$V_{OCP\_lim\_SYSSHRT\_ACX}$	System Short or SRN < 2.4 V	Reg0x32[4]=1b;RSNS_RAC=0b		90		mV
		Reg0x32[4]=1b;RSNS_RAC=1b		60		mV
		Reg0x32[4]=0b;RSNS_RAC=0b		150		mV
		Reg0x32[4]=0b;RSNS_RAC=1b		120		mV
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT_RISE}	Thermal shutdown rising temperature	Temperature increasing		155		°C
T_{SHUTF_FALL}	Thermal shutdown falling temperature	Temperature reducing		135		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			20		°C
t_{SHUT_RDEG}	Thermal deglitch shutdown rising			100		us
t_{SHUT_FHYS}	Thermal deglitch shutdown falling			12		ms
ICRIT PROCHOT COMPARATOR						
I_{ICRIT_PRO}	Input current rising threshold for throttling as 10% above ILIM2_VTH	Only when ILIM2 setting is higher than 2A	105%	110%	117%	
INOM PROCHOT COMPARATOR						
I_{INOM_PRO}	INOM rising threshold as 10% above IIN_DPM		105%	110%	116%	
BATTERY DISCHARGE CURRENT LIMIT PROCHOT COMPARATOR(IDCHG)						
I_{DCHG_TH1}	IDCHG threshold1 for throttling CPU	Reg0x39[7:2]=010000b, with 5mΩ SRP/SRN current sensing resistor		16.384		A
			96%		103%	

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DCHG_DEG1}	IDCHG threshold1 deglitch time	Reg0x39h[1:0]=01b		1.25		sec
I_{DCHG_TH2}	IDCHG threshold2 for throttling for IDSCHG of 6 A	Reg0x39[7:2]=010000b 3C[5:3]=001b,with 5mΩ SRP/SRN current sensing resistor		24.567		A
			96%		103%	
t_{DCHG_DEG2}	IDCHG threshold2 deglitch time	Reg0x3C[7:6]=01b		1.6		ms
INDEPENDENT COMPARATOR						
V_{INDEP_CMP}	Independent comparator threshold	Reg0x30h[7]= 1, CMPIN falling	1.17	1.2	1.23	V
		Reg0x30h[7]= 0, CMPIN falling	2.27	2.3	2.33	V
$V_{INDEP\_CMP\_HYS}$	Independent comparator hysteresis	CMPIN falling		100		mV
POWER MOSFET DRIVER						
PWM OSCILLATOR AND RAMP						
F_{SW}	PWM switching frequency	Reg0x01[1] = 0	680	800	920	kHz
		Reg0x01[1] = 1	340	400	460	kHz
PWM HIGH SIDE DRIVER (HIDRV Q1)						
$R_{DS\_HI\_ON\_Q1}$	The resistance of the gate driver loop for turning on Q1	V_{BTST1} - V_{SW1} = 5 V		6		Ω
$R_{DS\_HI\_OFF\_Q1}$	The resistance of the gate driver loop for turning off Q1	V_{BTST1} - V_{SW1} = 5 V		1.3	2.2	Ω
$V_{BTST1\_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	V_{BTST1} - V_{SW1} when low-side refresh pulse is requested	3.2	3.7	4.6	V
PWM HIGH SIDE DRIVER (HIDRV Q4)						
$R_{DS\_HI\_ON\_Q4}$	The resistance of the gate driver loop for turning on Q4	V_{BTST2} - V_{SW2} = 5 V		6		Ω
$R_{DS\_HI\_OFF\_Q4}$	The resistance of the gate driver loop for turning off Q4	V_{BTST2} - V_{SW2} = 5 V		1.5	2.4	Ω
$V_{BTST2\_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	V_{BTST2} - V_{SW2} when low-side refresh pulse is requested	3.3	3.7	4.6	V
PWM LOW SIDE DRIVER (LODRV Q2)						
$R_{DS\_LO\_ON\_Q2}$	The resistance of the gate driver loop for turning on Q2	V_{BTST1} - V_{SW1} = 5.5 V		6		Ω
$R_{DS\_LO\_OFF\_Q2}$	The resistance of the gate driver loop for turning off Q2	V_{BTST1} - V_{SW1} = 5.5 V		1.7	2.6	Ω
PWM LOW SIDE DRIVER (LODRV Q3)						
$R_{DS\_LO\_ON\_Q3}$	The resistance of the gate driver loop for turning on Q3	V_{BTST2} - V_{SW2} = 5.5 V		6.8		Ω
$R_{DS\_LO\_OFF\_Q3}$	The resistance of the gate driver loop for turning off Q3	V_{BTST2} - V_{SW2} = 5.5 V		2.2	4.6	Ω
INTERNAL SOFT START During Charge Enable						

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SS_{STEP_SIZE}	Charge current soft-start step size			64		mA
SS_{STEP_TIME}	Charge current soft-start duration time for each step			8		us
INTEGRATED BTST DIODE (D1)						
V_{F_D1}	Forward bias voltage	IF = 20 mA at 25°C		0.8		V
V_{R_D1}	Reverse breakdown voltage	IR = 2 µA at 25°C			20	V
INTEGRATED BTST DIODE (D2)						
V_{F_D2}	Forward bias voltage	IF = 20 mA at 25°C		0.8		V
V_{R_D2}	Reverse breakdown voltage	IR = 2 µA at 25°C			20	V
INTERFACE						
LOGIC INPUT (SDA, SCL)						
V_{IN_LO}	Input low threshold	I^2C			0.4	V
V_{IN_HI}	Input high threshold	I^2C	1.3			V
LOGIC OUTPUT OPEN DRAIN (SDA, CHRG_OK, CMPOUT)						
V_{OUT_LO}	Output saturation voltage	5 mA drain current			0.4	V
V_{OUT_LEAK}	Leakage current	Voltage = 7 V	–1		1	µA
LOGIC INPUT (OTG/VAP/FRS pin)						
$V_{IN\_LO\_OTG}$	Input low threshold				0.4	V
$V_{IN\_HI\_OTG}$	Input high threshold		1.3			V
LOGIC OUTPUT OPEN DRAIN SDA						
$V_{OUT\_LO\_SDA}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT\_LEAK\_SDA}$	Leakage Current	Voltage = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN CHRG_OK						
$V_{OUT\_LO\_CHRG\_OK}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT\_LEAK\_CHRG\_OK}$	Leakage Current	Voltage = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN CMPOUT						
$V_{OUT\_LO\_CMPOUT}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT\_LEAK\_CMPOUT}$	Leakage Current	Voltage = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN ($\overline{PROCHOT}$)						
$V_{OUT\_LO\_PROCHOT}$	Output saturation voltage	50 Ω pullup to 1.05 V / 5-mA			300	mV
$V_{OUT\_LEAK\_PROCHOT}$	Leakage current	Voltage = 5.5 V	–1		1	µA
ANALOG INPUT (ILIM_HIZ)						
V_{HIZ_LO}	Voltage to get out of HIZ mode	ILIM_HIZ pin rising	0.8			V
V_{HIZ_HIGH}	Voltage to enable HIZ mode	ILIM_HIZ pin falling			0.4	V
ANALOG INPUT (CELL_BATPRESZ)						
V_{CELL_5S}	5s	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	90%	100%		

8.5 Electrical Characteristics(BQ25731) (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUSOV_FALL} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

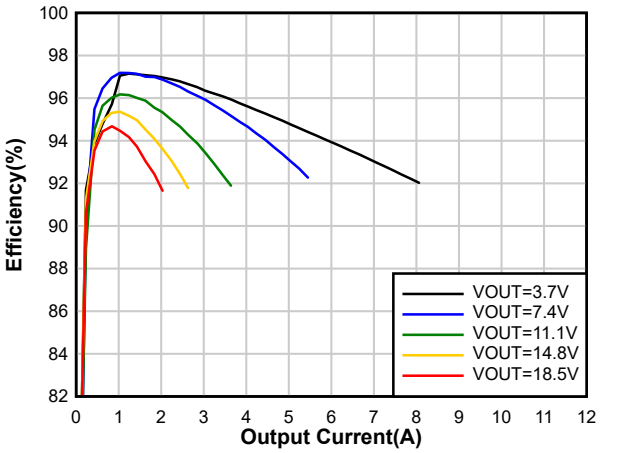
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CELL_4S}	4s setting	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	68.4%	75%	81.5%	
V_{CELL_3S}	3s setting	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	51.7%	55%	65%	
V_{CELL_2S}	2s setting	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	35%	40%	48.5%	
V_{CELL_1S}	1s setting	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	18.4%	25%	31.6%	
$V_{CELL\_BATPRESZ\_RISE}$	Battery is present	CELL_BATPRESZ rising	18%			
$V_{CELL\_BATPRESZ\_FALL}$	Battery is removed	CELL_BATPRESZ falling			15%	
ANALOG INPUT (COMP1, COMP2)						
I_{LEAK_COMP1}	COMP1 Leakage		–120		120	nA
I_{LEAK_COMP2}	COMP2 Leakage		–120		120	nA

8.6 Timing Requirements

		MIN	NOM	MAX	UNIT
I²C TIMING CHARACTERISTICS					
t_r	SCL/SDA rise time			300	ns
t_f	SCL/SDA fall time			300	ns
t_{HIGH}	SCL pulse width high	0.6		50	µs
t_{LOW}	SCL pulse width low	1.3			µs
$t_{SU:STA}$	Setup time for START condition	0.6			µs
$t_{HD:STA}$	Start condition hold time after which first clock pulse is generated	0.6			µs
$t_{SU:DAT}$	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	300			ns
$t_{SU:STO}$	Set up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between START and STOP conditions	1.3			µs
f_{SCL}	Clock frequency	10		400	kHz
HOST COMMUNICATION FAILURE					
$t_{TIMEOUT}$	I²C bus release timeout(1)	25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal	10			ms
t_{WDI}	Watchdog timeout period, REG0x01[6:5]=01	4	5.5	7	s
	Watchdog timeout period, REG0x01[6:5]=10	70	88	105	s
	Watchdog timeout period, REG0x01[6:5]=11	140	175	210	s

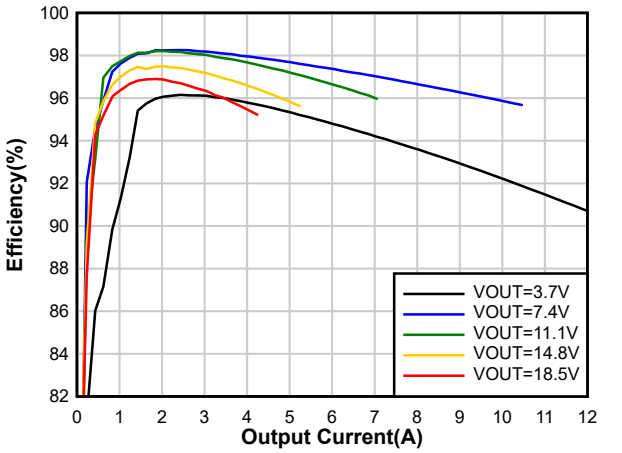
(1) Devices participating in a transfer timeout when any clock low exceeds the 25-ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35-ms maximum timeout period. Both a host and a target must adhere to the maximum value specified because it incorporates the cumulative stretch limit for both a host (10 ms) and a target (25 ms).

8.7 Typical Characteristics



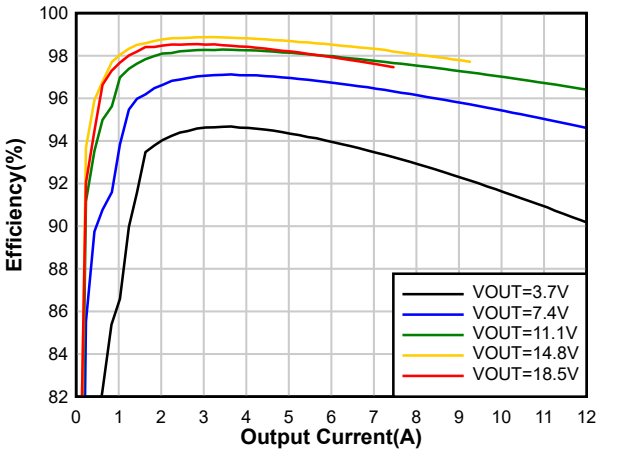
VIN = 5 V CCM VOUT=Battery Voltage
Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

図 8-1. Charge Efficiency



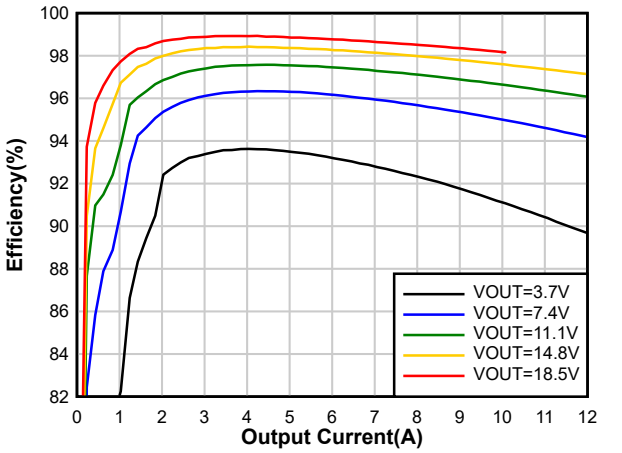
VIN = 9 V CCM VOUT=Battery Voltage
Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

図 8-2. Charge Efficiency



VIN = 15 V CCM VOUT=Battery Voltage
Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

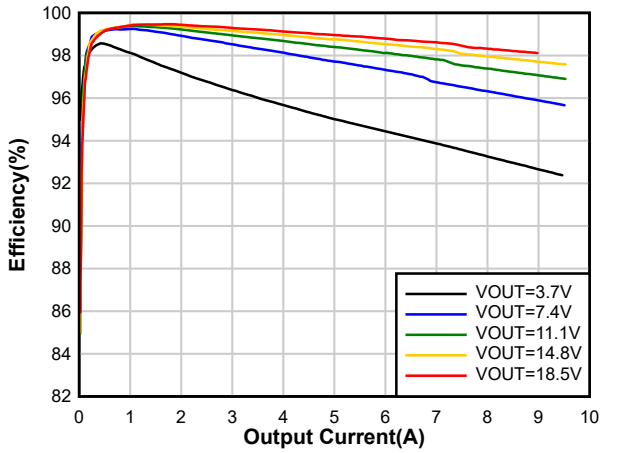
図 8-3. Charge Efficiency



VIN = 20 V CCM VOUT=Battery Voltage
Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

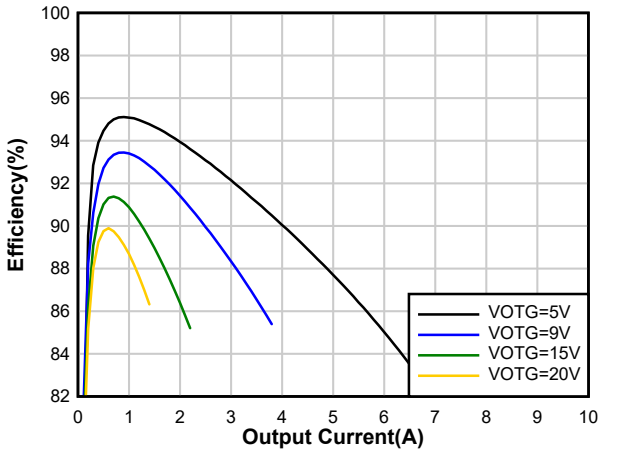
図 8-4. Charge Efficiency

8.7 Typical Characteristics (continued)



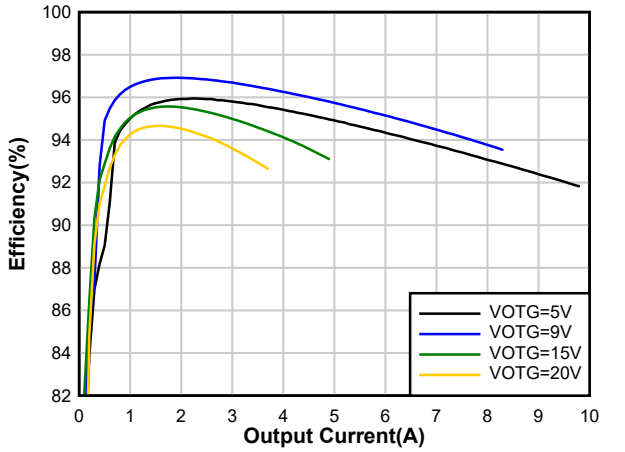
PTM Mode VOUT=Battery Voltage
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

図 8-5. PTM Mode Charge Efficiency



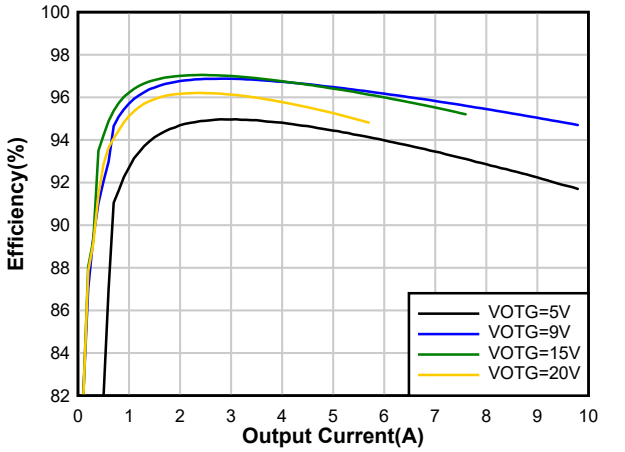
VBAT= 4 V CCM Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

図 8-6. OTG Efficiency with 1S Battery



VBAT= 8 V CCM Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

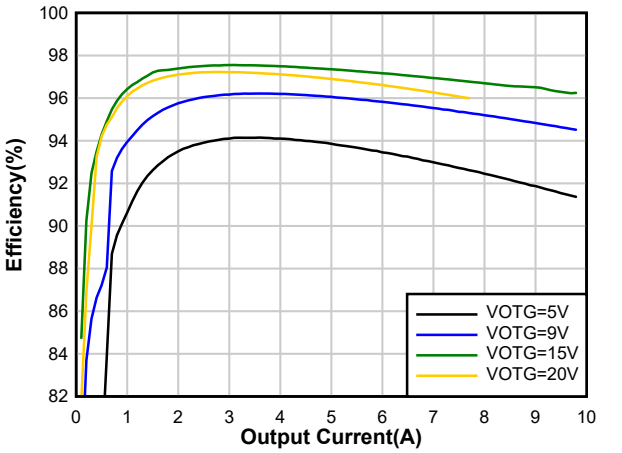
図 8-7. OTG Efficiency with 2S Battery



VBAT= 12 V CCM Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

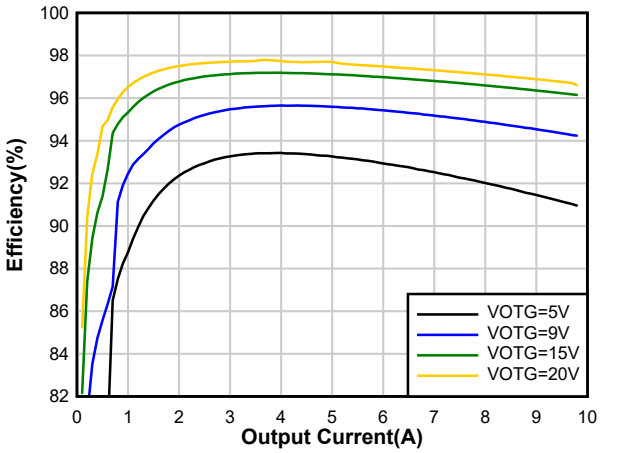
図 8-8. OTG Efficiency with 3S Battery

8.7 Typical Characteristics (continued)



VBAT= 16 V CCM Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

図 8-9. OTG Efficiency with 4S Battery



VBAT= 20 V CCM Fs=400kHz
R_{AC}=5mΩ R_{SR}=5mΩ Inductance=4.7uH

図 8-10. OTG Efficiency with 5S Battery

9 Detailed Description

9.1 Overview

The BQ25731 is a buck-boost charger controller for cordless power tools, power banks, and other appliances with rechargeable batteries. It provides seamless transition between different converter operation modes (buck, boost, or buck-boost), fast transient response, and high light load efficiency.

The BQ25731 supports a wide range of power sources, including USB-C PD ports, legacy USB ports, traditional AC-DC adapters, and so forth. It takes input voltage from 3.5 V to 26 V and charges a battery of 1 to 5 cells in series. In the absence of an input source, the BQ25731 supports the USB On-the-Go (OTG) function from a 1- to 5-cell battery to generate an adjustable 3 V to 24 V at the USB port with 8-mV resolution.

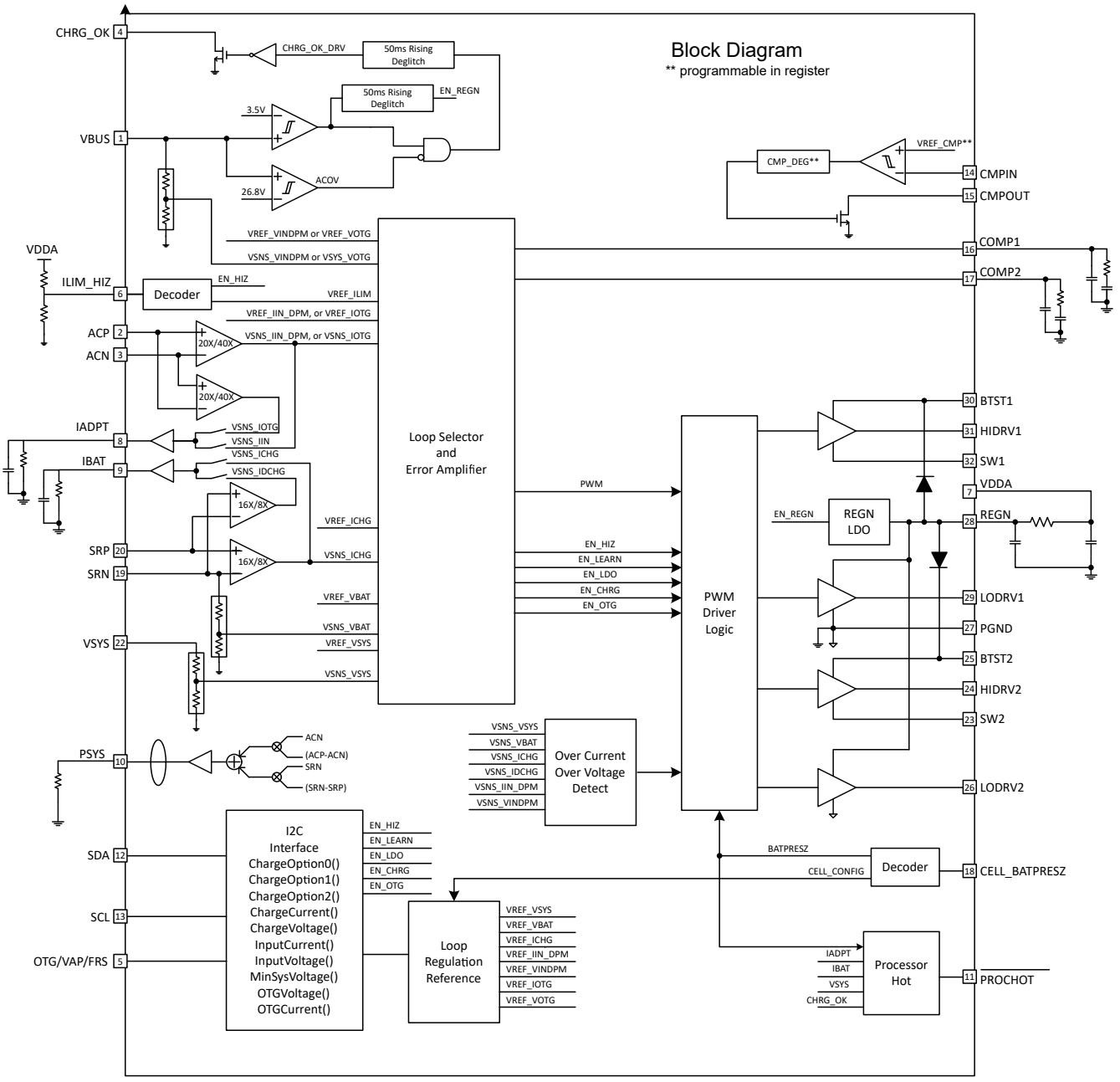
The BQ25731 features Dynamic Power Management (DPM) to limit input power and avoid AC adapter overloading. During battery charging, as system power increases, charging current is reduced to maintain total input current below adapter rating.

The latest version of the USB-C PD specification includes Fast Role Swap (FRS) to ensure power role swapping occurs in a timely fashion so that the device(s) connected to the dock never experience momentary power loss or glitching. The device integrates FRS with compliance to the USB-C PD specification.

The TI patented switching frequency dithering pattern can significantly reduce EMI noise over the entire conductive EMI frequency range (150 kHz to 30 MHz). Multiple dithering scale options are available to provide flexibility for different applications to simplify EMI noise filter design.

The I^2C host controls input current, charge current, and charge voltage registers with high resolution, high accuracy regulation limits.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-Up Sequence

The device powers up from the higher voltage of VBUS or VBAT through integrated power selector. The charger starts POR (power on reset) when VBUS exceeds V_{VBUS_UVLOZ} or VBAT exceeds V_{VBAT_UVLOZ}. 5 ms after either VBUS or VBAT becomes valid, the charger resets all the registers to the default state. Another 5 ms later, the user registers become accessible to the host.

Power up sequence when the charger is powered up from VBUS:

- After VBUS above V_{VBUS_UVLOZ}, enable 6-V LDO REGN pin and VDDA pin voltage increase accordingly. CHRG_OK pin goes HIGH and the AC_STAT is configured to 1.
- After passing VBUS qualification, the REGN voltage is setup. VINDPM is detected in VBUS steady state voltage and IIN_DPM is detected at ILIM_HIZ pin steady state voltage.
- Battery CELL configuration is read at CELL_BATPRESZ pin voltage and compared to VDDA to determine cell configuration. Corresponding the default value of ChargeVoltage register (REG0x05/04()), ChargeCurrent register (Reg0x03/02), VSYS_MIN and SYSOVP threshold are loaded.
- Converter powers up.

Power up sequence when the charger is powered up from VBAT:

- If only battery is present and the voltage is above V_{VBAT_UVLOZ} , charger wakes up .
- By default, the charger is in low power mode (EN_LWPWR = 1b) with lowest quiescent current. The REGN LDO stays off. The Quiescent current is minimized. $\overline{\text{PROCHOT}}$ is available through the independent comparator by setting EN_PROCHOT_LPWR=1b.
- The adapter present comparator is activated, to monitor the VBUS voltage.
- SDA and SDL lines stand by waiting for host commands.
- Device can move to performance mode by configuring EN_LWPWR = 0b. The host can enable IBAT buffer through setting EN_IBAT=1b to monitor discharge current. The PSYS, $\overline{\text{PROCHOT}}$ or the independent comparator also can be enabled by the host.
- In performance mode, the REGN LDO is always available to provide an accurate reference and gate drive voltage for the converter.

9.3.2 Two-Level Battery Discharge Current Limit

To prevent the triggering of battery overcurrent protection and avoid battery wear-out, two battery current limit levels (IDCHG_TH1 and IDCHG_TH2) $\overline{\text{PROCHOT}}$ profiles are recommended to be enabled. Define IDCHG_TH1 through REG0x39h[7:2], IDCHG_TH2 is set through REG0x3Ch[5:3] for fixed percentage of IDCHG_TH1. There are dedicated de-glitch time setting registers(IDCHG_DEG1 and IDCHG_DEG2) for both IDCHG_TH1 and IDCHG_TH2.

- When battery discharge current is continuously higher than IDCHG_TH1 for more than IDCHG_DEG1 de-glitch time, $\overline{\text{PROCHOT}}$ is asserted immediately. If the discharge current reduces to lower than IDCHG_TH1, then the time counter resets automatically. STAT_IDCHG1 bit will be set to 1 after $\overline{\text{PROCHOT}}$ is triggered.

  Set PP_IDCHG1=1b to enable IDCHG_TH1 for triggering $\overline{\text{PROCHOT}}$.
- When battery discharge current is continuously higher than IDCHG_TH2 for more than IDCHG_DEG2 de-glitch time, $\overline{\text{PROCHOT}}$ is asserted immediately. If the discharge current reduces to lower than IDCHG_TH2, then the time counter resets automatically. STAT_IDCHG2 bit will be set to 1 after $\overline{\text{PROCHOT}}$ is triggered.

  Set PP_IDCHG2=1b to enable IDCHG_TH2 for triggering $\overline{\text{PROCHOT}}$.

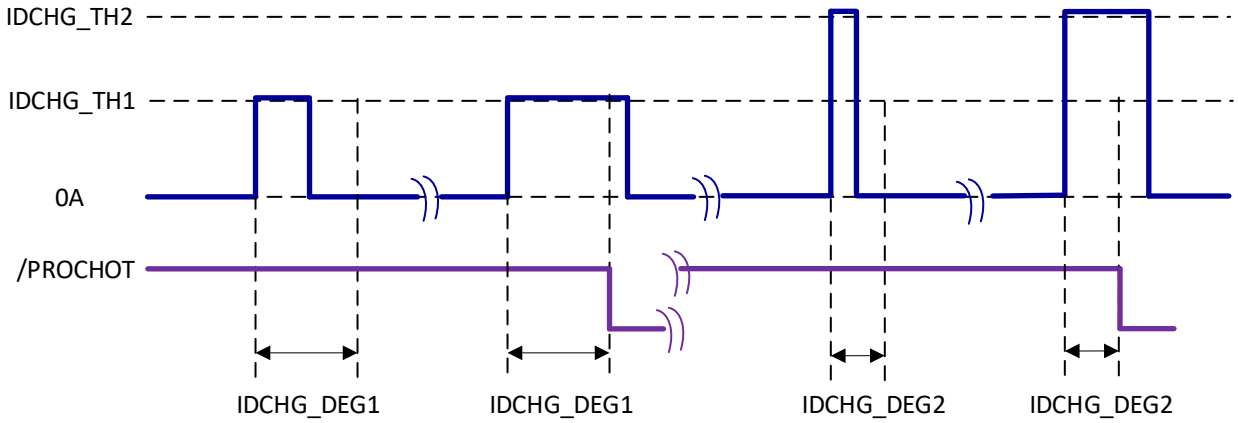


図 9-1. Two-Level Battery Discharging Current Trigger $\overline{\text{PROCHOT}}$ Diagram

9.3.3 Fast Role Swap Feature

Fast Role Swap (FRS) means charger quickly swaps from power sink role to power source role to provide an OTG output voltage to accessories when the original power source is disconnected. This feature is defined to transfer the charger from forward mode to OTG mode quickly without dropping VBUS voltage per USB-C PD specification requirement.Please contact factory for more detail information about FRS mode.

9.3.4 CHRG_OK Indicator

CHRG_OK is an active HIGH open drain indicator. It indicates the charger is in normal operation when the following conditions are valid:

- VBUS is above V_{VBUS_CONVEN}
- VBUS is below V_{ACOV_FALL}
- No faults triggered such as: SYSOVP/SYSUVP/ACOC/TSHUT/BATOVP/BATOC/force converter off.

9.3.5 Input and Charge Current Sensing

The charger supports 10 mΩ and 5 mΩ for both input current sensing and charge current sensing. By default, 5 mΩ is enabled by POR setting RSNS_RAC=1b and RSNS_RSR=1b, if 10-mΩ sensing is used please configure RSNS_RAC=0b and RSNS_RSR=0b. Lower current sensing resistor can help improve overall charge efficiency especially under heavy load. At same time PSYS,IADPT,IBAT pin accuracy and IINDPM/ICHG/IOTG regulation accuracy get worse due to effective signal reduction in comparison to error signal components.

When RSNS_RAC=RSNS_RSR=0b and 10 mΩ is used for both input and charge current sensing, the battery low voltage current clamp is 384 mA (2 A for 1S if 3.6 V>VBAT>3 V), the maximum IIN_HOST setting is clamped at 6.35 A, and the maximum charge current is clamped at 8.128 A.

When RSNS_RAC=RSNS_RSR=1b and 5 mΩ is used for both input and charge current sensing, the charger will internally compensate battery low voltage current clamp to be 384 mA (2 A for 1S if 3.6 V>VBAT>3 V) under 5-mΩ current sensing which keeps consistent between 10 mΩ and 5 mΩ. Under 5-mΩ current sensing application charge current range is doubled to 16.256 A. Based on EN_FAST_5MOHM register bit status and IADPT pin resistor the maximum input current can be configured referring to 表 9-1:

For defined current sense resistors (10 mΩ/5 mΩ), PSYS function is still valid when unsymmetrical input current sense and charge current sense resistors are used. But RSNS_RAC and RSNS_RSR bit status have to be consistent with practical resistors used in the system.

表 9-1. Maximum Input Current Limit Configuration Table

INDUCTANCE (IADPT Pin Resistance)	EN_FAST_5MOHM	RSR_RAC BIT	MAXIMUM INPUT CURRENT LIMIT (IINDPM)
1.0 uH(90.9 kΩ) 1.5 uH(121 kΩ) 2.2 uH(137 kΩ)	Xb	RSNS_RAC=0b	6.35 A
	1b	RSNS_RAC=1b	6.35 A
	0b	RSNS_RAC=1b	10 A
3.3 uH(169 kΩ)	Xb	RSNS_RAC=0b	6.35 A
	Xb	RSNS_RAC=1b	10 A

9.3.6 Input Voltage and Current Limit Setup

The actual input current limit being adopted by the device is the lower setting of IIN_DPM and ILIM_HIZ pin. Register IIN_DPM input current limit setting will reset for below scenarios:

- When adapter is removed (CHRG_OK is not valid). Note when adapter is removed IIN_HOST will be reset one time to 3.25 A, under battery only host is still able to overwrite IIN_HOST register with a new value. If the adapter plug back in and CHRG_OK is pulled up, IIN_HOST will not be reset again.
- When input current optimization (ICO) is executed (EN_ICO_MODE=1b), the charger will automatically detect the optimized input current limit based on adapter output characteristic. The final IIN_DPM register setting could be different from IIN_HOST after ICO.

The voltage regulation loop of the charger regulates the input voltage to prevent the input adapter collapsing. The VINDPM threshold should be configured based on no load input voltage level.Charger initiates a VBUS voltage measurement without any load (VBUS at no load) right before the converter is enabled. The default VINDPM threshold is VBUS at no load – 1.28 V. Host can adjust VINDPM threshold after device POR through InputVoltage register(0x0B/0Ah[]), range from 3.2V to 19.52V with LSB 64mV.

After input current and voltage limits are set, the charger device is ready to power up. The host can always program the input current and voltage limit after the charger being powered up based on the input source type.

9.3.7 Battery Cell Configuration

CELL_BATPRESZ pin is biased with a resistor divider from VDDA to GND. After REGN LDO is activated (VDDA rise up), the device detects the battery configuration through CELL_BATPRESZ pin bias voltage. No external cap is allowed at CELL_BATPRESZ pin. When CELL_BATPRESZ pin is pulled down to GND (because of battery removal) at the beginning of startup process, VSYS_MIN = 3.6 V and SYS_OVP = 25 V and Maximum charge voltage (REG0x15) follow 1 cell default setting 4.2 V. VSYS and VBAT ADC offset is also determined by CELL_BATPRESZ pin setting, under 1S-4S VSYS/VBAT ADC holds 2.88-V offset, however under 5S detection VSYS/VBAT ADC only holds 8.16-V offset to cover higher voltage range. Refer to 表 9-2 for CELL_BATPRESZ pin configuration typical voltage for swept cell count.

表 9-2. Battery Cell Configuration

CELL COUNT	PIN VOLTAGE w.r.t. VDDA	CHARGEVOLTAGE (REG0x05/04h)	SYSOVP	VSYS_MIN	VSYS/VBAT ADC OFFSET
5S	100%(Directly connect to VDDA)	21.000 V	25 V	15.4 V	8.16 V
4S	75%	16.800 V	19.5 V	12.3 V	2.88 V
3S	55%	12.600 V	19.5 V	9.2 V	2.88 V
2S	40%	8.400 V	12 V	6.6 V	2.88 V
1S	25%	4.200 V	6 V	3.6 V	2.88 V
Battery removal	0%	4.200 V	25 V	3.6 V	2.88 V

9.3.8 Device HIZ State

When input source is present, the charger can enter HIZ mode (converter shuts off) when ILIM_HIZ pin voltage is below 0.4 V or EN_HIZ is set to 1b. The charger is in the low quiescent current mode with REGN LDO enabled, ADC circuits are disactivated to reduce quiescent current. In order to exit HIZ mode, ILIM_HIZ pin voltage has to be higher than 0.8 V and EN_HIZ bit has to be set to 0b.

9.3.9 USB On-The-Go (OTG)

The device supports USB OTG operation to deliver power from the battery to other portable devices through USB port. The OTG mode output voltage is set in OTGVoltage register REG0x07/06() with 8-mV LSB range from 3.0 V to 24 V. The OTG mode output current is set in OTGCurrent register REG0x09() with 100-mA LSB range from 0 A to 12.7 A under 5-mΩ input current sensing. Both OTG voltage and OTG current are qualified for USB-C™ programed power supply (PPS) specification in terms of resolution and accuracy. The OTG mode can be enabled following below steps:

- Set target OTG current limit in OTGCurrent register, VBUS is below $V_{VBUS\_CONVENZ}$.
- Set OTG_VAP_MODE = 1b and EN_OTG = 1b.
- OTG/VAP/FRS pin is pulled high.
- 15 ms after the above conditions are valid, converter starts and VBUS ramps up to target voltage. CHRG_OK pin goes HIGH if OTG_ON_CHRGOK= 1b.

OTG/VAP/FRS pin is used as multi-function to enable OTG and FRS mode.

9.3.10 Converter Operation

The charger operates in buck, buck-boost and boost mode under different VBUS and VBAT combination. The buck-boost can operate seamlessly across the three operation modes. The 4 main switches operating status under continuous conduction mode (CCM) are listed below for reference.

表 9-3. MOSFET Operation

MODE	BUCK	BUCK-BOOST	BOOST
Q1	Switching	Switching	ON
Q2	Switching	Switching	OFF
Q3	OFF	Switching	Switching
Q4	ON	Switching	Switching

9.3.11 Inductance Detection Through IADPT Pin

The charger reads both converter operation frequency and the inductance value through the resistance tied to IADPT pin before the converter starts up. The resistances recommended for 2.2-µH (800 kHz), 3.3-µH (800 kHz) and 4.7-µH (400 kHz) inductance refers to 表 9-4. A surface mount chip resistor with ±3% or better tolerance must to be used for an accurate inductance detection.

表 9-4. Inductor Detection through IADPT Resistance

INDUCTOR IN USE	RESISTOR ON IADPT PIN
2.2 µH (recommended for 800 kHz)	137 kΩ or 140 kΩ
3.3 µH (recommended for 800 kHz)	169 kΩ
4.7 µH (recommended for 400 kHz)	191 kΩ or 187 kΩ

9.3.12 Converter Compensation

The charger employs two compensation pins COMP1 and COMP2 for converter compensation purpose, appropriate RC network is needed to guarantee converter steady state and transient operation. Under different operation frequency corresponding RC network value needs to be configured respectively as shown in below table. The definition of these RC components can be referred to 図 9-2. It is not recommended to change the compensation network value due to the complexity of various operation modes.

表 9-5. Compensation Configuration

COMPONENT VALUE	INDUCTOR	COMP1 R1	COMP1 C11	COMP1 C12	COMP2 R2	COMP2 C21	COMP2 C22
400 kHz	4.7 µH	40.2 kΩ	4.7 nF	33 pF	15 kΩ	680 pF	15 pF
800 kHz	3.3 µH	16.9 kΩ	3.3 nF	33 pF	15 kΩ	1200 pF	15 pF
800 kHz	2.2 µH	16.9 kΩ	3.3 nF	33 pF	10 kΩ	1200 pF	15 pF

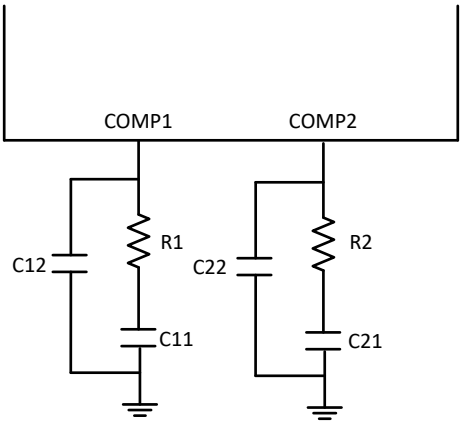


図 9-2. Compensation RC Network

9.3.13 Continuous Conduction Mode (CCM)

With sufficient charge or system current, the inductor current does not cross 0 A, which is defined as CCM. The controller starts a new cycle with ramp coming up from 200 mV. As long as the error amplifier output voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds error amplifier output voltage, HSFET turns off and low-side MOSFET (LSFET) turns on. At the end of the cycle, ramp gets reset and LSFET turns off, ready for the next cycle. There is always break-before-make logic during transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM, the inductor current always flows. Having the LSFET turn-on when the HSFET is off keeps the power dissipation low and allows safe charging at high currents.

9.3.14 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, BQ25731 switches to PFM operation at light load. The effective switching frequency will decrease accordingly when system load decreases. The minimum frequency can be limited to 25 kHz when the OOA feature is enabled (EN_OOA=1b) to avoid audible noise.

9.3.15 Switching Frequency and Dithering Feature

Normally, the IC switches in fixed frequency which can be adjusted through PWM_FREQ register bit. The Charger also support frequency dithering function to improve EMI performance. This function is disabled by default with setting EN_DITHER=00b. It can be enabled by setting EN_DITHER=01/10/11b, the switching frequency is not fixed when dithering is enabled. It varies within determined range by EN_DITHER setting, 01/10/11b is corresponding to ±2%/4%/6% switching frequency. Please contact factory for more detail information.

9.3.16 Current and Power Monitor

9.3.16.1 High-Accuracy Current Sense Amplifier (IADPT and IBAT)

A high-accuracy current sense amplifier (CSA) is used to monitor the input current during forward charging, or output current during OTG (IADPT) and the charge/discharge current (IBAT). IADPT voltage is 20× or 40× the differential voltage across ACP and ACN. IBAT voltage is 8×/16× of the differential across SRP and SRN. After input voltage or battery voltage is above UVLO, IADPT output becomes valid. To lower the voltage on current

monitoring, a resistor divider from CSA output to GND can be used and accuracy over temperature can still be achieved.

- V_{IADPT} = 20 or 40 × (V_{ACP} – V_{ACN}) during forward mode, or 20 or 40 × (V_{ACN} – V_{ACP}) during reverse OTG mode.
- V_{IBAT} = 8 or 16 × (V_{SRP} – V_{SRN}) during forward charging mode.
- V_{IBAT} = 8 or 16 × (V_{SRN} – V_{SRP}) during forward supplement mode, reverse OTG mode and battery only discharge scenario.

A maximum 100-pF capacitor is recommended to connect on the output for decoupling high-frequency noise. An additional RC filter is optional. Note that RC filtering has additional response delay. The CSA output voltage is clamped at 3.3 V.

9.3.16.2 High-Accuracy Power Sense Amplifier (PSYS)

The charger monitors total system power. During forward mode, the input adapter powers the system. During reverse OTG mode and battery only discharge scenario, the battery powers the system and VBUS output. The ratio of PSYS pin output current and total system power, K_{PSYS}, can be programmed in PSYS_RATIO register bit with default 1 µA/W. The input and charge sense resistors (R_{AC} and R_{SR}) are selected in RSNS_RAC bit and RSNS_RSR bit. By default, PSYS_CONFIG=00b and PSYS voltage can be calculated with 式 1, where I_{IN}>0 when the charger is in forward charging and I_{IN}<0 when charger is in OTG operation; where I_{BAT}>0 when the battery is in charging and I_{BAT}<0 when battery is discharging.

$$V_{PSYS} = R_{PSYS} \cdot K_{PSYS} (V_{ACP} \cdot I_{IN} + V_{SYS} \cdot I_{BAT}) \quad (1)$$

R_{AC} and R_{SR} values are not limited to symmetrical both 5 mΩ or both 10 mΩ. For defined current sense resistors (10 mΩ/5 mΩ), PSYS function is still valid when R_{AC}=5 mΩ(RSNS_RAC=1b) and R_{SR}=10 mΩ(RSNS_RAC=0b), vice versa. As long as RSNS_RAC and RSNS_RSR bit status are consistent with practical resistors used in the system.

Charger can block IBAT contribution to above equation by setting PSYS_CONFIG =01b in forward mode and block IBUS contribution to above equation by setting PSYS_OTG_IDCHG=1b in OTG mode.

To minimize the quiescent current, the PSYS function is disabled by default PSYS_CONFIG = 11b.

表 9-6. PSYS Configuration Table

CASE #	PSYS_CONFIG BITS	PSYS_OTG_IDCHG BITS	FORWARD MODE PSYS CONFIGURATION	OTG MODE PSYS CONFIGURATION
1	00b	0b	PSYS = PBUS+PBAT	PSYS = PBUS + PBAT
2	00b	1b	PSYS = PBUS+PBAT	PSYS =PBAT
3	01b	Xb	PSYS = PBUS	PSYS = 0
4	11b	Xb	PSYS = 0 (Disabled)	PSYS = 0 (Disabled)
5 (Reserved)	10b	Xb	PSYS = 0 (Reserved)	PSYS = 0 (Reserved)

9.3.17 Input Source Dynamic Power Management

The charger supports Dynamic Power Management (DPM). Normally, the input power source provides power for the system load and/or charging the battery. When the input current exceeds the input current setting (IIN_DPM), or the input voltage falls below the input voltage setting (VINDPM), the charger decreases the charge current to provide priority to the system load. As the system current rises, the available charge current drops accordingly towards zero. If the system load keeps increasing after the charge current drops down to zero, the system voltage starts to drop. As the system voltage drops below the battery voltage, the battery will discharge to supplement the heavy system load.

9.3.18 Input Current Optimizer (ICO)

For a recognized input adapter, IINDPM can be configured precisely to prevent adapter collapasing. When a third party unknown adapter is used, then input voltage regulation (VINDPM) feature can be leveraged to

prevent input crash. With the increasing of input current, voltage drops along the input cable also increases and voltage measured it charger input port decreases accordingly. VINDPM feature can limit input power from adapter by regulating VBUS at certain value configured at InputVoltage register(0x0Bh/0Ah[]). However, the adapter may still overheat when it is kept running at its voltage limit for a long period of time. Therefore, it is preferred to operate the third party adapter slightly under its current rating. The Input Current Optimizer (ICO) feature can automatically maximize the power of unknown input adapter without continuously working under VINDPM. Note the ICO feature can only be employed when the adapter input current limit is at least 500 mA. Please contact factory for more detail information about ICO feature.

9.3.19 Two-Level Adapter Current Limit (Peak Power Mode)

Usually adapter can supply current higher than DC rating for a few milliseconds to tens of milliseconds. The charger employs two-level input current limit, or peak power mode, to fully utilize the overloading capability. The level 1 current limit, or I_{LIM1}, is the same as adapter DC current, set in IIN_DPM register. The level 2 overloading current, or I_{LIM2}, is set in ILIM2_VTH, as a percentage of I_{LIM1}.

When the charger detects input current surge and battery discharge due to load transient (both the adapter and battery support the system together), the charger will first apply I_{LIM2} for T_{OVLD} (PKPWR_TOVLD_DEG register bits), and then I_{LIM1} for up to $T_{MAX} - T_{OVLD}$ time. T_{MAX} is programmed in PKPWR_TMAX register bits. After $T_{MAX,}$ if the load is still high, another peak power cycle starts. Charging is disabled during T_{MAX} and T_{OVLD} already expires; once $T_{MAX,}$ expires, a new cycle starts and resumes charging automatically.

To prepare entering peak power follow below steps:

- Set EN_IIN_DPM=1b to enable input current dynamic power management.
- Set EN_EXTILIM=0b to disable external current limit.
- Set register IIN_HOST based on adapter output current rating as the level 1 current limit(I_{LIM1})
- Set register bits ILIM2_VTH according to the adapter overload capability as the level 2 current limit(I_{LIM2}) .
- Set register bits PKPWR_TOVLD_DEG as I_{LIM2} effective duration time for each peak power mode operation cycle based on adapter capability.
- Set register bits PKPWR_TMAX as each peak power mode operation cycling time based on adapter capability.

Host need to set EN_PKPWR_IIN_DPM=1b to enable peak power mode triggered by input current overshoot. The overshoot threshold is IIN_DPM register which is same as the level 1 current limit (I_{LIM1}). Typical application waveform refer to 図 10-18.

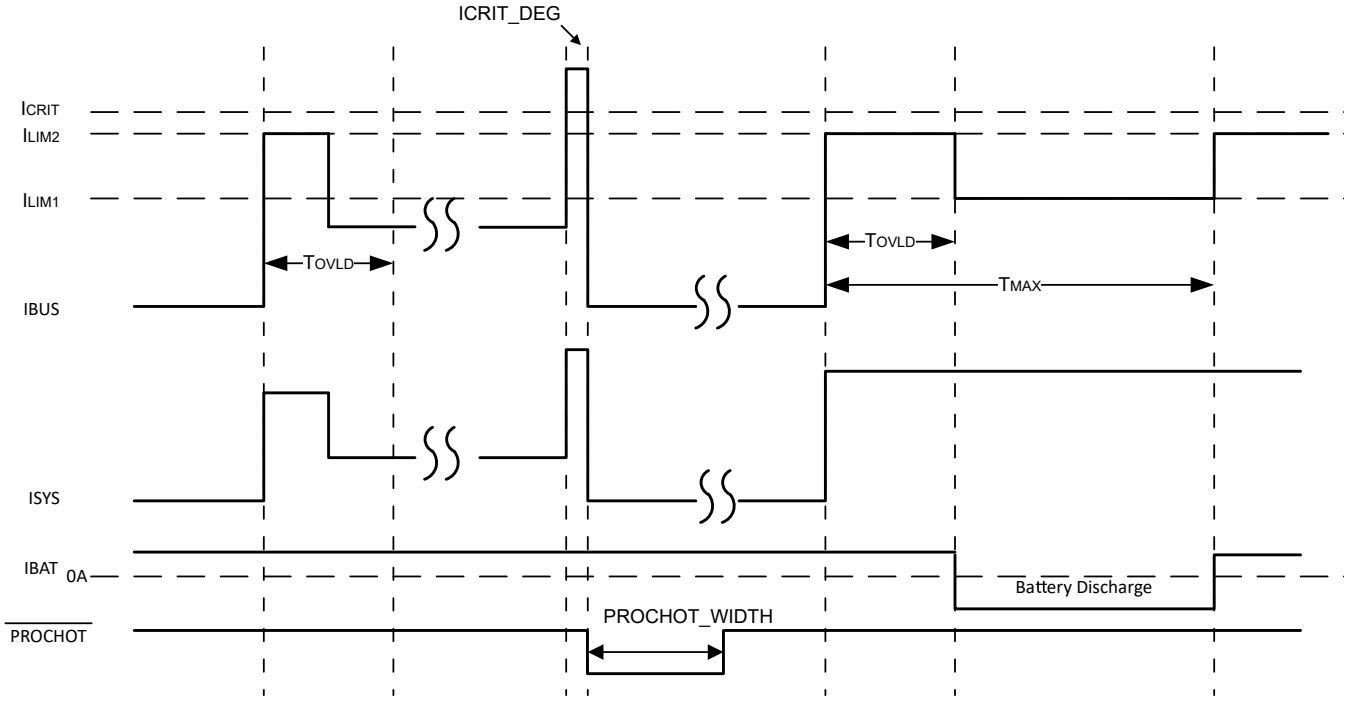


図 9-3. Two-Level Adapter Current Limit Timing Diagram

9.3.20 Processor Hot Indication

The events monitored by the processor hot function includes:

- ICRIT: adapter peak current, as 110% of I_{LIM2}
- INOM: adapter average current (110% of IIN_DPM)
- IDCHG1: battery discharge current level 1
- IDCHG2: battery discharge current level 2, note IDCHG2 threshold is always larger than IDCHG1 threshold determined by IDCHG_TH2 register setting.
- VBUS_VAP: VBUS threshold to trigger PROCHOT in VAP mode 2 and 3.
- VSYS: system voltage on VSYS pin
- Adapter Removal: upon adapter removal (VBUS is lower than ACOK_TH=3.2 V same as $V_{VBUS\_CONVENZ}$ threshold)
- Battery Removal: upon battery removal (CELL_BATPRESZ pin goes LOW)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)
- VINDPM: VBUS lower than 83%/91%/100% of VINDPM setting. The effective threshold PROCHOT_VINDPM is determined by combination of register PROCHOT_VINDPM_80_90 bit and LOWER_PROCHOT_VINDPM bit:
  - PROCHOT_VINDPM=VINDPM register setting: LOWER_PROCHOT_VINDPM=0b;
  - PROCHOT_VINDPM=83% VINDPM register setting: LOWER_PROCHOT_VINDPM=1b;PROCHOT_VINDPM_80_90=0b;
  - PROCHOT_VINDPM=91% VINDPM register setting: LOWER_PROCHOT_VINDPM=1b;PROCHOT_VINDPM_80_90=1b;
- EXIT_VAP: Every time when the charger exits VAP mode.

The threshold of ICRIT, IDCHG1,IDCHG2,VSYS or VINDPM, and the deglitch time of ICRIT, INOM, IDCHG1, IDCHG2, or CMPOUT are programmable through I^2C register bits. Except the PROCHOT_EXIT_VAP is always enabled, the other triggering events can be individually enabled in ProchotOption1[7:0], PP_IDCHG2 and PP_VBUS_VAP. When any enabled event in $\overline{\text{PROCHOT}}$ profile is triggered, $\overline{\text{PROCHOT}}$ is asserted low for a single pulse with minimal width programmable in PROCHOT_WIDTH register bits. At the end of the single pulse, if the $\overline{\text{PROCHOT}}$ event is still active, the pulse gets extended until the event is removed.

If the PROCHOT pulse extension mode is enabled by setting EN_PROCHOT_EXT= 1b, the PROCHOT pin will be kept low until host writes PROCHOT_CLEAR= 0b, even if the triggering event has been removed.

If the PROCHOT_VINDPM or PROCHOT_EXIT_VAP is triggered, PROCHOT pin will always stay low until the host clears it, no matter the PROCHOT is in one pulse mode or in extended mode. In order to clear PROCHOT_VINDPM, host needs to write 0 to STAT_VINDPM. In order to clear PROCHOT_EXIT_VAP, host needs to write 0 to STAT_EXIT_VAP.

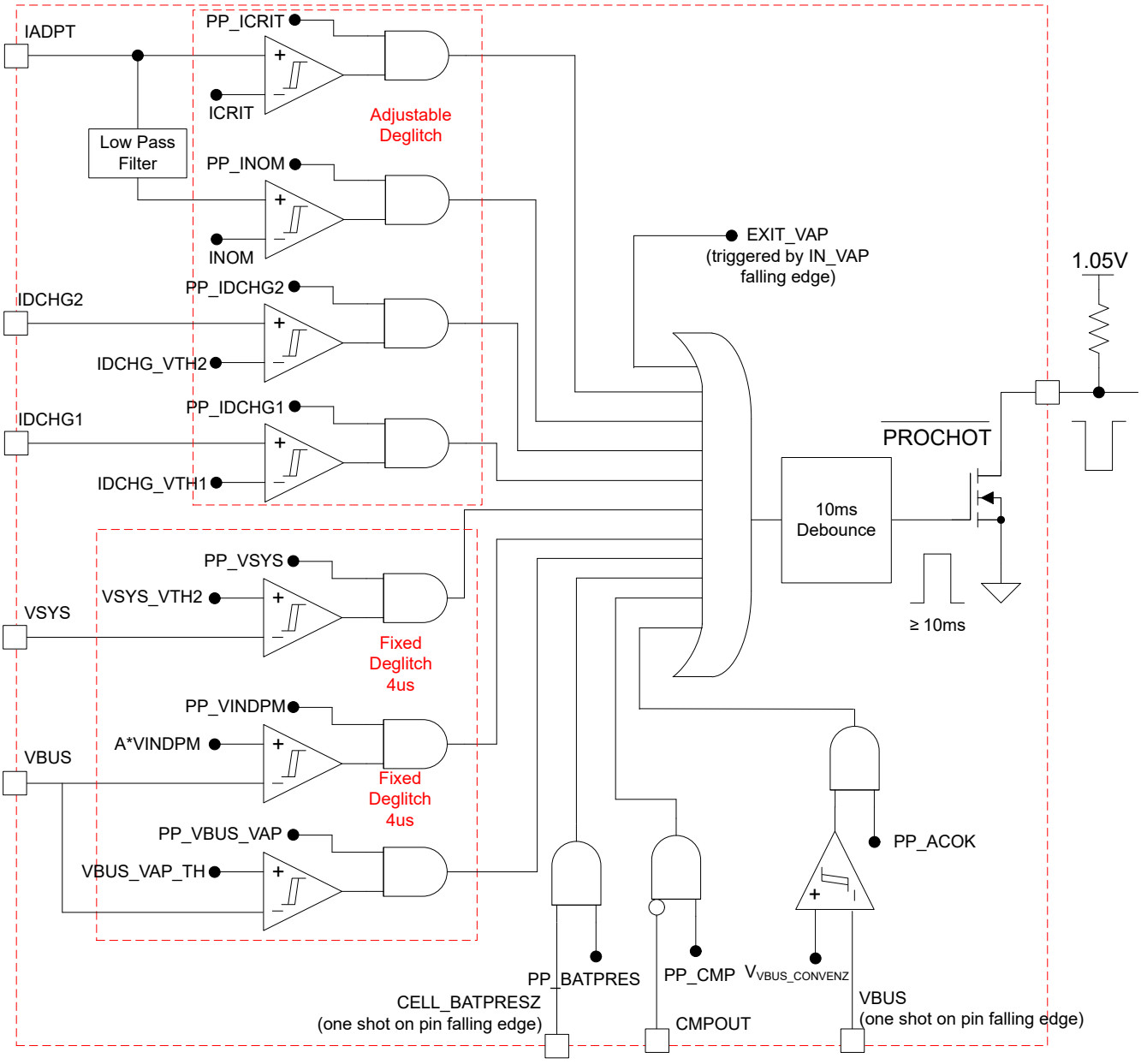


図 9-4. PROCHOT Profile

9.3.20.1 PROCHOT During Low Power Mode

During low power mode (EN_LWPWR = 1), the charger offers a low power PROCHOT function with very low quiescent current consumption (~35 µA), which uses the independent comparator to monitor the system voltage, and assert PROCHOT to CPU if the system power is too high and resulting system voltage is lower than specific threshold.

Below lists the register setting to enable $\overline{\text{PROCHOT}}$ monitoring system voltage in low power mode.

- EN_LWPWR = 1b to enable charger low power mode.
- REG0x34[7:0] = 00h
- REG0x30[6:4] = 000b
- Independent comparator threshold is always 1.2 V
- When EN_PROCHOT_LPWR = 1b, charger monitors system voltage. Connect CMPIN to voltage proportional to system voltage. $\overline{\text{PROCHOT}}$ triggers from HIGH to LOW when CMPIN voltage rises above 1.2 V.

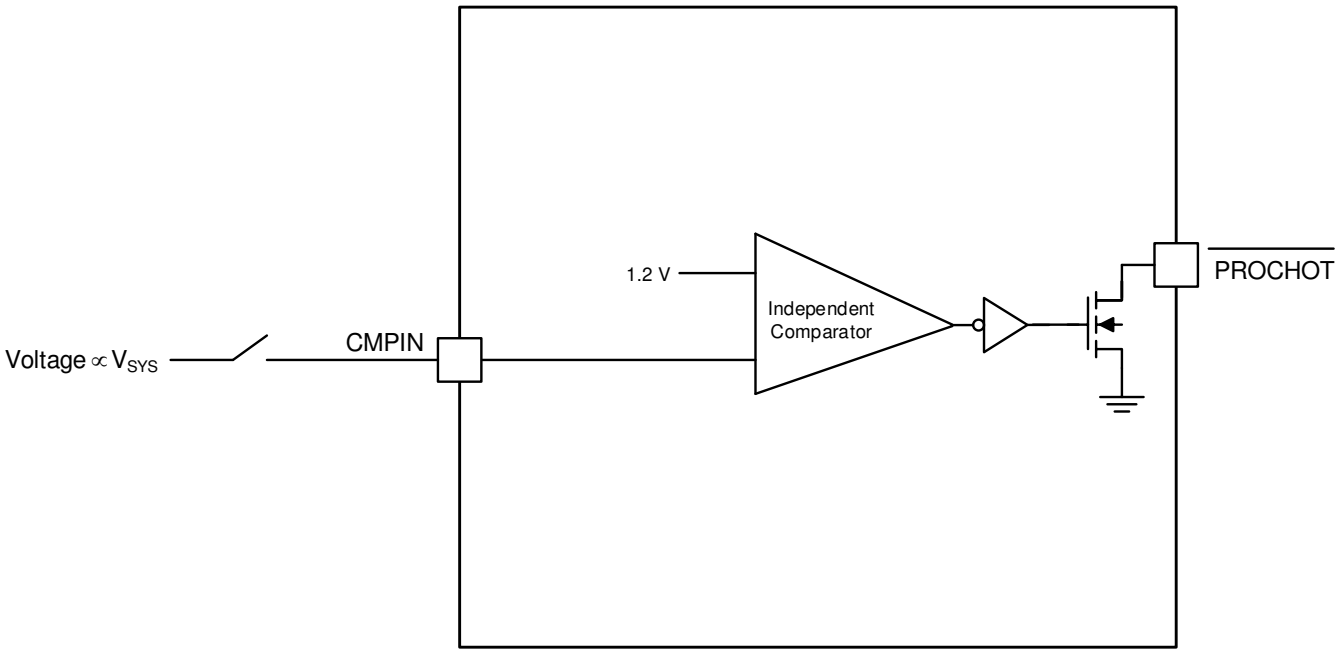


図 9-5. $\overline{\text{PROCHOT}}$ Low Power Mode Implementation

9.3.20.2 $\overline{\text{PROCHOT}}$ Status

report which event in the profile triggers $\overline{\text{PROCHOT}}$ if the corresponding bit is set to 1. The status bit can be reset back to 0 after it is read by the host, when the current $\overline{\text{PROCHOT}}$ event is not active any more.

Assume there are two $\overline{\text{PROCHOT}}$ events, event A and event B. Event A triggers $\overline{\text{PROCHOT}}$ first, but event B is also active. Both status bits will be HIGH. At the end of the 10-ms $\overline{\text{PROCHOT}}$ pulse, if any of the $\overline{\text{PROCHOT}}$ event is still active (either A or B), the $\overline{\text{PROCHOT}}$ pulse is extended.

9.3.21 Device Protection

9.3.21.1 Watchdog Timer

The charger includes a watchdog timer to terminate charging if the charger does not receive a write ChargeVoltage() or write ChargeCurrent() command within 175s (default value and adjustable via WDTMR_ADJ). When watchdog timeout occurs, all register values are kept unchanged except ChargeCurrent() resets to 256 mA . Write ChargeVoltage() or write ChargeCurrent() commands must be resent to reset watchdog timer. Writing WDTMR_ADJ = 00b to disable watchdog timer or update new watchdog timer values can also reset watchdog timer.

9.3.21.2 Input Overvoltage Protection (ACOV)

The charger has fixed ACOV voltage threshold with hysteresis. When VBUS pin voltage is higher than V_{ACOV_RISE} for more than 100 µs, it is considered as adapter overvoltage. CHRG_OK pin will be pulled low by the charger, and the converter will be disabled. When VBUS pin voltage falls below V_{ACOV_FALL} for more than 1

ms, it is considered as adapter voltage returns back to normal voltage. CHRG_OK pin is pulled high by external pull-up resistor. The converter resumes if enable conditions are valid.

9.3.21.3 Input Overcurrent Protection (ACOC)

If the input current exceeds the 1.33× or 2× of ILIM2_VTH set point ACOC_TH (adjustable through ACOC_VTH), after 250-µs rising edge de-glitch time converter stops switching because of input overcurrent protection (ACOC). ACOC is a non-latch fault, if input current falls below set point, after 250-ms falling edge de-glitch time converter starts switching again. ACOC is disabled by default and need to be enabled by configuring EN_ACOC=1b. When ACOC is triggered, its corresponding status bit Fault ACOC will be set and it can be cleared by host read.

9.3.21.4 System Overvoltage Protection (SYSOVP)

When the converter starts up, the BQ25731 reads CELL_BATPRESZ pin configuration and sets ChargeVoltage() and SYSOVP threshold (1s – 6 V, 2s – 12 V, 3s/4s – 19.5 V and 5s – 25 V). Before ChargeVoltage() is written by the host, the battery configuration will change with CELL pin voltage. When SYSOVP happens, the device latches off the converter. Fault SYSOVP status bit is set to 1. The user can clear latch-off by either writing 0 to the Fault SYSOVP status bit or removing and plugging in the adapter again. After latch-off is cleared, the converter starts again.

9.3.21.5 Battery Overvoltage Protection (BATOVP)

Battery overvoltage may happen when user plugs in a wrong battery or a wrong regulation voltage is written into ChargeVoltage() register. The BATOVP rising threshold is 104% of regulation voltage set in ChargeVoltage() register, and falling threshold is 102% of regulation voltage set in ChargeVoltage() register. When BATOVP rising condition is triggered: if charge is enabled (charge current is not 0A) converter should shut down with both HS MOSFET and LS MOSFET turned off; if charge is disabled the converter should keep operating without disturbance until battery rise up system voltage to be high enough trigger SYSOVP. There is no user status bit to monitor. Note VBAT voltage used for BATOVP detection is based on SRN pin measurement. When BATOVP is triggered with charge enabled, 40-mA discharge current is added on VSYS pin will help discharge battery voltage.

9.3.21.6 Battery Discharge Overcurrent Protection (BATOC)

The charger monitors the battery discharge current to provide the battery overcurrent protection (BATOC) through voltage across SRN and SRP. BATOC can be enabled by configuring EN_BATOC=1b. BATOC threshold is selected either 133% of IDCHG_TH2 or 200% IDCHG_TH2 through BATOC_VTH bit. The threshold is also clamped between 100 mV and 360 mV SRN-SRP cross voltage.

When discharge current is higher than the threshold after 250-µs deglitch time, BATOC fault is triggered, status bit Fault BATOC is set accordingly. Converter shuts down when BATOC is asserted to disable OTG operation and reduce discharge current.

BATOC is not a latch fault, therefore after BATOC fault is removed, with 250-ms relax time, converter resume switching automatically. But status bit Fault BATOC is only cleared by host read.

9.3.21.7 Battery Short Protection (BATSP)

For multicell operation, if BAT voltage falls below VSYS_MIN during charging, the maximum charger current is limited to 384 mA. For single-cell operation, if BAT voltage falls below 3.0 V during charging, the maximum charge current is limited to 384 mA; if BAT voltage is between 3.0 V and 3.6V then maximum charge current is limited to 2 A. Note VBAT voltage used for battery short detection is based on SRN pin measurement.

9.3.21.8 System Undervoltage Lockout (VSYS_UVP)

During converter steady state operation VSYS pin is monitoring the system voltage, when VSYS is lower than 1.6 V, there is 2-ms deglitch time, the IIN_DPM is set to 0.5 A by the charger itself. After 2-ms deglitch time, the charger should shut down and latched off. Fault VSYS_UVP bit will be set to 1 to report a system short fault. The charger only can be enabled again once the host writes Fault VSYS_UVP bit to 0b.

During converter startup after VBUS rise above V_{VBUS_CONVEN}: when VSYS is lower than 1.6 V, the IIN_DPM is set to 0.5 A by the charger itself. After VSYS rise up higher than 1.6-V threshold IIN_DPM will be released to default charger IIN_DPM setting. If after converter startup for 3 min (BQ25731), VSYS is still lower than 1.6-V threshold, then the charger should shut down and latched off. Fault VSYS_UVP bit will be set to 1 to report a system short fault. The charger only can be enabled again once the host writes Fault VSYS_UVP bit to 0b.

The charger VSYS_UVP is enabled by POR and can be disabled by writing VSYS_UVP_ENZ=1b.

9.3.21.9 Thermal Shutdown (TSHUT)

The WQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature reaches the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shut down, the REGN LDO current limit is reduced to 16 mA and stays on. When the temperature falls below 135°C, charge can be resumed with soft start.

When thermal shut down is triggered, TSHUT status bit will be triggered. This status bit keep triggered until host read to clear it. If TSHUT is still present during host read, then this bit will try to be cleared when host read but finally keep triggered because TSHUT still exists.

9.4 Device Functional Modes

9.4.1 Forward Mode

When input source is connected to VBUS, BQ25731 is in forward mode to charge 1- to 5-cell battery in constant current (CC), and constant voltage (CV) mode. Based on CELL_BATPREZ pin setting, the charger sets default battery voltage 4.2V/cell to ChargeVoltage(). According to battery capacity, the host programs appropriate charge current to ChargeCurrent() register. When battery is full or battery is not in good condition to charge, host terminates charge by setting CHRG_INHIBIT bit to 1b, or setting ChargeCurrent() to zero(WDTMR_ADJ=00 should be configured to disable watch dog timer, otherwise charge current will reset to 256 mA after watch dog timer expires).

9.4.2 USB On-The-Go

The BQ25731 supports USB OTG functionality to deliver power from the battery to other portable devices through USB port (reverse mode). The OTG output voltage is compliant with USB-C PD specification, including 5 V, 9 V, 15 V, and 20 V. The output current regulation is compliant with USB-C PD specification, including 500 mA, 1.5 A, 3 A and 5 A, and so forth.

Similar to forward operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.

9.4.3 Pass Through Mode (PTM)-Patented Technology

The charger can be operated in the pass through mode (PTM) to improve efficiency. In PTM, the Buck and Boost high-side FETs (Q1 and Q4) are both turned on, while the Buck and Boost low-side FETs are both turned off. The input power is directly passed through the charger to the system. The switching losses of MOSFETs and the inductor core loss are saved. The charger quiescent current under PTM mode is also minimized to further increase light load efficiency. Charger will be transition from normal Buck-Boost operation to PTM operation by setting EN_PTM = 1b; and will transition out of PTM mode with host control by setting EN_PTM =0b. Please contact factory for more detail information about PTM mode.

9.5 Programming

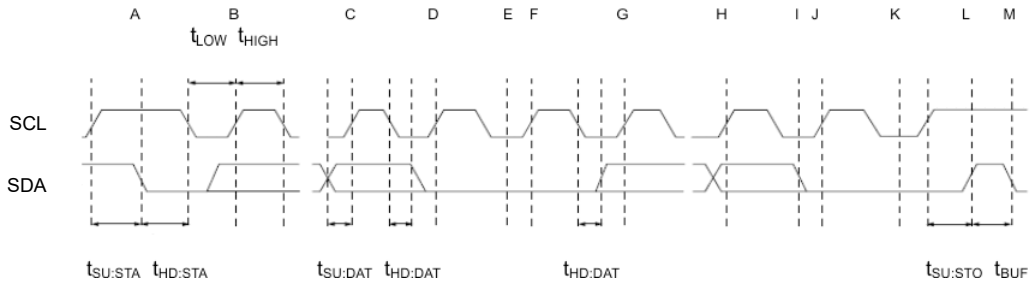
The charger supports battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in セクション 9.5.1.7. The I^2C address is 6Bh(0b1101011) consist of 7 bits. Adding read(1b) and write(0b) to the end of address 7bits, the total 8bits data format address should be D6h (1101011_0 for write)/ D7h(1101011_1 for read). The ManufacturerID and DeviceID registers are assigned to identify the charger device. The ManufacturerID register command always returns 40h.

9.5.1 I²C Serial Interface

The BQ25731 uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as host or target when performing data transfers. A host is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target device.

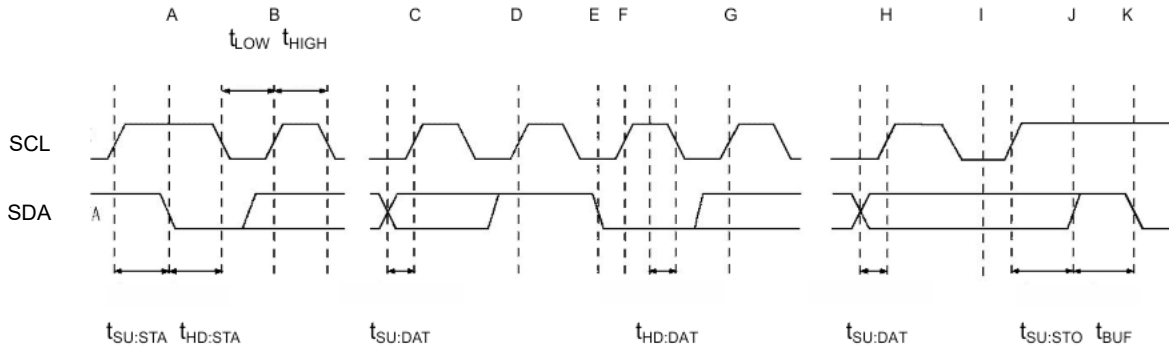
The device operates as a target device with address D6h, receiving control inputs from the host device like micro controller or a digital signal processor through REG00-REG3F. The I²C interface supports both standard mode (up to 100 kHz), and fast mode (up to 400 kHz). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

9.5.1.1 Timing Diagrams



A = Start condition
B = MSB of address clocked into target
C = LSB of address clocked into target
D = R/W bit clocked into target
E = Target pulls SDA line low
F = ACKNOWLEDGE bit clocked into host
G = MSB of data clocked into target
H = LSB of data clocked into target
I = Target pulls SDA line low
J = Acknowledge clocked into host
K = Acknowledge clock pulse
L = Stop condition, data executed by target
M = New start condition

図 9-6. I²C Write Timing



A = Start condition
B = MSB of address clocked into target
C = LSB of address clocked into target
D = R/W bit clocked into target
E = Target pulls SDA line low
G = MSB of data clocked into host
H = LSB of data clocked into host
I = Acknowledge clock pulse
J = Stop condition
K = New start condition

F = ACKNOWLEDGE bit clocked into host

図 9-7. I²C Read Timing

9.5.1.2 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

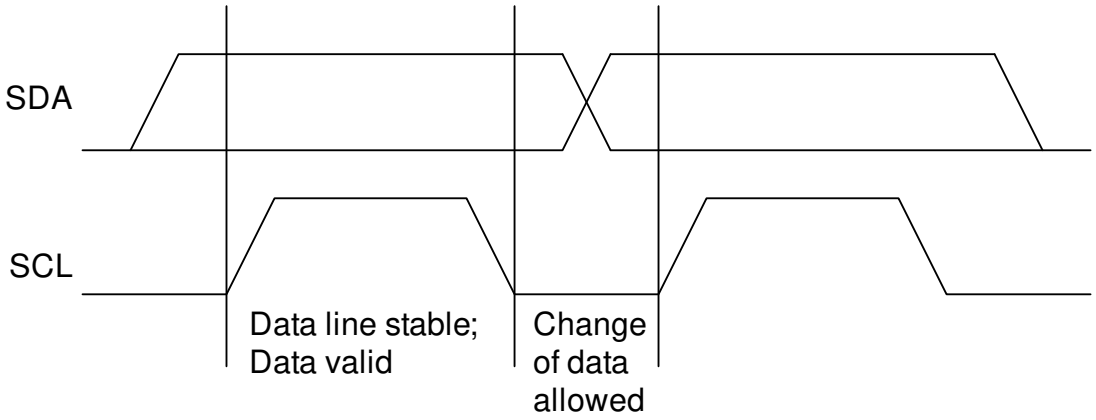


図 9-8. Bit Transfer on the I²C Bus

9.5.1.3 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

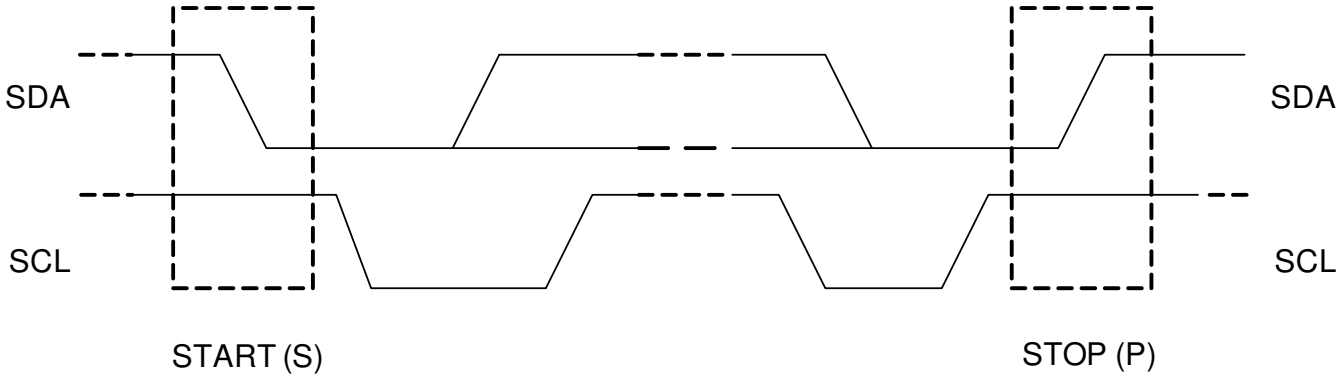


図 9-9. START and STOP Conditions

9.5.1.4 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.

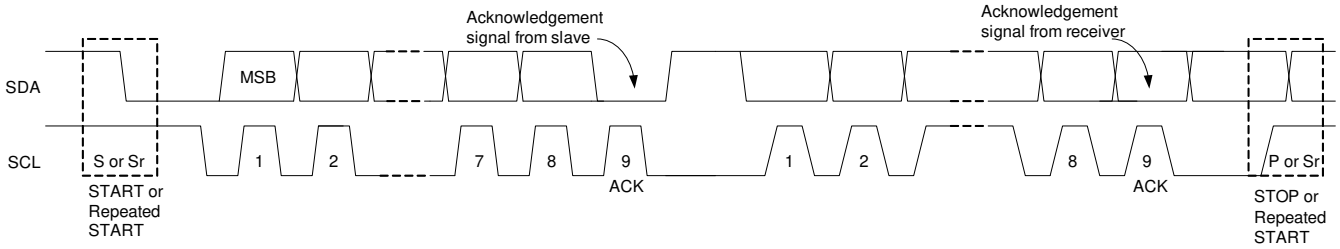


図 9-10. Data Transfer on the I²C Bus

9.5.1.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

9.5.1.6 Target Address and Data Direction Bit

After the START, a target address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

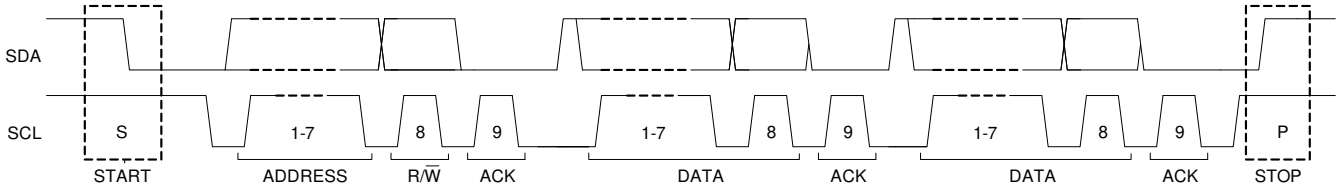


図 9-11. Complete Data Transfer

9.5.1.7 Single Read and Write

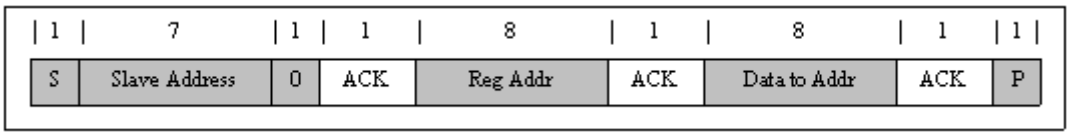


図 9-12. Single Write

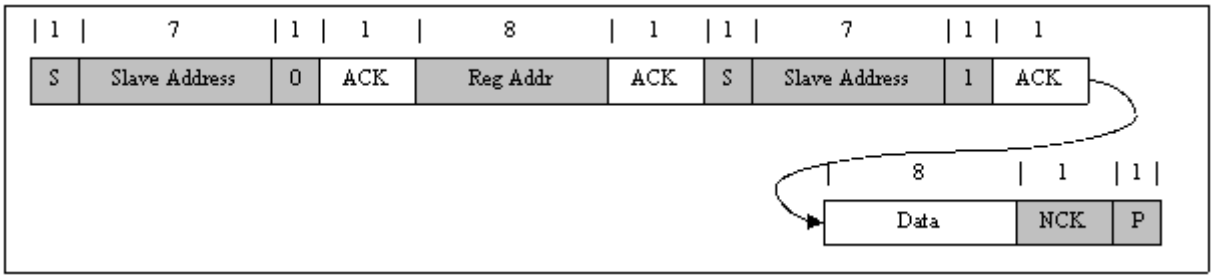


図 9-13. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

9.5.1.8 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write.

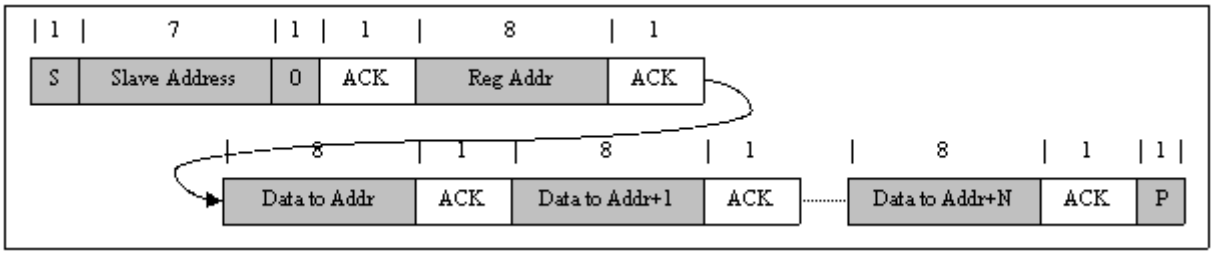


図 9-14. Multi Write

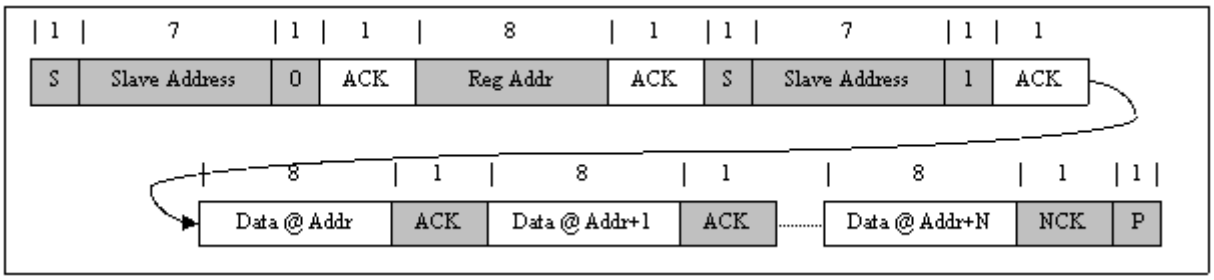


図 9-15. Multi Read

9.5.1.9 Write 2-Byte I²C Commands

A few I²C commands combine two 8-bit registers together to form a complete value. These commands include:

- ChargeCurrent()
- ChargeVoltage()
- IIN_DPM()
- OTGVoltage()
- InputVoltage()

Host has to write LSB bit first and then move on to MSB bit. No other command can be inserted in between these two writes. The charger waits for the complete write to the two registers to decide whether to accept or ignore the new value.

After the completion of LSB and MSB bytes, the two bytes will be updated at the same time. If host writes MSB byte first, the command will be ignored. If the time between write of LSB and MSB bytes exceeds watchdog timer, both the LSB and MSB commands will be ignored.

9.6 Register Map

表 9-7. Charger Command Summary

I²C ADDR (MSB/LSB)	REGISTER NAME	TYPE	DESCRIPTION	LINKS
01/00h	ChargeOption0()	R/W	Charge Option 0	Go
03/02h	ChargeCurrent()	R/W	7-bit charge current setting LSB 128 mA, Range 0 mA – 16256 mA (R_{SR}=5mΩ)	Go
05/04h	ChargeVoltage()	R/W	12-bit charge voltage setting LSB 8 mV, Default: 1S-4200mV, 2S-8400mV, 3S-12600mV, 4S-16800mV, 5S-21000mV	Go
07/06h	OTGVoltage()	R/W	12-bit OTG voltage setting LSB 8 mV, Range: 3000 mV – 24000 mV	Go
09/08h	OTGCurrent()	R/W	7-bit OTG output current setting LSB 100 mA, Range: 0 A – 12700 mA (R_{AC}=5mΩ)	Go
0B/0Ah	InputVoltage()	R/W	8-bit input voltage setting LSB 64 mV, Range: 3200 mV – 19520 mV	Go
0F/0Eh	IIN_HOST()	R/W	6-bit Input current limit set by host LSB: 100-mA, Range: 100 mA - 10000 mA with 100 mA offset (R_{AC}=5mΩ)	Go
21/20h	ChargerStatus()	R with R/W bits	Charger Status	Go
23/22h	ProchotStatus()	R and R/W bits	Prochot Status	Go
25/24h	IIN_DPM()	R	7-bit input current limit in use LSB: 50 mA, Range: 100 mA - 10000 mA (R_{AC}=5mΩ)	Go
27/26h	ADCVBUS/PSYS()	R	8-bit digital output of input voltage, 8-bit digital output of system power PSYS: Full range: 3.06 V, LSB: 12 mV VBUS: Full range: 0 V - 24.48 V, LSB 96 mV	Go
29/28h	ADCIBAT()	R	7-bit digital output of battery charge current, 7-bit digital output of battery discharge current ICHG: Full range 16.256 A, LSB 128 mA IDCHG: Full range: 65.024 A, LSB: 512 mA (R_{SR}=5mΩ)	Go
2B/2Ah	ADCIINCMPIN()	R	8-bit digital output of input current, 8-bit digital output of CMPIN voltage POR State - IIN: Full range: 25.5 A, LSB 100 mA (R_{AC}=5mΩ) CMPIN: Full range 3.06 V, LSB: 12 mV	Go
2D/2Ch	ADCVSYSVBAT()	R	8-bit digital output of system voltage, 8-bit digital output of battery voltage VSYS: Full range: 2.88 V - 19.2 V, LSB: 64 mV (1S-4S) VSYS: Full range: 8.16 V - 24.48 V, LSB: 64 mV (5S) VBAT: Full range : 2.88 V - 19.2 V, LSB 64 mV (1S-4S) VBAT: Full range : 8.16 V - 24.48 V, LSB 64 mV (5S)	Go
2Eh	ManufacturerID()	R	Manufacturer ID - 0x0040H	Go
2Fh	DeviceID()	R	Device ID	Go
31/30h	ChargeOption1()	R/W	Charge Option 1	Go
33/32h	ChargeOption2()	R/W	Charge Option 2	Go
35/34h	ChargeOption3()	R/W	Charge Option 3	Go

表 9-7. Charger Command Summary (continued)

I²C ADDR (MSB/LSB)	REGISTER NAME	TYPE	DESCRIPTION	LINKS
37/36h	ProchotOption0()	R/W	$\overline{\text{PROCHOT}}$ Option 0	Go
39/38h	ProchotOption1()	R/W	$\overline{\text{PROCHOT}}$ Option 1	Go
3B/3Ah	ADCOption()	R/W	ADC Option	Go
3D/3Ch	ChargeOption4()	R/W	Charge Option 4	Go
3F/3Eh	Vmin Active Protection()	R/W	Vmin Active Protection	Go

9.6.1 ChargeOption0 Register (I²C address = 01/00h) [reset = E70Eh]

図 9-16. ChargeOption0 Register (I²C address = 01/00h) [reset = E70Eh]

7	6	5	4	3	2	1	0
EN_LWPWR	WDTMR_ADJ		IIN_DPM_AUTO_DISABLE	OTG_ON_CHRGOK	EN_OOA	PWM_FREQ	LOW_PTM_RIPPLE
R/W	R/W		R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
EN_CMP_LATCH	VSYS_UVP_ENZ	EN_LEARN	IADPT_GAIN	IBAT_GAIN	Reserved	EN_IIN_DPM	CHRG_INHIBIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-8. ChargeOption0 Register (I²C address = 01h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_LWPWR	R/W	1b	Low Power Mode Enable, under low power mode lowest quiescent current is achieved when only battery exist. It is not recommended to enable low power mode when adapter present. 0b: Disable Low Power Mode. Device in performance mode with battery only. The $\overline{\text{PROCHOT}}$, current/power monitor buffer and comparator follow register setting. 1b: Enable Low Power Mode. Device in low power mode with battery only for lowest quiescent current. The REGN is off. The $\overline{\text{PROCHOT}}$, discharge current monitor buffer, power monitor buffer and independent comparator are disabled. ADC is not available in Low Power Mode. Independent comparator and its low power mode $\overline{\text{PROCHOT}}$ profile can be enabled by setting EN_PROCHOT_LPWR bit to 1b. <default at POR>
6-5	WDTMR_ADJ	R/W	11b	WATCHDOG Timer Adjust Set maximum delay between consecutive Host write of charge voltage or charge current command. If device does not receive a write on the REG0x15() or the REG0x14() within the watchdog time period, the charger will be suspended by setting the REG0x14() to 0 mA 256 mA (BQ25731). After expiration, the timer will resume upon the write of REG0x14(), REG0x15() or REG0x12[14:13]. 00b: Disable Watchdog Timer 01b: Enabled, 5 sec 10b: Enabled, 88 sec 11b: Enable Watchdog Timer, 175 sec <default at POR>
4	IIN_DPM_AUTO_DISABLE	R/W	0b	IIN_DPM Auto Disable When CELL_BATPRESZ pin is LOW, the charger automatically disables the IIN_DPM function by setting EN_IIN_DPM (REG0x12[1]) to 0. The host can enable IIN_DPM function later by writing EN_IIN_DPM bit (REG0x12[1]) to 1. 0b: Disable this function. IIN_DPM is not disabled when CELL_BATPRESZ goes LOW. <default at POR> 1b: Enable this function. IIN_DPM is disabled when CELL_BATPRESZ goes LOW.
3	OTG_ON_CHRGOK	R/W	0b	Add OTG to CHRG_OK Drive CHRG_OK to HIGH when the device is in OTG mode. 0b: Disable <default at POR> 1b: Enable

表 9-8. ChargeOption0 Register (I²C address = 01h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
2	EN_OOA	R/W	1b	Out-of-Audio Enable In both forward mode and OTG mode, switching frequency reduces with diminishing load, under extreme light load condition the switching frequency could be lower than 25 kHz which is already in audible frequency range. By configuring EN_OOA=1b, the minimum PFM burst frequency is clamped at around 25 kHz to avoid any audible noise. 0b: No limit of PFM burst frequency 1b: Set minimum PFM burst frequency to above 25 kHz to avoid audio noise <default at POR>
1	PWM_FREQ	R/W	1b	Switching Frequency Selection: Recommend 800 kHz with 2.2 µH, and 400 kHz with 4.7 µH. 0b: 800kHz 1b: 400 kHz<default at POR>
0	LOW_PTM_RIPPLE	R/W	1b	PTM mode input voltage and current ripple reduction 0b: Disable 1b: Enable <default at POR>

表 9-9. ChargeOption0 Register (I²C address = 00h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_CMP_LATCH	R/W	0b	The EN_CMP_LATCH bit, will latch the independent comparator output after it is triggered at low state. If enabled in PROCHOT profile REG34H[6]=1 , STAT_COMP bit REG0x21[6] keep 1b after triggered until read by host and clear 0b: Independent comparator output will not latch when it is low<default at POR> 1b: Independent comparator output will latch when it is low, host can clear CMPOUT pin by toggling this REG0x12[7] bit.
6	VSYS_UVP_ENZ	R/W	0b	To disable system under voltage protection. 0b: VSYS under voltage protection is enabled <default at POR> 1b: VSYS under voltage protection is disabled
5	EN_LEARN	R/W	0b	LEARN mode allows the battery to discharge and converter to shut off while the adapter is present . It calibrates the battery gas gauge over a complete discharge/charge cycle. When the host determines the battery voltage is below battery depletion threshold, the host switch the system back to adapter input by writing this bit back to 0b. 0b: Disable LEARN Mode <default at POR> 1b: Enable LEARN Mode
4	IADPT_GAIN	R/W	0b	IADPT Amplifier Ratio The ratio of voltage on IADPT and voltage across ACP and ACN. 0b: 20× <default at POR> 1b: 40×
3	IBAT_GAIN	R/W	1b	IBAT Amplifier Ratio The ratio of voltage on IBAT and voltage across SRP and SRN 0b: 8× 1b: 16× <default at POR>
2	Reserved	R/W	1b	Reserved

表 9-9. ChargeOption0 Register (I²C address = 00h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1	EN_IIN_DPM	R/W	1b	IIN_DPM Enable Host writes this bit to enable IIN_DPM regulation loop. When the IIN_DPM is disabled by the charger (refer to IIN_DPM_AUTO_DISABLE), this bit goes LOW. 0b: IIN_DPM disabled 1b: IIN_DPM enabled <default at POR>
0	CHRG_INHIBIT	R/W	0b	Charge Inhibit When this bit is 0, battery charging will start with valid values in the ChargeVoltage() register and the ChargeCurrent register. 0b: Enable Charge <default at POR> 1b: Inhibit Charge

9.6.2 ChargeCurrent Register (I²C address = 03/02h) [reset = 0080h]

To set the charge current, write 16-bit ChargeCurrent() command (REG0x03/02h()) using the data format listed 図 9-17.

With 5-mΩ sense resistor, the charger provides charge current range of 0 A to 16.256 A, with a 128-mA step resolution. With 10-mΩ sense resistor, the charger provides charge current range of 0 A to 8.128 A, with a 64-mA step resolution.

Upon POR, ChargeCurrent() is 0 A. Below scenarios will also reset Charge current to zero:

- CELL_BATPRESZ going LOW (battery removal).
- STAT_AC is not valid(Adapter removal).
- RESET_REG is asserted and reset all registers.
- Charge voltage is written to be 0 V.
- Watch dog event is triggered.

Charge current is not reset in force converter latch off fault (REG0x20[2]), and ACOC/TSHUT/SYSOVP/ACOV/VSYS_UVP/BATOVP/BATOC faults.

図 9-17. ChargeCurrent Register (I²C address = 03/02h) [reset = 0000h]

7	6	5	4	3	2	1	0
Reserved			Charge Current, bit 6	Charge Current, bit 5	Charge Current, bit 4	Charge Current, bit 3	Charge Current, bit 2
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Charge Current, bit 1	Charge Current, bit 0	Reserved	Reserved				
R/W	R/W	R/W	R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-10. Charge Current Register with 5-mΩ Sense Resistor (I²C address = 03h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-5	Reserved	R/W	000b	Not used. 1 = invalid write.
4	Charge Current, bit 6	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 8192 mA of charger current.
3	Charge Current, bit 5	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 4096 mA of charger current.
2	Charge Current, bit 4	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 2048 mA of charger current.
1	Charge Current, bit 3	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 1024 mA of charger current.
0	Charge Current, bit 2	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 512 mA of charger current.

表 9-11. Charge Current Register with 5-mΩ Sense Resistor (I²C address = 02h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Charge Current, bit 1	R/W	1b	0 = Adds 0 mA of charger current. 1 = Adds 256 mA of charger current.
6	Charge Current, bit 0	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 128 mA of charger current.
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

9.6.2.1 Battery Low Voltage Current Clamp

During battery voltage is low, there is current clamp implemented by converter. For 2-4 cell battery, if the battery voltage is below battery low voltage threshold(VSYS_MIN) then the charge current is clamped at 384 mA. For 1 cell battery, the battery low voltage threshold is 3 V, and the charge current is clamped at 384 mA if battery voltage is below 3V. However, during battery voltage from 3 V to 3.6 V(VSYS_MIN for 1 cell), the charge current is clamped at 2 A. Until battery voltage is above VSYS_MIN, charge current is not clamped anymore.

9.6.3 ChargeVoltage Register (I²C address = 05/04h) [reset value based on CELL_BATPRESZ pin setting]

To set the output charge voltage, write a 16-bit ChargeVoltage register command (REG0x05/04h()) using the data format listed in 図 9-18, 表 9-12, and 表 9-13. The charger provides charge voltage range from 1.024 V to 23.000 V, with 8-mV step resolution. Any write below 1.024 V or above 23.000 V is ignored.

Upon POR, ChargeVoltage() is by default set as 4200 mV for 1 s, 8400 mV for 2 s, 12600 mV for 3 s or 16800 mV for 4 s, 21000 mV for 5s. After CHRG_OK goes high, the charge will start when the host writes the charging current to ChargeCurrent() register, the default charging voltage is used if ChargeVoltage() is not programmed. If the battery is different from 4.2 V/cell, the host has to write to ChargeVoltage() before ChargeCurrent() register for correct battery voltage setting. Writing ChargeVoltage() to 0 should keep ChargeVoltage() value unchanged, and force ChargeCurrent() register to zero to disable charge.

The SRN pin senses the battery voltage for voltage regulation and should be connected as close to the battery as possible.

図 9-18. ChargeVoltage Register (I²C address = 05/04h) [reset value based on CELL_BATPRESZ pin setting]

7	6	5	4	3	2	1	0
Reserved	Charge Voltage, bit 11	Charge Voltage, bit 10	Charge Voltage, bit 9	Charge Voltage, bit 8	Charge Voltage, bit 7	Charge Voltage, bit 6	Charge Voltage, bit 5
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Charge Voltage, bit 4	Charge Voltage, bit 3	Charge Voltage, bit 2	Charge Voltage, bit 1	Charge Voltage, bit 0	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-12. ChargeVoltage Register (I²C address = 05h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Charge Voltage, bit 11	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 16384 mV of charger voltage.
5	Charge Voltage, bit 10	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 8192 mV of charger voltage
4	Charge Voltage, bit 9	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 4096 mV of charger voltage.
3	Charge Voltage, bit 8	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 2048 mV of charger voltage.
2	Charge Voltage, bit 7	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 1024 mV of charger voltage.
1	Charge Voltage, bit 6	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 512 mV of charger voltage.
0	Charge Voltage, bit 5	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 256 mV of charger voltage.

表 9-13. ChargeVoltage Register (I²C address = 04h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Charge Voltage, bit 4	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 128 mV of charger voltage.

表 9-13. ChargeVoltage Register (I²C address = 04h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
6	Charge Voltage, bit 3	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 64 mV of charger voltage.
5	Charge Voltage, bit 2	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 32 mV of charger voltage.
4	Charge Voltage, bit 1	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 16 mV of charger voltage.
3	Charge Voltage, bit 0	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 8 mV of charger voltage.
2-0	Reserved	R/W	000b	Not used. Value Ignored.

9.6.4 ChargerStatus Register (I²C address = 21/20h) [reset = 0000h]

図 9-19. ChargerStatus Register (I²C address = 21/20h) [reset = 0000h]

7	6	5	4	3	2	1	0
STAT_AC	ICO_DONE	IN_VAP	IN_VINDPM	IN_IIN_DPM	IN_FCHRG	Reserved	IN_OTG
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Fault ACOV	Fault BATOC	Fault ACOC	FAULT SYSOVP	Fault VSYS _UVP	Fault Force_Converte r_Off	Fault_OTG _OVP	Fault_OTG _UVP
R	R	R	R/W	R/W	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-14. ChargerStatus Register (I²C address = 21h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	STAT_AC	R	0b	Input source status. STAT_AC is valid as long as VBUS go within 3.5-V to 26-V range. It is different from CHRG_OK bit, When CHRG_OK is valid, STAT_AC must be valid, but if STAT_AC is valid, it is not necessary CHRG_OK is valid. There are Force converter off, ACOC, TSHUT , SYSOVP, VSYS_UVP, BATOVP can pull low CHRG_OK. 0b: Input not present 1b: Input is present
6	ICO_DONE	R	0b	After the ICO routine is successfully executed, the bit goes 1. 0b: ICO is not complete 1b: ICO is complete
5	IN_VAP	R	0b	0b: Charger is not operated in VAP mode 1b: Charger is operated in VAP mode Digital status bit indicates VAP has enabled(1) or disabled(0). The enable of VAP mode only follows the host command, which is not blocked by any status of /PROCHOT. The exit of VAP mode also follows the host command, except that any faults will exit VAP mode automatically. STAT_EXIT_VAP (REG0x21[8]) becomes 1 which will pull low /PROCHOT until host clear. The host can enable VAP by setting OTG/VAP/FRS pin high and 0x32[5]=0, disable VAP by setting either OTG/VAP/FRS pin low or 0x32[5]=1. Any faults in VAP When IN_VAP bit goes 0->1, charger should disable VINDPM, IIN_DPM, ICRIT, ILIM pin, disable PP_ACOK if it is enabled, enable PP_VSYS if it is disabled. When IN_VAP bit goes 1->0, charger should enable VINDPM, IIN_DPM, ICRIT, ILIM pin function.
4	IN_VINDPM	R	0b	0b: Charger is not in VINDPM during forward mode, or voltage regulation during OTG mode 1b: Charger is in VINDPM during forward mode, or voltage regulation during OTG mode
3	IN_IIN_DPM	R	0b	0b: Charger is not in IIN_DPM during forward mode. 1b: Charger is not in IIN_DPM during forward mode.
2	IN_FCHRG	R	0b	0b: Charger is not in fast charge 1b: Charger is in fast charger
1	Reserved	R	0b	Reserved

表 9-14. ChargerStatus Register (I²C address = 21h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
0	IN_OTG	R	0b	0b: Charger is not in OTG 1b: Charge is in OTG

表 9-15. ChargerStatus Register (I²C address = 20h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Fault ACOV	R	0b	The status are latched if triggered until a read from host. 0b: No fault 1b: ACOV
6	Fault BATOC	R	0b	The status is latched if triggered until a read from host. Fault indicator for BATOC only during normal operation. However, in PTM mode when EN_BATOC=1b, this status bit is fault indicator for both BATOVP and BATOC; when EN_BATOC=0b, this status bit is not effective. 0b: No fault 1b: BATOC is triggered
5	Fault ACOC	R	0b	The status is latched if triggered until a read from host. 0b: No fault 1b: ACOC
4	Fault SYSOVP	R/W	0b	SYSOVP Status and Clear. SYSOVP fault is latched until a clear from host by writing this bit to 0. When the SYSOVP occurs, this bit is HIGH. During the SYSOVP, the converter is disabled. After the SYSOVP is removed, the user must write a 0 to this bit or unplug the adapter to clear the SYSOVP condition to enable the converter again. 0b: Not in SYSOVP <default at POR> 1b: In SYSOVP. When SYSOVP is removed, write 0 to clear the SYSOVP latch.
3	Fault VSYS_UVP	R/W	0b	VSYS_UVP fault status and clear. VSYS_UVP fault is latched until a clear from host by writing this bit to 0. 0b: No fault <default at POR> 1b: When system voltage is lower than VSYS_UVP, then 7 times restart tries are failed.
2	Fault Force_Converter_Off	R	0b	The status is latched if triggered until a read from host. 0b: No fault 1b: Force converter off triggered (when FORCE_CONV_OFF (REG0x30[3])=1b)
1	Fault_OTG_OVP	R	0b	The status is latched if triggered until a read from host. 0b: No fault 1b: OTG OVP fault is triggered
0	Fault_OTG_UVP	R	0b	The status is latched if triggered until a read from host. 0b: No fault 1b: OTG UVP fault is triggered

9.6.5 ProchotStatus Register (I²C address = 23/22h) [reset = B800h]

All the status bits in REG0x23[7,2],REG0x23[6:0] will be cleared after host read.

図 9-20. ProchotStatus Register (I²C address = 23/22h) [reset = B800h]

7	6	5	4	3	2	1	0
Reserved	EN_PROCHOT _EXT	PROCHOT_WIDTH		PROCHOT_CL EAR	Reserved	STAT_VAP_FAI L	STAT_EXIT_VA P
R	R/W	R/W		R/W	R	R/W	R/W
7	6	5	4	3	2	1	0
STAT_VINDPM	STAT_COMP	STAT_ICRIT	STAT_INOM	STAT_IDCHG1	STAT_VSYS	STAT_BAT_Re moval	STAT_ADPT_R emoval
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-16. ProchotStatus Register (I²C address = 23h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R	1b	Reserved
6	EN_PROCHOT _EXT	R/W	0b	$\overline{\text{PROCHOT}}$ Pulse Extension Enable. When pulse extension is enabled, keep the $\overline{\text{PROCHOT}}$ pin voltage LOW until host writes PROCHOT _CLEAR = 0b. 0b: Disable pulse extension <default at POR> 1b: Enable pulse extension
5-4	PROCHOT _WIDTH	R/W	11b	$\overline{\text{PROCHOT}}$ Pulse Width Minimum $\overline{\text{PROCHOT}}$ pulse width when EN_PROCHOT _EXT = 0b 00b: 100 us 01b: 1 ms 10b: 5 ms 11b: 10 ms <default at POR>
3	PROCHOT _CLEAR	R/W	1b	$\overline{\text{PROCHOT}}$ Pulse Clear. Clear $\overline{\text{PROCHOT}}$ pulse when EN_PROCHOT _EXT = 1b. 0b: Clear $\overline{\text{PROCHOT}}$ pulse and drive $\overline{\text{PROCHOT}}$ pin HIGH 1b: Idle <default at POR>
2	TSHUT	R	0b	TSHUT trigger: 0b: TSHUT is not triggered 1b: TSHUT is triggered
1	STAT_VAP_FAIL	R/W	0b	This status bit reports a failure to load VBUS 7 consecutive times in VAP mode, which indicates the battery voltage might be not high enough to enter VAP mode, or the VAP loading current settings are too high. 0b: Not is VAP failure <default at POR> 1b: In VAP failure, the charger exits VAP mode, and latches off until the host writes this bit to 0.
0	STAT_EXIT_VAP	R/W	0b	When the charger is operated in VAP mode, it can exit VAP by either being disabled through host, or there are ACOV/ACOC/ SYSOVP/BATOVP/VSYS_UVP faults. 0b: PROCHOT_EXIT_VAP is not active <default at POR> 1b: PROCHOT_EXIT_VAP is active, $\overline{\text{PROCHOT}}$ pin is low until host writes this status bit to 0.

表 9-17. ProchotStatus Register (I²C address = 22h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	STAT_VINDPM	R/W	0b	$\overline{\text{PROCHOT}}$ Profile VINDPM status bit 0b: Not triggered 1b: Triggered, $\overline{\text{PROCHOT}}$ pin is low until host writes this status bit to 0 when PP_VINDPM = 1b
6	STAT_COMP	R	0b	$\overline{\text{PROCHOT}}$ Profile CMPOUT status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
5	STAT_ICRIT	R	0b	$\overline{\text{PROCHOT}}$ Profile ICRIT status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
4	STAT_INOM	R	0b	$\overline{\text{PROCHOT}}$ Profile INOM status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
3	STAT_IDCHG1	R	0b	$\overline{\text{PROCHOT}}$ Profile IDCHG1 status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
2	STAT_VSYS	R	0b	$\overline{\text{PROCHOT}}$ Profile VSYS status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
1	STAT_Battery_Removal	R	0b	$\overline{\text{PROCHOT}}$ Profile Battery Removal status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
0	STAT_Adapter_Removal	R	0b	$\overline{\text{PROCHOT}}$ Profile Adapter Removal status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered

9.6.6 IIN_DPM Register (I²C address = 25/24h) [reset = 4100h]

IIN_DPM register reflects the actual input current limit programmed in the register, either from IIN_HOST register or from ICO.

After ICO, the current limit used by DPM regulation may differ from the IIN_HOST register settings. The actual DPM limit is reported in IIN_DPM register.

To read the nominal or typical input current limit

- When using a 10-mΩ sense resistor (RSNS_RAC=0b). There is 50-mA offset at code 0. Note this offset is only applied to code 0, not applied to other codes.
- When using a 5-mΩ sense resistor (RSNS_RAC=1b). There is 100-mA offset at code 0. Note this offset is only applied to code 0, not applied to other codes.

To read the maximum input current limit, need to add 100 mA/200 mA offset based on above nominal input current limit reading approach.

- When using a 10-mΩ sense resistor (RSNS_RAC=0b). There is 150-mA offset at code 0 and this 150 mA offset is only applied to code 0, 100-mA offset should be added for all other non-zero codes.
- When using a 5-mΩ sense resistor (RSNS_RAC=1b). There is 300-mA offset at code 0 and this 300 mA offset is only applied to code 0, 200-mA offset should be added for all other non-zero codes

図 9-21. IIN_DPM Register with 10-mΩ Sense Resistor (I²C address = 25/24h) [reset = 4100h]

7	6	5	4	3	2	1	0
Reserved	Input Current in DPM, bit 6	Input Current in DPM, bit 5	Input Current in DPM, bit 4	Input Current in DPM, bit 3	Input Current in DPM, bit 2	Input Current in DPM, bit 1	Input Current in DPM, bit 0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-18. IIN_DPM Register with 5-mΩ Sense Resistor (I²C address = 25h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R	0b	Not used. 1 = invalid write.
6	Input Current in DPM, bit 6	R	0b	0 = Adds 0 mA of input current. 1 = Adds 6400 mA of input current.
5	Input Current in DPM, bit 5	R	0b	0 = Adds 0 mA of input current. 1 = Adds 3200 mA of input current.
4	Input Current in DPM, bit 4	R	0b	0 = Adds 0 mA of input current. 1 = Adds 1600 mA of input current.
3	Input Current in DPM, bit 3	R	0b	0 = Adds 0 mA of input current. 1 = Adds 800mA of input current
2	Input Current in DPM, bit 2	R	0b	0 = Adds 0 mA of input current. 1 = Adds 400 mA of input current.
1	Input Current in DPM, bit 1	R	0b	0 = Adds 0 mA of input current. 1 = Adds 200 mA of input current.
0	Input Current in DPM, bit 0	R	0b	0 = Adds 0 mA of input current. 1 = Adds 100 mA of input current.

表 9-19. IIN_DPM Register with 5-mΩ Sense Resistor (I²C address = 24h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R	00000000b	Not used. Value Ignored.

9.6.7 ADCVBUS/PSYS Register (I²C address = 27/26h)

- PSYS: Full range: 3.06 V, LSB: 12 mV (ADC_FULLSCALE=1b)
- PSYS: Full range: 2.04 V, LSB: 8 mV (ADC_FULLSCALE=0b)
- VBUS: Full range: 0 mV to 24480 mV, LSB: 96 mV

図 9-22. ADCVBUS/PSYS Register (I²C address = 27/26h)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-20. ADCVBUS Register (I²C address = 27h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Input Voltage

表 9-21. ADCPSYS Register (I²C address = 26h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of System Power

9.6.8 ADCIBAT Register (I²C address = 29/28h)

- ICHG: Full range when using a 10-mΩ sense resistor (RSNS_RSR=0b):8.128 A, LSB: 64 mA.
- ICHG: Full range when using a 5-mΩ sense resistor (RSNS_RSR=1b):16.256A,LSB: 128 mA.
- IDCHG: Full range when using a 10-mΩ sense resistor (RSNS_RSR=0b):32.512 A, LSB: 256 mA. Note when discharge current is higher than 32.512 A, the ADC will report 32.512 A
- IDCHG: Full range when using a 5-mΩ sense resistor (RSNS_RSR=1b):65.024A,LSB: 512 mA. Note when discharge current is higher than 65.024 A, the ADC will report 65.024 A

図 9-23. ADCIBAT Register (I²C address = 29/28h)

7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-22. ADCICHG Register (I²C address = 29h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Charge Current

表 9-23. ADCIDCHG Register (I²C address = 28h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Discharge Current

9.6.9 ADCIIN/CMPIN Register (I²C address = 2B/2Ah)

- IIN Full range: When using a 10-mΩ sense resistor (RSNS_RAC=0b): 12.75 A, LSB: 50 mA.
- IIN Full range: When using a 5-mΩ sense resistor (RSNS_RAC=1b): 25.5A, LSB:100 mA.
- CMPIN Full range: 3.06 V, LSB: 12 mV (ADC_FULLSCALE=1b)
- CMPIN Full range: 2.04 V, LSB: 8 mV (ADC_FULLSCALE=0b)

図 9-24. ADCIIN/CMPIN Register (I²C address = 2B/2Ah)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-24. ADCIIN Register (I²C address = 2Bh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Input Current

表 9-25. ADCCMPIN Register (I²C address = 2Ah) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of CMPIN voltage

9.6.10 ADCVSYS/VBAT Register (I²C address = 2D/2Ch)

- VSYS: Full range: 2.88 V to 19.2 V, LSB: 64 mV (1S-4S)
- VSYS: Full range: 8.16 V to 24.48 V, LSB: 64 mV (5S)
- VBAT: Full range: 2.88 V to 19.2 V, LSB: 64 mV (1S-4S)
- VBAT: Full range: 8.16 V to 24.48 V, LSB: 64 mV (5S)

図 9-25. ADCVSYS/VBAT Register (I²C address = 2D/2Ch)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-26. ADCVSYS Register (I²C address = 2Dh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of System Voltage

表 9-27. ADCVSYSVBAT Register (I²C address = 2Ch) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Battery Voltage

9.6.11 ChargeOption1 Register (I²C address = 31/30h) [reset = 3F00h]

図 9-26. ChargeOption1 Register (I²C address = 31/30h) [reset = 3300h]

7	6	5	4	3	2	1	0
EN_IBAT	EN_PROCHOT_LPWR	PSYS_CONFIG		RSNS_RAC	RSNS_RSR	PSYS_RATIO	EN_FAST_5MOHM
R/W	R/W	R/W		R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
CMP_REF	CMP_POL	CMP_DEG		FORCE_CONV_OFF	EN_PTM	EN_SHIP_DCHG	AUTO_WAKEUP_EN
R/W	R/W	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-28. ChargeOption1 Register (I²C address = 31h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_IBAT	R/W	0b	IBAT Enable Enable the IBAT output buffer. In low power mode (EN_LWPWR=1b), IBAT buffer is always disabled regardless of this bit value. 0b Turn off IBAT buffer to minimize Iq <default at POR> 1b: Turn on IBAT buffer
6	EN_PROCHOT_LPWR	R/W	0b	Enable $\overline{\text{PROCHOT}}$ during battery only low power mode With battery only, enable VSYS in $\overline{\text{PROCHOT}}$ with low power consumption. Do not enable this function with adapter present. Refer to セクション 9.3.20.1 for more details. 0b: Disable Independent Comparator low power $\overline{\text{PROCHOT}}$ <default at POR> 1b: Enable Independent Comparator low power $\overline{\text{PROCHOT}}$
5-4	PSYS_CONFIG	R/W	11b	PSYS Enable and Definition Register Enable PSYS sensing circuit and output buffer (whole PSYS circuit). In low power mode (EN_LWPWR=1b), PSYS sensing and buffer are always disabled regardless of this bit value. 00b: PSYS=PBUS+PBAT 01b: PSYS=PBUS 10b: Reserved 11b: Turn off PSYS buffer to minimize Iq<default at POR>
3	RSNS_RAC	R/W	1b	Input sense resistor R_{AC} 0b: 10 mΩ 1b: 5 mΩ <default at POR>
2	RSNS_RSR	R/W	1b	Charge sense resistor R_{SR} 0b: 10 mΩ 1b: 5 mΩ <default at POR>
1	PSYS_RATIO	R/W	1b	PSYS Gain Ratio of PSYS output current vs total system power 0b: 0.25 µA/W 1b: 1 µA/W <default at POR>

表 9-28. ChargeOption1 Register (I²C address = 31h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
0	EN_FAST_5MOHM	R/W	1b	Enable fast compensation to increase bandwidth under 5 mΩ RAC (RSNS_RAC=1b) for input current up to 6.4-A application (the fast compensation will only work when IADPT pin is configured less than 160 kΩ) 0b: Turn off bandwidth promotion under RSNS_RAC=1b (Note when this bit configured as 0b, IIN_HOST DAC can be extended up to 10 A, writing IIN_HOST value higher than 10 A will be neglected, the ICHG regulation loop will be slower to guarantee stability under 6.4-A to 10-A input current range) 1b: Turn on bandwidth promotion under RSNS_RAC=1b <default at POR> (Note when this bit configured as 1b, IIN_HOST DAC is clamped at 6.4 A, writing IIN_HOST value higher than 6.4 A will be neglected, the ICHG regulation loop will be faster within 6.4-A input current range)

表 9-29. ChargeOption1 Register (I²C address = 30h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CMP_REF	R/W	0b	Independent Comparator internal Reference 0b: 2.3 V <default at POR> 1b: 1.2 V
6	CMP_POL	R/W	0b	Independent Comparator output Polarity 0b: When CMPIN is above internal threshold, CMPOUT is LOW (internal hysteresis) <default at POR> 1b: When CMPIN is below internal threshold, CMPOUT is LOW (external hysteresis)
5-4	CMP_DEG	R/W	00b	Independent comparator deglitch time, only applied to the falling edge of CMPOUT (HIGH → LOW). 00b: Independent comparator is enabled with output deglitch time 5 µs <default at POR> 01b: Independent comparator is enabled with output deglitch time of 2 ms 10b: Independent comparator is enabled with output deglitch time of 20 ms 11b: Independent comparator is enabled with output deglitch time of 5 sec
3	FORCE_CONV_OFF	R/W	0b	Force Converter Off function When independent comparator triggers, (CMPOUT pin pulled down) converter latches off, at the same time, CHRG_OK signal goes LOW to notify the system. Charge current is also set to zero internally, but charge current register setting keeps the same. To get out of converter latches off, firstly the CMPOUT should be released to high and secondly FORCE_CONV_OFF bit should be cleared (=0b). 0b: Disable this function <default at POR> 1b: Enable this function
2	EN_PTM	R/W	0b	PTM enable register bit, it will automatically reset to zero 0b: disable PTM. <default at POR> 1b: enable PTM.

表 9-29. ChargeOption1 Register (I²C address = 30h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1	EN_SHIP_DCHG	R/W	0b	Discharge SRN for Shipping Mode. Used to discharge VBAT pin capacitor voltage which is necessary for battery gauge device shipping mode. When this bit is 1, discharge SRN pin down in 140 ms 20 mA. When 140 ms is over, this bit is reset to 0b automatically. If this bit is written to 0b by host before 140 ms expires, VSYS should stop discharging immediately. Note if after 140-ms SRN voltage is still not low enough for battery gauge device entering ship mode, the host may need to start a new 140-ms discharge cycle. 0b: Disable shipping mode <default at POR> 1b: Enable shipping mode
0	AUTO_WAKEUP_EN	R/W	0b	Auto Wakeup Enable When this bit is HIGH, if the battery is below VSYS_MIN , the device should automatically enable 128-mA charging current for 30 mins. When the battery is charged up above minimum system voltage, charge will terminate and the bit is reset to LOW. The charger will also exit auto wake up if host write a new charge current value to charge current register Reg0x14(). 0b: Disable <default at POR> 1b: Enable

9.6.12 ChargeOption2 Register (I²C address = 33/32h) [reset = 00B7]

図 9-27. ChargeOption2 Register (I²C address = 33/32h) [reset = 00B7]

7	6	5	4	3	2	1	0
PKPWR_TOVLD_DEG		EN_PKPWR_IIN_DPM	EN_PKPWR_VSYS	PKPWR_OVLD_STAT	PKPWR_RELAX_STAT	PKPWR_TMAX[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	
7	6	5	4	3	2	1	0
EN_EXTILIM	EN_ICHG_IDCHG	Q2_OCP	ACX_OCP	EN_ACOC	ACOC_VTH	EN_BATOC	BATOC_VTH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-30. ChargeOption2 Register (I²C address = 33h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	PKPWR_TOVLD_DEG	R/W	00b	Input Overload time in Peak Power Mode 00b: 1 ms <default at POR> 01b: 2 ms 10b: 5 ms 11b: 10 ms
5	EN_PKPWR_IIN_DPM	R/W	0b	Enable Peak Power Mode triggered by input current overshoot If REG0x33[5:4] are 00b, peak power mode is disabled. Upon adapter removal, the bits are reset to 00b. 0b: Disable peak power mode triggered by input current overshoot <default at POR> 1b: Enable peak power mode triggered by input current overshoot.
4	EN_PKPWR_VSYS	R/W	0b	Enable Peak Power Mode triggered by system voltage under-shoot If REG0x33[5:4] are 00b, peak power mode is disabled. Upon adapter removal, the bits are reset to 00b. 0b: Disable peak power mode triggered by system voltage under-shoot <default at POR> 1b: Enable peak power mode triggered by system voltage under-shoot.
3	STAT_PKPWR_OVLD	R/W	0b	Indicator that the device is in overloading cycle. Write 0 to get out of overloading cycle. 0b: Not in peak power mode. <default at POR> 1b: In peak power mode.
2	STAT_PKPWR_RELAX	R/W	0b	Indicator that the device is in relaxation cycle. Write 0 to get out of relaxation cycle. 0b: Not in relaxation cycle. <default at POR> 1b: In relaxation mode.
1-0	PKPWR_TMAX[1:0]	R/W	00b	Peak power mode overload and relax cycle time. 00b: 20 ms <default at POR> 01b: 40 ms 10b: 80 ms 11b: 1 sec

表 9-31. ChargeOption2 Register (I²C address = 32h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_EXTILIM	R/W	1b	Enable ILIM_HIZ pin to set input current limit 0b: Input current limit is set by IIN_DPM register.. 1b: Input current limit is set by the lower value of ILIM_HIZ pin and IIN_DPM register.. <default at POR>
6	EN_ICHG_IDCHG	R/W	0b	0b: IBAT pin as discharge current. <default at POR> 1b: IBAT pin as charge current.
5	Q2_OCP	R/W	1b	Q2 OCP threshold by sensing Q2 VDS 0b: 210 mV 1b: 150 mV <default at POR>
4	ACX_OCP	R/W	1b	Fixed Input current OCP threshold by sensing ACP-ACN, converter is disabled immediately when triggered non latch protection resume switching automatically after ACX comparator release. 0b: 280 mV(RSNS_RAC=0b)/200 mV(RSNS_RAC=1b) 1b: 150 mV(RSNS_RAC=0b)/100 mV(RSNS_RAC=1b) <default at POR>
3	EN_ACOC	R/W	0b	ACOC Enable Configurable Input overcurrent (ACOC) protection by sensing the voltage across ACP and ACN. Upon ACOC (after 250-µs blank-out time), converter is disabled. Non latch fault, after 250-ms falling edge de-glitch time converter starts switching automatically. 0b: Disable ACOC <default at POR> 1b: ACOC threshold 133% or 200% ILIM2
2	ACOC_VTH	R/W	1b	ACOC Limit Set MOSFET OCP threshold as percentage of IIN_DPM with current sensed from $R_{AC.}$ 0b: 133% of ILIM2 1b: 200% of ILIM2 <default at POR>
1	EN_BATOC	R/W	1b	BATOC Battery discharge overcurrent (BATOC) protection by sensing the voltage across SRN and SRP. Upon BATOC, converter is disabled. 0b: Disable BATOC 1b: Enable BATOC threshold 133% or 200% $\overline{\text{PROCHOT}}$ IDCHG_TH2 <default at POR>
0	BATOC_VTH	R/W	1b	Set battery discharge overcurrent threshold as percentage of $\overline{\text{PROCHOT}}$ battery discharge current limit. Note when SRN and SRP common voltage is low for 1S application, the BATOC threshold could be derating. 0b: 133% of $\overline{\text{PROCHOT}}$ IDCHG_TH2 1b: 200% of $\overline{\text{PROCHOT}}$ IDCHG _TH2<default at POR>

9.6.13 ChargeOption3 Register (I²C address = 35/34h) [reset = 0434h]

図 9-28. ChargeOption3 Register (I²C address = 35/34h) [reset = 0434h]

7	6	5	4	3	2	1	0
EN_HIZ	RESET_REG	RESET_VINDPM	EN_OTG	EN_ICO_MODE	Reserved	Reserved	EN_OTG_BIGCAP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved	EN_VBUS_VAP	OTG_VAP_MODE	IL_AVG		CMP_EN	Reserved	PSYS_OTG_IDCHG
R/W	R/W	R/W	R/W		R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-32. ChargeOption3 Register (I²C address = 35h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_HIZ	R/W	0b	Device HIZ Mode Enable When the charger is in HIZ mode, the device draws minimal quiescent current. With VBUS above UVLO. REGN LDO stays on, and system powers from battery. 0b: Device not in HIZ mode <default at POR> 1b: Device in HIZ mode
6	RESET_REG	R/W	0b	Reset Registers All the registers are reset to POR default setting except the VINDPM register. 0b: Idle <default at POR> 1b: Reset all the registers to default values. After reset, this bit goes back to 0.
5	RESET_VINDPM	R/W	0b	Reset VINDPM Threshold 0b: Idle 1b: Converter is disabled to measure VINDPM threshold. After VINDPM measurement is done, this bit goes back to 0 and converter starts.
4	EN_OTG	R/W	0b	OTG Mode Enable Enable device in OTG mode when OTG/VAP/FRS pin is HIGH. 0b: Disable OTG <default at POR> 1b: Enable OTG mode to supply VBUS from battery.
3	EN_ICO_MODE	R/W	0b	Enable ICO Algorithm 0b: Disable ICO algorithm. <default at POR> 1b: Enable ICO algorithm.
2	Reserved	R/W	1b	Reserved
1	Reserved	R/W	0b	Reserved
0	EN_OTG_BIGCAP	R/W	0b	Enable OTG compensation for VBUS effective capacitance larger than 33 µF 0b: Disable OTG large VBUS capacitance compensation (Recommended for VBUS effective capacitance smaller than 33 µF) <default at POR> 1b: Enable OTG large VBUS capacitance compensation (Recommended for VBUS effective capacitance larger than 33 µF)

表 9-33. ChargeOption3 Register (I²C address = 34h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Reserved

表 9-33. ChargeOption3 Register (I²C address = 34h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
6	EN_VBUS_VAP	R/W	0b	Enable the VBUS VAP for VAP operation mode 2&3 0b: Disabled <default at POR> 1b: Enabled
5	OTG_VAP_MODE	R/W	1b	The selection of the external OTG/VAP/FRS pin control. Don't recommend to change pin control after OTG/VAP/FRS pin is pulled high. 0b: the external OTG/VAP/FRS pin controls the EN/DIS VAP mode 1b: the external OTG/VAP/FRS pin controls the EN/DIS OTG mode <default at POR>
4-3	IL_AVG	R/W	10b	Converter inductor average current clamp. It is recommended to choose the smallest option which is higher than maximum possible converter average inductor current. 00b: 6A 01b: 10A 10b: 15A <default at POR> 11b: Disabled
2	CMP_EN	R/W	1b	Enable Independent Comparator with effective low. 0b: Disabled 1b: Enabled <default at POR>
1	Reserved	R/W	0b	Reserved
0	PSYS_OTG_IDCHG	R/W	0b	PSYS function during OTG mode. 0b: PSYS as battery discharge power minus OTG output power <default at POR> 1b: PSYS as battery discharge power only

9.6.14 ProchotOption0 Register (I²C address = 37/36h) [reset = 4A81h(2S~5s) 4A09(1S)]

To set VSYS_TH1 threshold to trigger discharging VBUS in VAP mode, write a 6-bit Vmin Active Protection register command (REG0x37<7:2>()) using the data format listed in 図 9-29, 表 9-34, and 表 9-35. The charger Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. The threshold range from 3.2 V (000000b) to 9.5 V (111111b) for 2s~5s and 3.2 V (000000b) to 3.9 V (000111b) for 1S, with 100-mV step resolution. There is a fixed DC offset which is 3.2 V. Under 1S application writing beyond 3.9 V will be ignored. For example 000111b and xxx111b result in same VSYS_TH1 setting 3.9 V. Upon POR, the VSYS_TH1 threshold to trigger VBUS discharge in VAP mode is 3.4 V (000010b) for 1S and 6.400 V (100000b) for 2s~5s.

図 9-29. ProchotOption0 Register (I²C address = 37/36h) [reset = 4A81h(2S~5s) 4A09(1S)]

7	6	5	4	3	2	1	0
ILIM2_VTH					ICRIT_DEG		PROCHOT_VINDPM_80_90
R/W	R/W	R/W	R/W	R/W	R/W		R/W
7	6	5	4	3	2	1	0
VSYS_TH1						INOM_DEG	LOWER_PROCHOT_VINDPM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-34. ProchotOption0 Register (I²C address = 37h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-3	ILIM2_VTH	R/W	01001b	I_{LIM2} Threshold 5 bits, percentage of IIN_DPM in 0x22H. Measure current between ACP and ACN. Trigger when the current is above this threshold: 00001b - 11001b: 110% - 230%, step 5% 11010b - 11110b: 250% - 450%, step 50% 11111b: Out of Range (Ignored) Default 150%, or 01001
2-1	ICRIT_DEG	R/W	01b	ICRIT Deglitch time ICRIT threshold is set to be 110% of I_{LIM2}. Typical ICRIT deglitch time to trigger $\overline{PROCHOT}$. 00b: 15 µs 01b: 100 µs <default at POR> 10b: 400 µs (max 500 µs) 11b: 800 µs (max 1 ms)
0	PROCHOT_VINDPM_80_90	R/W	0b	Lower threshold of the PROCHOT_VINDPM comparator When REG0x33[0]=1, the threshold of the PROCHOT_VINDPM comparator is determined by this bit setting. 0b: 83% of VinDPM threshold <default at POR>. 1b: 91% of VinDPM threshold

表 9-35. ProchotOption0 Register (I²C address = 36h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-2	VSYS_TH1	R/W	100000b(2S~5s) 000010b(1S)	VSYS Threshold to trigger discharging VBUS in VAP mode. Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. There is a fixed DC offset which is 3.2 V. 2S - 5s battery (Default: 6.4 V) 000000b- 111111b: 3.2 V - 9.5 V with 100-mV step size. 1S battery (Default: 3.4 V) XXX000b - XXX111b: 3.2 V - 3.9 V with 100-mV step size.
1	INOM_DEG	R/W	0b	INOM Deglitch Time INOM is always 10% above IIN_DPM register setting. Measure current between ACP and ACN. Trigger when the current is above this threshold. 0b: 1 ms(max) <default at POR> 1b: 60 ms(max)
0	LOWER_PROCHOT_VINDPM	R/W	1b	Enable the lower threshold of the PROCHOT_VINDPM comparator 0b: the threshold of the PROCHOT_VINDPM comparator follows the same VINDPM REG0x3D() setting. 1b: the threshold of the PROCHOT_VINDPM comparator is lower and determined by PROCHOT_VINDPM_80_90 bit setting. <default at POR>

9.6.15 ProchotOption1 Register (I²C address = 39/38h) [reset = 41A0h]

図 9-30. ProchotOption1 Register (I²C address = 39/38h) [reset = 41A0h]

7	6	5	4	3	2	1	0
IDCHG_TH1						IDCHG_DEG1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
PP_VINDPM	PP_COMP	PP_ICRIT	PP_INOM	PP_IDCHG1	PP_VSYS	PP_BATPRES	PP_ACOK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When the REG0x38h[7:0] are set to be disabled, the $\overline{\text{PROCHOT}}$ event associated with that bit will not be reported in the $\overline{\text{PROCHOT}}$ status register REG0x22h[7:0] any more, and the $\overline{\text{PROCHOT}}$ pin will not be pulled low any more if the event happens.

表 9-36. ProchotOption1 Register (I²C address = 39h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-2	IDCHG_TH1	R/W	010000b	IDCHG level 1 Threshold 6 bit, range, range 0 A to 64512 mA, step 1024 mA. Measure current between SRN and SRP. Trigger when the discharge current is above the threshold. If the value is programmed to 000000b $\overline{\text{PROCHOT}}$ is always triggered. Default: 16256 mA or 010000b
1-0	IDCHG_DEG1	R/W	00b	IDCHG level 1 Deglitch Time 00b: 78 ms 01b: 1.25s <default at POR> 10b: 5s 11b: 20s

表 9-37. ProchotOption1 Register (I²C address = 38h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	PP_VINDPM	R/W	1b	VINDPM $\overline{\text{PROCHOT}}$ Profile When all the REG0x38[7:0] , REG0x3D[1], REG0x3C[2]bits are 0, $\overline{\text{PROCHOT}}$ function is disabled. 0b: disable 1b: enable<default at POR>
6	PP_COMP	R/W	0b	Independent comparator $\overline{\text{PROCHOT}}$ Profile When not in low power mode(Battery only), use this bit to control independent comparator PROCHOT profiles. When in low power mode(Battery only), this bit will lose controllability to independent comparator PROCHOT profiles. Need to use EN_PROCHOT_LPWR to enable independent comparator and its PROCHOT profile. 0b: disable <default at POR> 1b: enable
5	PP_ICRIT	R/W	1b	ICRIT $\overline{\text{PROCHOT}}$ Profile 0b: disable 1b: enable <default at POR>

表 9-37. ProchotOption1 Register (I²C address = 38h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
4	PP_INOM	R/W	0b	INOM $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable
3	PP_IDCHG1	R/W	0b	IDCHG1 $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable
2	PP_VSYS	R/W	0b	VSYS $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable
1	PP_BATPRES	R/W	0b	Battery removal $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable (one-shot falling edge triggered) If BATPRES is enabled in $\overline{\text{PROCHOT}}$ after the battery is removed, it will immediately send out one-shot $\overline{\text{PROCHOT}}$ pulse.
0	PP_ACOK	R/W	0b	Adapter removal $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable EN_LWPWR= 0b to assert $\overline{\text{PROCHOT}}$ pulse after adapter removal. If PP_ACOK is enabled in $\overline{\text{PROCHOT}}$ after the adapter is removed, it will be pulled low.

9.6.16 ADCOption Register (I²C address = 3B/3Ah) [reset = 2000h]

図 9-31. ADCOption Register (I²C address = 3B/3Ah) [reset = 2000h]

7	6	5	4	3	2	1	0
ADC_CONV	ADC_START	ADC_FULLSCALE	Reserved				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
EN_ADC_CMPIN	EN_ADC_VBUS	EN_ADC_PSYS	EN_ADC_IIN	EN_ADC_IDCHG	EN_ADC_ICHG	EN_ADC_VSYS	EN_ADC_VBAT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The ADC registers are read in the following order: VBAT, VSYS, ICHG, IDCHG, IIN, PSYS, VBUS, CMPIN. ADC is disabled in low power mode. Before enabling ADC, low power mode should be disabled first.

表 9-38. ADCOption Register (I²C address = 3Bh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ADC_CONV	R/W	0b	Typical each ADC channel conversion time is 25 ms maximum. Total ADC conversion time is the product of 25 ms and enabled channel counts. 0b: One-shot update. Do one set of conversion updates to registers REG0x29/28(), REG0x27/26(), REG0x2B/2A(), and REG0x2D/2C() after ADC_START = 1. 1b: Continuous update. Do a set of conversion updates to registers REG0x29/28(), REG0x27/26(), REG0x2B/2A(), and REG0x2D/2C()every 1 sec.
6	ADC_START	R/W	0b	0b: No ADC conversion 1b: Start ADC conversion. After the one-shot update is complete, this bit automatically resets to zero
5	ADC_FULLSCALE	R/W	1b	ADC input voltage range adjustment for PSYS and CMPIN ADC Channels. 2.04-V full scale holds 8 mV/LSB resolution and 3.06-V full scale holds 12 mV/LSB resolution 0b: 2.04 V 1b: 3.06 V <default at POR>(Not accurate for REGN<6-V application (VBUS & VSYS< 6V))
4-0	Reserved	R/W	00000b	Reserved

表 9-39. ADCOption Register (I²C address = 3Ah) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_ADC_CMPIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
6	EN_ADC_VBUS	R/W	0b	0b: Disable <default at POR> 1b: Enable
5	EN_ADC_PSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
4	EN_ADC_IIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
3	EN_ADC_IDCHG	R/W	0b	0b: Disable <default at POR> 1b: Enable

表 9-39. ADCOption Register (I²C address = 3Ah) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
2	EN_ADC_ICHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
1	EN_ADC_VSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
0	EN_ADC_VBAT	R/W	0b	0b: Disable <default at POR> 1b: Enable

9.6.17 ChargeOption4 Register (I²C address = 3D/3Ch) [reset = 0048h]

図 9-32. ChargeOption4 Register (I²C address = 3D/3Ch) [reset = 0048h]

7	6	5	4	3	2	1	0
Reserved			EN_Dither		Reserved	PP_VBUS_VAP	STAT_VBUS_VAP
R/W			R/W		R/W	R/W	R
7	6	5	4	3	2	1	0
IDCHG_DEG2		IDCHG_TH2			PP_IDCHG2	STAT_IDCHG2	STAT_PTM
R/W		R/W			R/W	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-40. ChargeOption4 Register (I²C address = 3Dh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-5	Reserved	R/W	000b	Reserved
4-3	EN_DITHER	R/W	00b	Frequency Dither configuration 00b: Disable Dithering<default at POR> 01b: Dither 1X (±2% Fs dithering range) 10b: Dither 2X (±4% Fs dithering range) 11b: Dither 3X (±6% Fs dithering range)
2	Reserved	R/W	0b	Reserved
1	PP_VBUS_VAP	R/W	0b	VBUS_VAP $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 0b: enable
0	STAT_VBUS_VAP	R	0b	$\overline{\text{PROCHOT}}$ profile VBUS_VAP status bit. The status is latched until a read from host. 0b: Not triggered <default at POR> 1b: Triggered

表 9-41. ChargeOption4 Register (I²C address = 3Ch) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	IDCHG_DEG2	R/W	01b	Battery discharge current limit 2 deglitch time(minimum value) 00b: 100 µs 01b: 1.6 ms <default at POR> 10b: 6 ms 11b: 12 ms
5-3	IDCHG_TH2	R/W	001b	Battery discharge current limit2 based on percentage of IDCHG_TH1. Note IDCHG_TH2 setting higher than 32256 mA should lose accuracy de-rating between target value and 32256 mA. (Recommend not to set higher than 20 A for 1S OTG boost operation) 000b: 125% IDCHG_TH1 001b: 150% IDCHG_TH1 <default at POR> 010b: 175% IDCHG_TH1 011b: 200% IDCHG_TH1 100b: 250% IDCHG_TH1 101b: 300% IDCHG_TH1 110b: 350% IDCHG_TH1 111b: 400% IDCHG_TH1
2	PP_IDCHG2	R/W	0b	IDCHG2 $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable

表 9-41. ChargeOption4 Register (I²C address = 3Ch) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1	STAT_IDCHG2	R	0b	The status is latched until a read from host. 0b: Not triggered <default at POR> 1b: Triggered
0	STAT_PTM	R	0b	PTM operation status bit monitor 0b: Not in PTM Operation <default at POR> 1b: In PTM Operation

9.6.18 Vmin Active Protection Register (I²C address = 3F/3Eh) [reset = 006Ch(2s~5s)/0004h(1S)]

To set the VAP VBUS $\overline{\text{PROCHOT}}$ trigger threshold, write a 7-bit Vmin Active Protection register command (REG0x3F[7:1]) using the data format listed in 図 9-33 and 表 9-42. The charger provides VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger threshold range from 3.2 V (0000000b) to 15.9 V (1111111b), with 100-mV step resolution. There is a fixed offset of 3.2 V. Upon POR, the VBUS $\overline{\text{PROCHOT}}$ trigger threshold is 3.2 V (0000000b).

To set VSYS_TH2 Threshold to assert STAT_VSYS, write a 6-bit Vmin Active Protection register command (REG0x3E[7:2]) using the data format listed in 図 9-33 and 表 9-43. The charger Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. The threshold range from 3.2 V (000000b) to 9.5 V (111111b) for 2s~5s and 3.2 V (000000b) to 3.9 V (000111b) for 1S, with 100-mV step resolution. There is a fixed DC offset which is 3.2 V. Under 1S application writing beyond 3.9 V will be ignored. For example, xxx111b and 000111b result in same VSYS_TH2 setting 3.9 V. Upon POR, the VSYS $\overline{\text{PROCHOT}}$ trigger threshold is 3.2 V (000000b) for 1S and 5.9 V (011011b) for 2s~5s .

図 9-33. Vmin Active Protection Register (I²C address = 3F/3Eh) [reset = 0070h/0004h]

7	6	5	4	3	2	1	0
VBUS_VAP_TH Bit6	VBUS_VAP_TH Bit5	VBUS_VAP_TH Bit4	VBUS_VAP_TH Bit3	VBUS_VAP_TH Bit2	VBUS_VAP_TH Bit1	VBUS_VAP_TH Bit0	Reserved
R/W							R/W
7	6	5	4	3	2	1	0
VSYS_TH2 Bit6	VSYS_TH2 Bit5	VSYS_TH2 Bit4	VSYS_TH2 Bit3	VSYS_TH2 Bit2	VSYS_TH2 Bit1	EN_TH2_FOLLOW_TH1	EN_FRS
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-42. Vmin Active Protection Register (I²C address = 3Fh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	VBUS_VAP_TH, Bit6	R/W	0b	0 = Adds 0 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 6400 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
6	VBUS_VAP_TH, Bit5	R/W	0b	0 = Adds 0 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 3200 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
5	VBUS_VAP_TH, Bit4	R/W	0b	0 = Adds 0 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 1600 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
4	VBUS_VAP_TH, Bit3	R/W	0b	0 = Adds 0 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 800 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
3	VBUS_VAP_TH, Bit2	R/W	0b	0 = Adds 0 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 400 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
2	VBUS_VAP_TH, Bit1	R/W	0b	0 = Adds 0 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 200 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
1	VBUS_VAP_TH, Bit0	R/W	0b	0 = Adds 0 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 100 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
0	Reserve	R/W	0b	Reserve

表 9-43. Vmin Active Protection Register (I^2C address = 3Eh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	VSYS_TH2, Bit5	R/W	0b	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 3200 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
6	VSYS_TH2, Bit4	R/W	1b(2S~5s) 0b(1S)	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 1600 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
5	VSYS_TH2, Bit3	R/W	1b(2S~5s) 0b(1S)	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 800 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
4	VSYS_TH2, Bit2	R/W	0b	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 400 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
3	VSYS_TH2, Bit1	R/W	0b(1S) 1b(2S~5s)	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 200 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
2	VSYS_TH2, Bit0	R/W	1b	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 100 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
1	EN_VSYSTH2_FOLLOW_VSYSTH1	R/W	0b	Enable internal VSYS_TH2 follow VSYS_TH1 setting neglecting register REG37[7:2] setting 0b: disable <default at POR> 1b: enable
0	EN_FRS	R/W	0b	Fast Role Swap feature enable (note not recommend to change EN_FRS during OTG operation, the FRS bit from 0 to 1 change will disable power stage for about 200 µs (Fs = 400 kHz). HIZ mode holds higher priority, If EN_HIZ=1b, this EN_FRS bit should be forced to 0b. 0b: disable <default at POR> 1b: enable

9.6.19 OTGVoltage Register (I²C address = 07/06h) [reset = 09C4h]

To set the OTG output voltage limit, write to REG0x07/06h() using the data format listed in 図 9-34, 表 9-44, and 表 9-45.

The DAC is clamped in digital core at minimal 3 V and maximum 24.0 V during normal OTG operation. Any register writing lower than the minimal or higher than the maximum will be ignored.

図 9-34. OTGVoltage Register (I²C address = 07/06h) [reset = 09C4h]

7	6	5	4	3	2	1	0
Reserved		OTG Voltage, bit 11	OTG Voltage, bit 10	OTG Voltage, bit 9	OTG Voltage, bit 8	OTG Voltage, bit 7	OTG Voltage, bit 6
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
OTG Voltage, bit 5	OTG Voltage, bit 4	OTG Voltage, bit 3	OTG Voltage, bit 2	OTG Voltage, bit 1	OTG Voltage, bit 0	Reserved	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-44. OTGVoltage Register (I²C address = 07h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	Reserved	R/W	00b	Not used. 1 = invalid write.
13	OTG Voltage, bit 11	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 16384 mV of OTG voltage.
12	OTG Voltage, bit 10	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 8192 mV of OTG voltage.
11	OTG Voltage, bit 9	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 4096 mV of OTG voltage.
10	OTG Voltage, bit 8	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 2048 mV of OTG voltage.
9	OTG Voltage, bit 7	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 1024 mV of OTG voltage.
8	OTG Voltage, bit 6	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 512 mV of OTG voltage.

表 9-45. OTGVoltage Register (I²C address = 06h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	OTG Voltage, bit 5	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 256 mV of OTG voltage.
6	OTG Voltage, bit 4	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 128 mV of OTG voltage.
5	OTG Voltage, bit 3	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 64 mV of OTG voltage.
4	OTG Voltage, bit 2	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 32 mV of OTG voltage.
3	OTG Voltage, bit 1	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 16 mV of OTG voltage.
2	OTG Voltage, bit 0	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 8 mV of OTG voltage.

表 9-45. OTGVoltage Register (I²C address = 06h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1-0	Reserved	R/W	00b	Not used. Value Ignored.

9.6.20 OTGCurrent Register (I²C address = 09/08h) [reset = 3C00h]

To set the OTG output current limit, write to REG0x09() using the data format listed in 図 9-35 and 表 9-46.

図 9-35. OTGCurrent Register (I²C address = 09/08h) [reset = 3C00h]

7	6	5	4	3	2	1	0
Reserved	OTG Current set by host, bit 6	OTG Current set by host, bit 5	OTG Current set by host, bit 4	OTG Current set by host, bit 3	OTG Current set by host, bit 2	OTG Current set by host, bit 1	OTG Current set by host, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-46. OTGCurrent Register (I²C address = 09h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	OTG Current set by host, bit 6	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 3200 mA of OTG current.
5	OTG Current set by host, bit 5	R/W	1b	0 = Adds 0 mA of OTG current. 1 = Adds 1600 mA of OTG current.
4	OTG Current set by host, bit 4	R/W	1b	0 = Adds 0 mA of OTG current. 1 = Adds 800 mA of OTG current.
3	OTG Current set by host, bit 3	R/W	1b	0 = Adds 0 mA of OTG current. 1 = Adds 400 mA of OTG current.
2	OTG Current set by host, bit 2	R/W	1b	0 = Adds 0 mA of OTG current. 1 = Adds 200 mA of OTG current.
1	OTG Current set by host, bit 1	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 100 mA of OTG current.
0	OTG Current set by host, bit 0	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 50 mA of OTG current.

表 9-47. OTGCurrent Register (I²C address = 08h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R/W	00000000b	Not used. Value Ignored.

9.6.21 InputVoltage(VINDPM) Register (I²C address = 0B/0Ah) [reset =VBUS-1.28V]

To set the input voltage limit, write a 16-bit InputVoltage register command (REG0x0B/0A()) using the data format listed in 図 9-36, 表 9-48, and 表 9-49.

If the input voltage drops more than the InputVoltage register allows, the device enters VINDPM and reduces the charge current. The default setting is 1.28 V below the no-load VBUS voltage. There is a fixed DC offset 3.2 V for all codes.

図 9-36. InputVoltage Register (I²C address = 0B/0Ah) [reset = VBUS-1.28V]

7	6	5	4	3	2	1	0
Reserved		Input Voltage, bit 7	Input Voltage, bit 6	Input Voltage, bit 5	Input Voltage, bit 4	Input Voltage, bit 3	Input Voltage, bit 2
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Input Voltage, bit 1	Input Voltage, bit 0	Reserved					
R/W	R/W	R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-48. InputVoltage Register (I²C address = 0Bh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	Reserved	R/W	00b	Not used. 1 = invalid write.
5	Input Voltage, bit 7	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 8192 mV of input voltage.
4	Input Voltage, bit 6	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 4096 mV of input voltage.
3	Input Voltage, bit 5	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 2048 mV of input voltage.
2	Input Voltage, bit 4	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 1024 mV of input voltage.
1	Input Voltage, bit 3	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 512 mV of input voltage.
0	Input Voltage, bit 2	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 256 mV of input voltage.

表 9-49. InputVoltage Register (I²C address = 0Ah) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Input Voltage, bit 1	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 128 mV of input voltage.
6	Input Voltage, bit 0	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 64 mV of input voltage
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

9.6.22 IIN_HOST Register (I²C address = 0F/0Eh) [reset = 2000h]

To set the nominal or typical input current limit based on the adapter rated current. Write a 7-bit IIN_HOST register command using the data format listed below.

When using a 10-mΩ sense resistor (RSNS_RAC=0b), the charger provides a nominal input-current limit range of 50 mA to 6350 mA, with 50-mA resolution. The upper boundary is implemented through DAC clamp, writing value higher than limitation will be neglected. The lower boundary is implemented through 50-mA offset at code 0. Note this offset is only applied to code 0, not applied to other codes. The default nominal input current limit is 3.25 A. Upon adapter removal, the input current limit is reset to the default value of 3.25 A.

When using a 5-mΩ sense resistor (RSNS_RAC=1b) referring to セクション 9.3.5, the input-current limit range can be found under certain IADPT pin, EN_FAST_5MOHM bit status. The lower boundary is implemented through 100-mA offset at code 0. Note this offset is only applied to code 0, not applied to other codes. The default current limit is 3.2 A. Due to the USB current setting requirement, the register setting specifies the maximum current instead of the typical current. Upon adapter removal, the nominal input current limit is reset to the default value of 3.2 A.

To set the maximum input current limit based on adapter rated current. Additional 100-mA (10-mΩ sense resistor)/200-mA (5-mΩ sense resistor) offset should be added based on above nominal input current limit to obtain the maximum input current limit.

The ACP and ACN pins are used to sense R_{AC} with the default value of 5 mΩ. For a 10-mΩ sense resistor, a larger sense voltage is given and a better regulation accuracy, but at the cost of higher conduction loss.

Instead of using the internal IIN_DPM loop, the user can build up an external input current regulation loop and have the feedback signal on the ILIM_HIZ pin.

In order to disable ILIM_HIZ pin, the host can write EN_EXTILIM=0b to disable ILIM_HIZ pin, or pull ILIM_HIZ pin above 4.0 V.

図 9-37. IIN_HOST Register (I²C address = 0F/0Eh) [reset = 4100h]

7	6	5	4	3	2	1	0
Reserved	Input Current set by host, bit 6	Input Current set by host, bit 5	Input Current set by host, bit 4	Input Current set by host, bit 3	Input Current set by host, bit 2	Input Current set by host, bit 1	Input Current set by host, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-50. IIN_HOST Register With 5-mΩ Sense Resistor (I²C address = 0Fh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Input Current set by host, bit 6	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 6400 mA of input current.
5	Input Current set by host, bit 5	R/W	1b	0 = Adds 0 mA of input current. 1 = Adds 3200 mA of input current.
4	Input Current set by host, bit 4	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 1600 mA of input current.
3	Input Current set by host, bit 3	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 800 mA of input current.

表 9-50. IIN_HOST Register With 5-mΩ Sense Resistor (I²C address = 0Fh) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
2	Input Current set by host, bit 2	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 400 mA of input current.
1	Input Current set by host, bit 1	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 200 mA of input current.
0	Input Current set by host, bit 0	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 100 mA of input current.

表 9-51. IIN_HOST Register With 5-mΩ Sense Resistor (I²C address = 0Eh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R	00000000b	Not used. Value Ignored.

9.6.23 ID Registers

9.6.23.1 ManufactureID Register (I²C address = 2Eh) [reset = 40h]

図 9-38. ManufactureID Register (I²C address = 2Eh) [reset = 40h]

7-0
Manufacturer ID
R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-52. ManufactureID Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION (READ ONLY)
7-0	MANUFACTURE_ID	R	40h	40h

9.6.23.2 Device ID (DeviceAddress) Register (I²C address = 2Fh) [reset = D6h]

図 9-39. Device ID (DeviceAddress) Register (I²C address = 2Fh) [reset = D6h]

7-0
DEVICE_ID
R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-53. Device ID (DeviceAddress) Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	DEVICE_ID	R	BQ25731: 11 01 0110b (D6h)	BQ25731: 11 01 0110b (D6h)

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The BQ2573xEVM evaluation module (EVM) is a complete charger module for evaluating the BQ25731. The application curves were taken using the BQ2573xEVM.

As shown in 図 10-1, at the charger VSYS terminal, a minimum 7-µF effective MLCC capacitance (7 × 10-µF 0603 package MLCC) is suggested for a 45-W to 65-W adapter, and two more 10-µF MLCC capacitors are needed when power reaches 90 W. Overall 50-µF effective capacitance on VSYS net is necessary (POSCAP is preferred). These capacitors do not have to be placed at the charger VSYS output terminal; all capacitors connected to VSYS net can be counted including the input capacitor of the next stage converters.

10.2 Typical Application

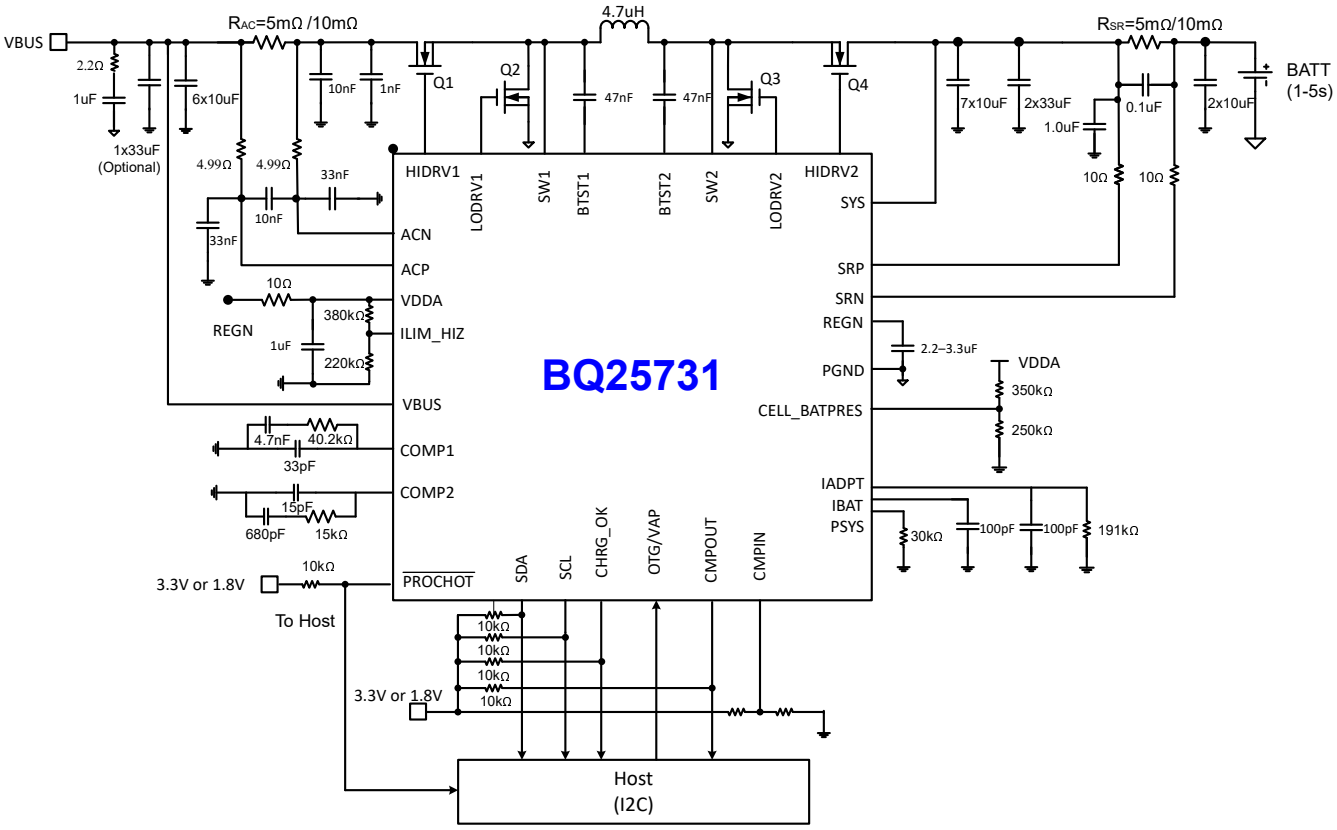


図 10-1. Application Diagram of BQ25731 with Non Power Path

10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage(2)	3.5 V < Adapter Voltage < 26V
Input Current Limit (2)	3.2 A for 65-W adapter
Battery Charge Voltage(1)	8400 mV for 2s battery

DESIGN PARAMETER	EXAMPLE VALUE
Battery Charge Current(1)	3072 mA for 2s battery
Minimum System Voltage(1)	6600 mV for 2s battery

(1) Refer to battery specification for settings.
(2) Refer to adapter specification for settings for Input Voltage and Input Current Limit.

10.2.2 Detailed Design Procedure

The parameters are configurable using the evaluation software. The simplified application circuit (see 図 10-1, as the application diagram) shows the minimum component requirements. Inductor, capacitor, and MOSFET selection are explained in the rest of this section. Refer to the EVM user's guide for the complete application schematic.

10.2.2.1 Input Snubber and Filter for Voltage Spike Damping

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at VBUS pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent overvoltage event on VBUS pin.

There are several methods to damp or limit the overvoltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the overvoltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the overvoltage level to an IC safe level. However these two solutions may not save cost or have small size.

A cost effective and small size solution is shown in 図 10-2. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result the over voltage spike is limited to a safe level. D1 is used for reverse voltage protection for VBUS pin. C2 is VBUS pin decoupling capacitor and it should be placed as close as possible to VBUS pin. C2 value should be less than C1 value so R1 can dominate the equivalent ESR value to get enough damping effect. R2 is used to limit inrush current of D1 to prevent D1 getting damage when adapter hot plug-in. R2 and C2 should have 10-µs time constant to limit the dv/dt on VBUS pin to reduce inrush current when adapter hot plug in. R1 has high inrush current. R1 package must be sized enough to handle inrush current power loss according to resistor manufacturer's data sheet. The filter components' value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

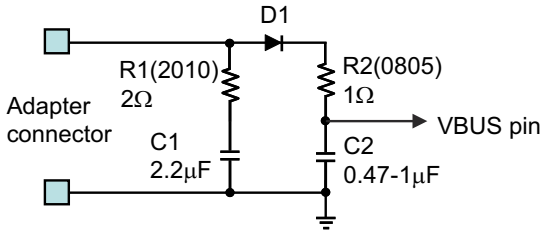


図 10-2. Input Filter

10.2.2.2 ACP-ACN Input Filter

The BQ25731 has average current mode control. The input current sensing through ACP/ACN is critical to recover inductor current ripple. Parasitic inductance on board will generate high frequency ringing on ACP-ACN which overwhelms converter sensed inductor current information. It is also difficult to manage parasitic inductance created based on different PCB layout. Larger parasitic inductance will generate larger sense current ringing which could cause the average current control loop to go into oscillation. Therefore ACP-ACN sensing information need to be conditioned.

For real system board condition, we suggest using below circuit design to get best result and filter noise induced from different PCB parasitic factor. With time constant of filter from 47 ns to 200 ns, the filter is effective and the delay of on the sensed signal is small, therefore there is no concern for average current mode control. If 400-kHz switching frequency is employed, 10 nF is recommended for C_{DIFF}; if 800-kHz switching frequency is chosen, then C_{DIFF} can be left open.

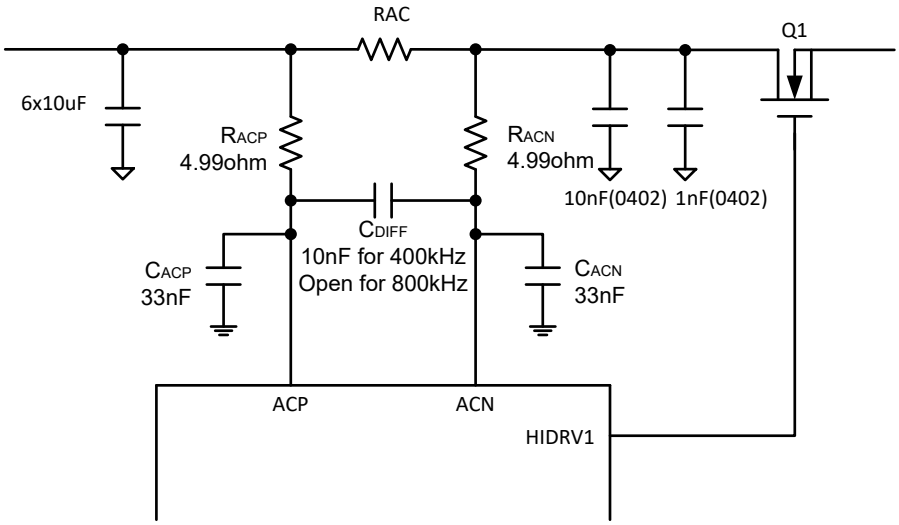


図 10-3. ACN-ACP Input Filter

10.2.2.3 Inductor Selection

The BQ25731 has two selectable fixed switching frequency. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (2)$$

The inductor ripple current in buck operation depends on input voltage (V_{IN}), duty cycle ($D_{BUCK} = V_{OUT}/V_{IN}$), switching frequency ($f_S$) and inductance (L):

$$I_{RIPPLE\_BUCK} = V_{IN} \times D_{BUCK} \times (1-D_{BUCK}) / (f_S \times L) \quad (3)$$

During boost operation, the duty cycle is:

$D_{BOOST} = 1 – (V_{IN}/V_{BAT})$

and the ripple current is:

$I_{RIPPLE\_BOOST} = (V_{IN} \times D_{BOOST}) / (f_S \times L)$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9 V to 12.6 V for 3-cell battery pack. For 20-V adapter voltage, 10-V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12 V to 16.8 V, and 12-V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

10.2.2.4 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current (plus system current there is any system load) when duty cycle is 0.5 in buck mode. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by 式 4:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (4)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed in front of R_{AC} current sensing and as close as possible to the power stage half bridge MOSFETs. Capacitance after R_{AC} before power stage half bridge should be limited to 10 nF + 1 nF referring to 図 10-3 diagram. Because too large capacitance after R_{AC} could filter out R_{AC} current sensing ripple information. Voltage rating of the capacitor must be higher than normal input voltage level, 25-V rating or higher capacitor is preferred for 19-V to 20-V input voltage.

Ceramic capacitors (MLCC) show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the derating performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required effective capacitance value at the operating point.

10.2.2.5 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 10 kHz and 20 kHz. The preferred ceramic capacitor is 25-V X7R or X5R for output capacitor. Minimum 7 pcs of 10-µF 0603 package capacitor is suggested to be placed as close as possible to Q3&Q4 half bridge (between Q4 drain and Q3 source terminal). Total minimum output effective capacitance along VSYS distribution line is 50 µF refers to 表 10-1. Recommend to place minimum 20-µF MLCC capacitors after the charge current sense resistor for best stability.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the derating performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required capacitance value at the operating point. Considering the 25-V 0603 package MLCC capacitance derating under 21-V to 23-V output voltage, the recommended practical capacitors configuration at VSYS output terminal can also be found in 表 10-1. Tantalum capacitors (POSCAP) can avoid dc-bias effect and temperature variation effect which are recommend to be used along VSYS output distribution line to meet total minimum effective output capacitance requirement.

表 10-1. Minimum Output Capacitance Requirement

OUTPUT CAPACITORS vs TOTAL INPUT POWER	65 W	90 W	130 W
Minimum Effective Output Capacitance	50 µF	50 µF	50 µF
Minimum output capacitors at charger VSYS output terminal	7*10 µF (0603 25 V MLCC)	9*10 µF (0603 25 V MLCC)	9*10 µF (0603 25 V MLCC)
Additional output capacitors along VSYS distribution line	2*22 µF (25 V~35 V POSCAP)	2*22 µF (25 V~35 V POSCAP)	2*22 µF (25 V~35 V POSCAP)

10.2.2.6 Power MOSFETs Selection

Four external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are integrated into the IC with 6 V of gate drive voltage. 30 V or higher voltage rating MOSFETs are preferred for 19-V to 20-V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \cdot Q_{GD}; \; FOM_{bottom} = R_{DS(on)} \cdot Q_G \quad (5)$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. Taking buck mode operation as an example the power loss is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ($R_{DS(ON)\_top}$), input voltage (V_{IN}), switching frequency (f_S), turn-on time (t_{on}) and turn-off time (t_{off}):

$$P_{top} = P_{con\_top} + P_{sw\_top} \quad (6)$$

$$P_{con\_top} = D \cdot I_{L\_RMS}^{2} \cdot R_{DS(on)\_top}; \quad (7)$$

$$I_{L\_RMS}^{2} = I_{L\_DC}^{2} + I_{ripple}^{2}/12 \quad (8)$$

- I_{L_DC} is the average inductor DC current under buck mode;
- I_{ripple} is the inductor current ripple peak-to-peak value;

$$P_{sw\_top} = P_{IV\_top} + P_{Qoss\_top} + P_{Gate\_top}; \quad (9)$$

The first item P_{con_top} represents the conduction loss which is straight forward. The second term P_{sw_top} represents the multiple switching loss items in top MOSFET including voltage and current overlap losses (P_{IV_top}), MOSFET parasitic output capacitance loss (P_{Qoss_top}) and gate drive loss (P_{Gate_top}). To calculate voltage and current overlap losses (P_{IV_top}):

$$P_{IV\_top} = 0.5x\, V_{IN} \cdot I_{valley} \cdot t_{on} \cdot f_S + 0.5x\, V_{IN} \cdot I_{peak} \cdot t_{off} \cdot f_S \quad (10)$$

$$I_{valley} = I_{L\_DC} - 0.5 \cdot I_{ripple} \text{ (inductor current valley value)}; \quad (11)$$

$$I_{peak} = I_{L\_DC} + 0.5 \cdot I_{ripple} \text{ (inductor current peak value)}; \quad (12)$$

- t_{on} is the MOSFET turn-on time that V_{DS} falling time from V_{IN} to almost zero (MOSFET turn on conduction voltage);
- t_{off} is the MOSFET turn-off time that I_{DS} falling time from I_{peak} to zero;

The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}} \quad (13)$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current, and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{sw} = Q_{GD} + Q_{GS} \quad (14)$$

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}), and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \quad (15)$$

To calculate top MOSFET parasitic output capacitance loss (P_{Qoss_top}):

$$P_{Qoss\_top} = 0.5 \cdot V_{IN} \cdot Q_{oss} \cdot f_S \quad (16)$$

- Q_{oss} is the MOSFET parasitic output charge which can be found in MOSFET datasheet;

To calculate top MOSFET gate drive loss (P_{Gate_top}):

$$P_{Gate\_top} = V_{IN} \cdot Q_{Gate\_top} \cdot f_S \quad (17)$$

- Q_{Gate_top} is the top MOSFET gate charge which can be found in MOSFET datasheet;
- Note here V_{IN} is used instead of real gate drive voltage 6 V because, the gate drive 6 V is generated based on LDO from V_{IN} under buck mode, the total gate drive related loss are all considered when V_{IN} is used for gate drive loss calculation .

The bottom-side MOSFET loss also includes conduction loss and switching loss:

$$P_{bottom} = P_{con\_bottom} + P_{sw\_bottom} \quad (18)$$

$$P_{con\_bottom} = (1 - D) \cdot I_{L\_RMS}^{2} \cdot R_{DS(on)\_bottom}; \quad (19)$$

$$P_{sw\_bottom} = P_{RR\_bottom} + P_{Dead\_bottom} + P_{Gate\_bottom}; \quad (20)$$

The first item P_{con_bottom} represents the conduction loss which is straight forward. The second term P_{sw_bottom} represents the multiple switching loss items in bottom MOSFET including reverse recovery losses (P_{RR_bottom}), Dead time body diode conduction loss (P_{Dead_bottom}) and gate drive loss (P_{Gate_bottom}). The detail calculation can be found below:

$$P_{RR\_bottom} = V_{IN} \cdot Q_{rr} \cdot f_S \quad (21)$$

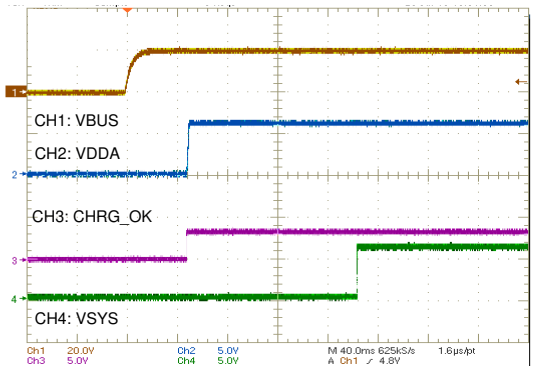
- Q_{rr} is the bottom MOSFET reverse recovery charge which can be found in MOSFET data sheet;

$$P_{Dead\_bottom} = V_F \cdot I_{valley} \cdot f_S \cdot t_{dead\_rise} + V_F \cdot I_{peak} \cdot f_S \cdot t_{dead\_fall} \quad (22)$$

- V_F is the body diode forward conduction voltage drop;
- t_{dead_rise} is the SW rising edge deadtime between top and bottom MOSFETs which is around 40 ns;
- t_{dead_fall} is the SW falling edge deadtime between top and bottom MOSFETs which is around 30 ns;

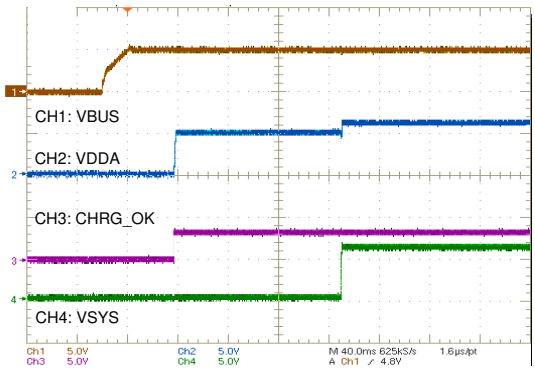
P_{Gate_bottom} can follow the same method as top MOSFET gate drive loss calculation approach refer to 式 17.

10.2.3 Application Curves



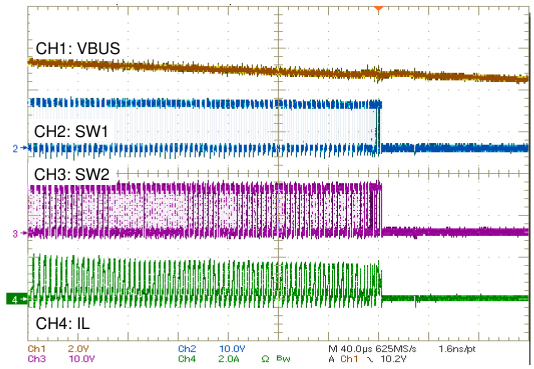
2-cell without battery

図 10-4. Power Up From 20 V



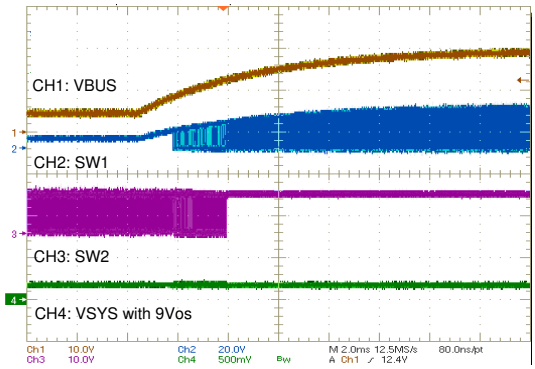
2-cell without battery

図 10-5. Power Up From 5 V



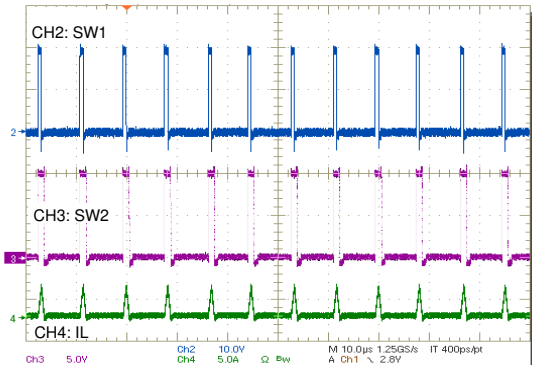
3-cell VBAT = 10 V

図 10-6. Power Off From 12 V



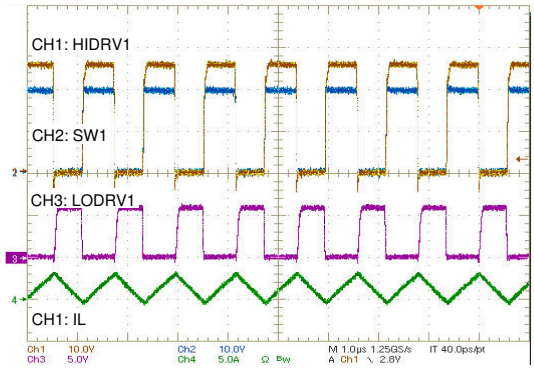
VBUS 5 V to 20 V

図 10-7. Line Regulation



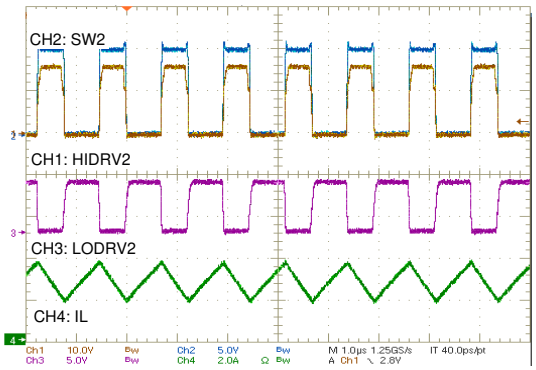
VBUS = 20 V, VSYS = 10 V, ISYS = 200 mA

図 10-8. PFM Operation



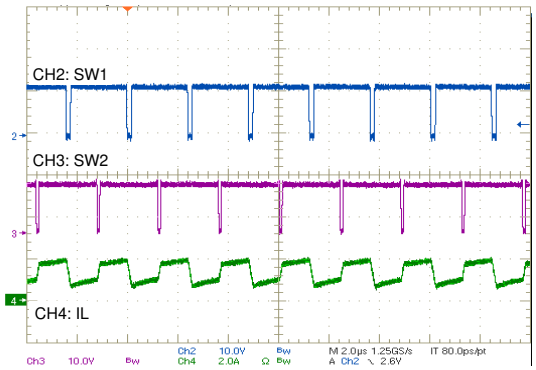
VBUS = 20 V, VSYS = 10 V, ISYS = 2 A

図 10-9. PWM Operation



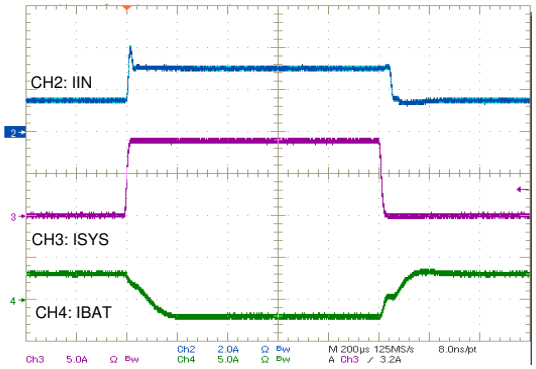
VBUS = 5 V, VBAT = 10 V

図 10-10. Switching During Boost Mode



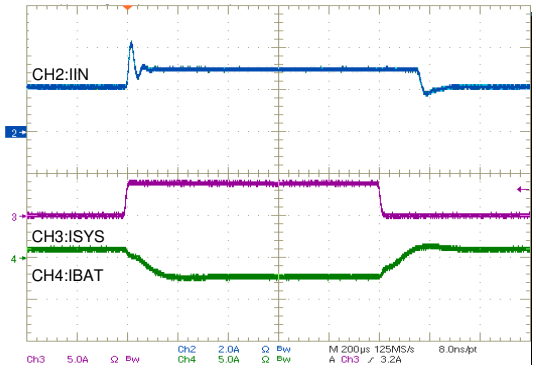
VBUS = 12 V, VBAT = 12 V

図 10-11. Switching During Buck Boost Mode



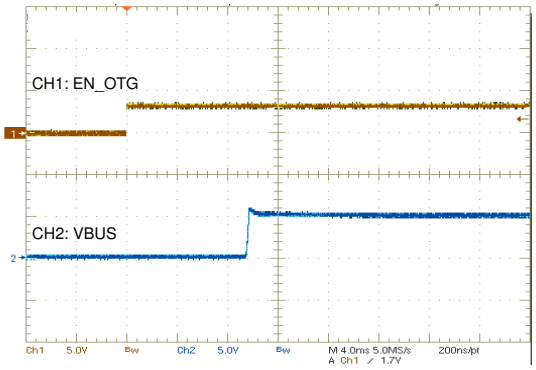
VBUS = 20 V/3.25 A, VBAT = 7.5 V

図 10-12. Input Current Regulation in Buck Mode



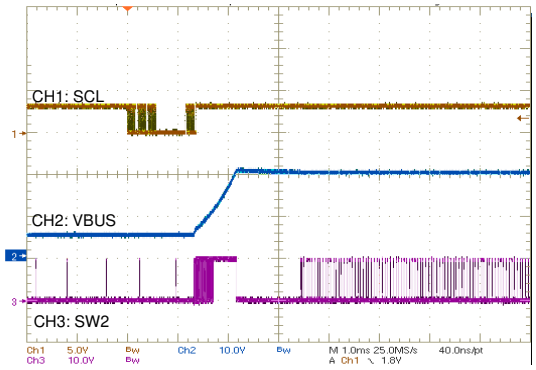
VBUS = 5 V/3.25 A, VBAT = 7.5 V

図 10-13. Input Current in Boost Mode



VBUS = 5 V

図 10-14. OTG Power Up from 8-V Battery



VBAT = 10 V, VBUS 5 V to 20 V, IOTG = 500 mA

図 10-15. OTG Voltage Ramp Up

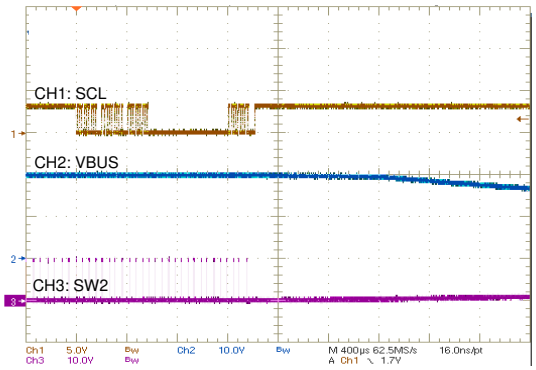
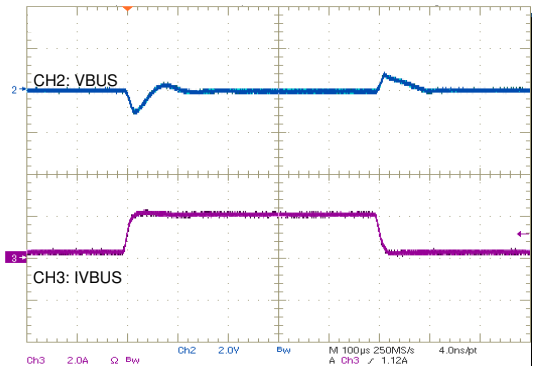
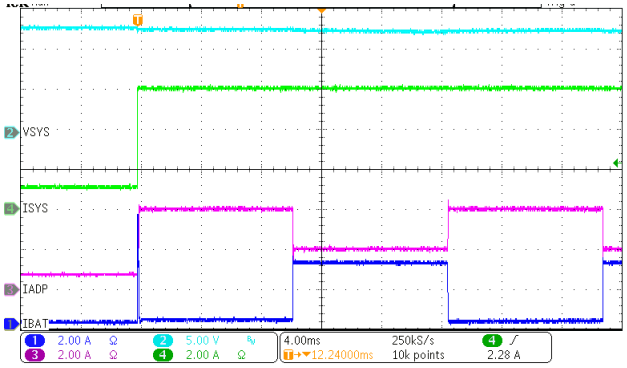


図 10-16. OTG Power Off



VBAT = 10 V, VBUS = 20 V

図 10-17. OTG Load Transient



VBUS = 20 V
T_{MAX} = 20 ms
ISYS = 1 to 6 A

IIN_DPM = 2 A
T_{OVLD} = 10 ms
ICHG = 0 A

ILIM2_VTH = 200%
VBAT = 12.8 V

図 10-18. Peak Power Mode IBUS Trigger

11 Power Supply Recommendations

The valid adapter range is from 3.5 V (V_{VBUS_CONVEN}) to 26 V with at least 500-mA current rating. When CHRG_OK goes HIGH, the system is powered from adapter through the charger. When adapter is removed, the system is connected to battery.

12 Layout

12.1 Layout Guidelines

Proper layout of the components to minimize high frequency current path loop (see セクション 12.2) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout.

表 12-1. PCB Layout Guidelines

RULES	COMPONENTS	FUNCTION	IMPACT	GUIDELINES
1		PCB layer stack up	Thermal, efficiency, signal integrity	Multi- layer PCB is suggested. Allocate at least one ground layer. The BQ257XXEVM uses a 4-layer PCB (top layer, ground layer, signal layer and bottom layer).
2	CBUS, RAC, Q1, Q2	Input loop	High frequency noise, ripple	VBUS capacitors, RAC, Q1 and Q2 form a small loop 1. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CBUS to the other side of PCB for high density design. After RAC before Q1 and Q2 power stage recommend to put 10 nF + 1 nF (0402 package) decoupling capacitors as close as possible to IC to decoupling switching loop high frequency noise.
3	R_{AC}, Q1, L1, Q4	Current path	Efficiency	The current path from VBUS to VSYS, through R_{AC}, Q1, L1, Q4, has low impedance. Pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1 to 2A/via for a 10-mil via with 1 oz. copper thickness.
4	CSYS, Q3, Q4	Output loop	High frequency noise, ripple	VSYS capacitors, Q3 and Q4 form a small loop 2. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CSYS to the other side of PCB for high density design.
5	R_{SR}	Current path	Efficiency, battery voltage detection	Place R_{SR} near the battery terminal. The current path from VBAT to VSYS, through R_{SR}, has low impedance. Pay attention to via resistance if they are not on the same side. The device detects the battery voltage through SRN near battery terminal.
6	Q1, Q2, L1, Q3, Q4	Power stage	Thermal, efficiency	Place Q1, Q2, L1, Q3 and Q4 next to each other. Allow enough copper area for thermal dissipation. The copper area is suggested to be 2x to 4x of the pad size. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat.
7	R_{AC}, R_{SR}	Current sense	Regulation accuracy	Use Kelvin-sensing technique for R_{AC} and R_{SR} current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs.
8	Small capacitors	IC bypass caps	Noise, jittering, ripple	Place VBUS cap, VCC cap, REGN caps near IC.
9	BST capacitors	HS gate drive	High frequency noise, ripple	Place HS MOSFET boost strap circuit capacitor close to IC and on the same side of PCB board. Capacitors SW1/2 nodes are recommended to use wide copper polygon to connect to power stage and capacitors BST1/2 node are recommended to use at least 8mil trace to connected to IC BST1/2 pins.

表 12-1. PCB Layout Guidelines (continued)

RULES	COMPONENTS	FUNCTION	IMPACT	GUIDELINES
10		Ground partition	Measurement accuracy, regulation accuracy, jitters, ripple	Separate analog ground(AGND) and power grounds(PGND) is preferred. PGND should be used for all power stage related ground net. AGND should be used for all sensing, compensation and control network ground for example ACP/ACN/COMP1/ COMP2/CMPIN/CMPOUT/IADPT/IBAT/PSYS. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. If possible, use dedicated COMP1, COMP2 AGND traces. Connect analog ground and power ground together using power pad as the single ground connection point.

12.2 Layout Example

12.2.1 Layout Example Reference Top View

Based on the above layout guidelines, the buck-boost charger layout example top view is shown below including all the key power components.

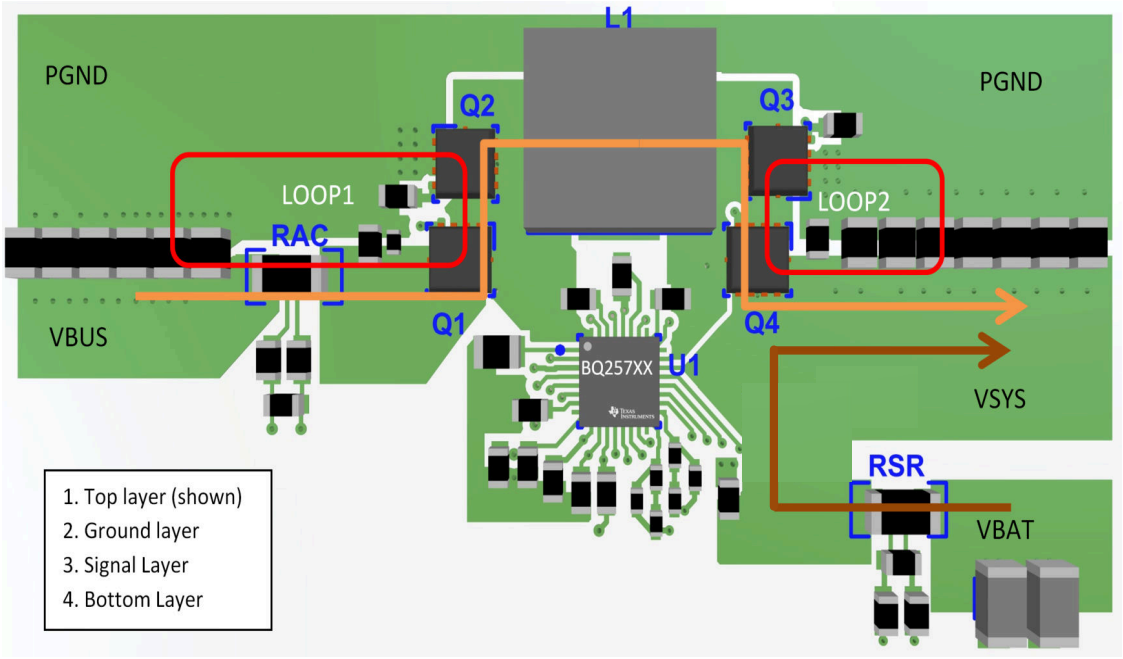


図 12-1. Buck-Boost Charger Layout Reference Example Top View

12.2.2 Inner Layer Layout and Routing Example

For both input sensing resistor and charging current sensing resistor, differential sensing and routing method are suggested and highlighted in below figure. Use wide trace for gate drive traces, minimum 15 mil trace width. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. Suggest using dedicated COMP1, COMP2 analog ground traces shown in below figure.

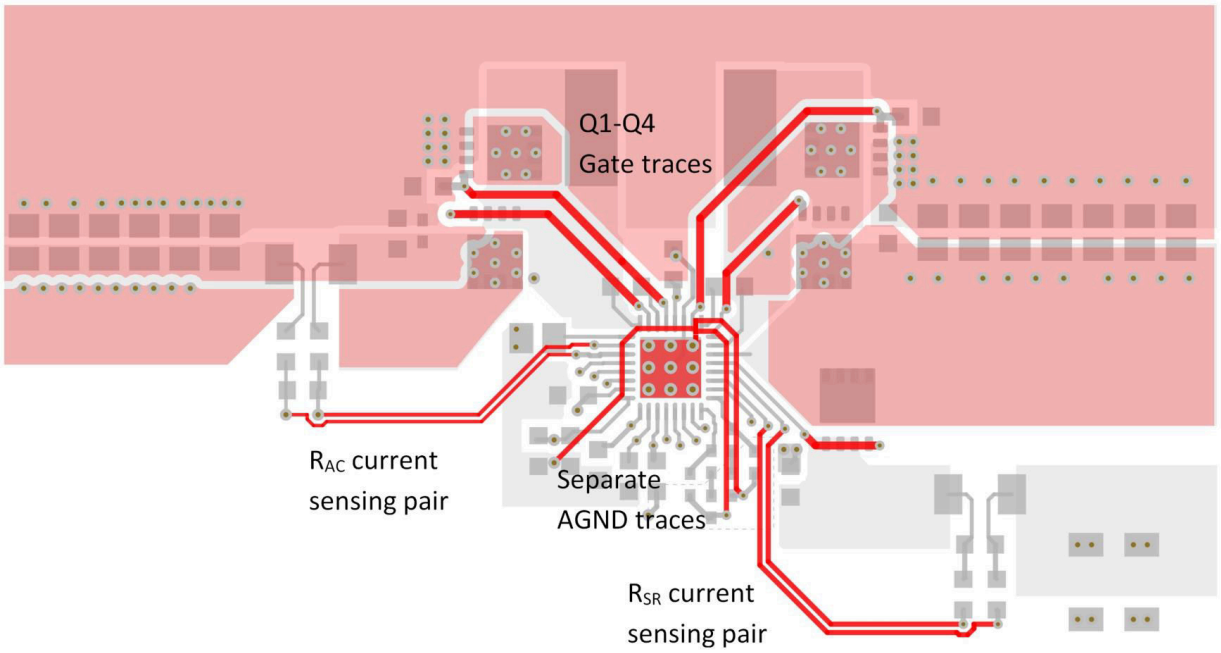


図 12-2. Buck-Boost Charger Gate Drive/Current Sensing/AGND Signal Layer Routing Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics Application Report*
- *BQ2571x Evaluation Module User's Guide*
- *QFN/SON PCB Attachment Application Report*

13.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

13.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25731RSNR	ACTIVE	QFN	RSN	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25731	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

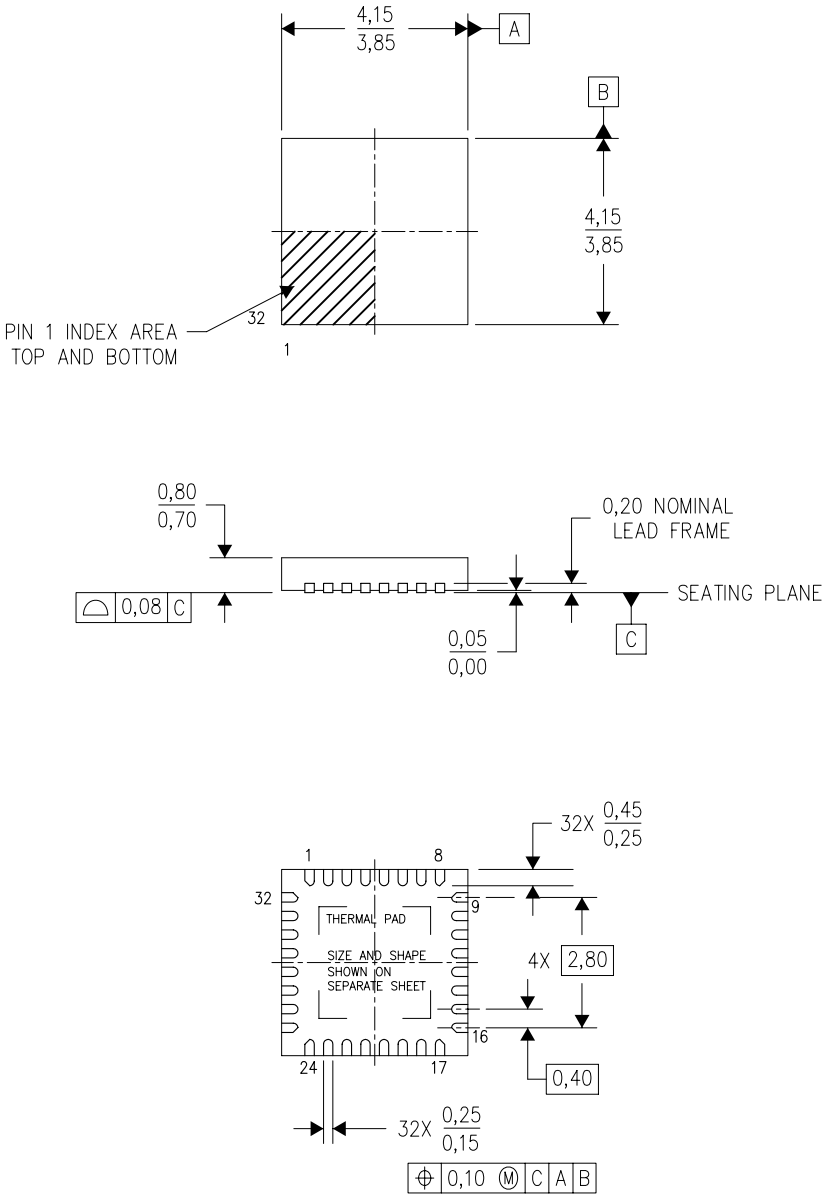
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207561/C 08/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

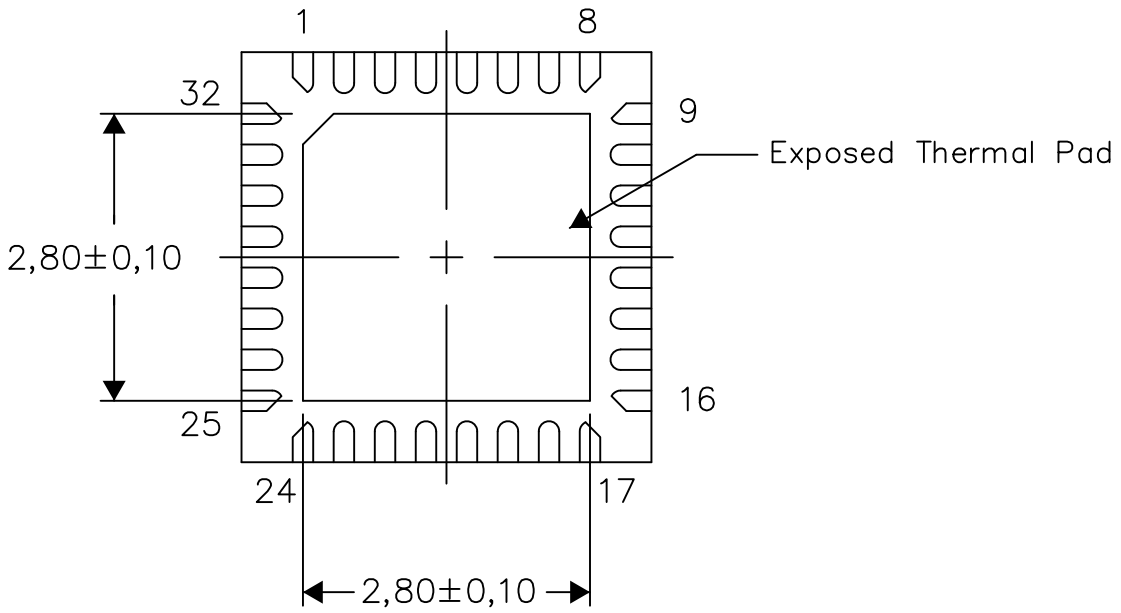
RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



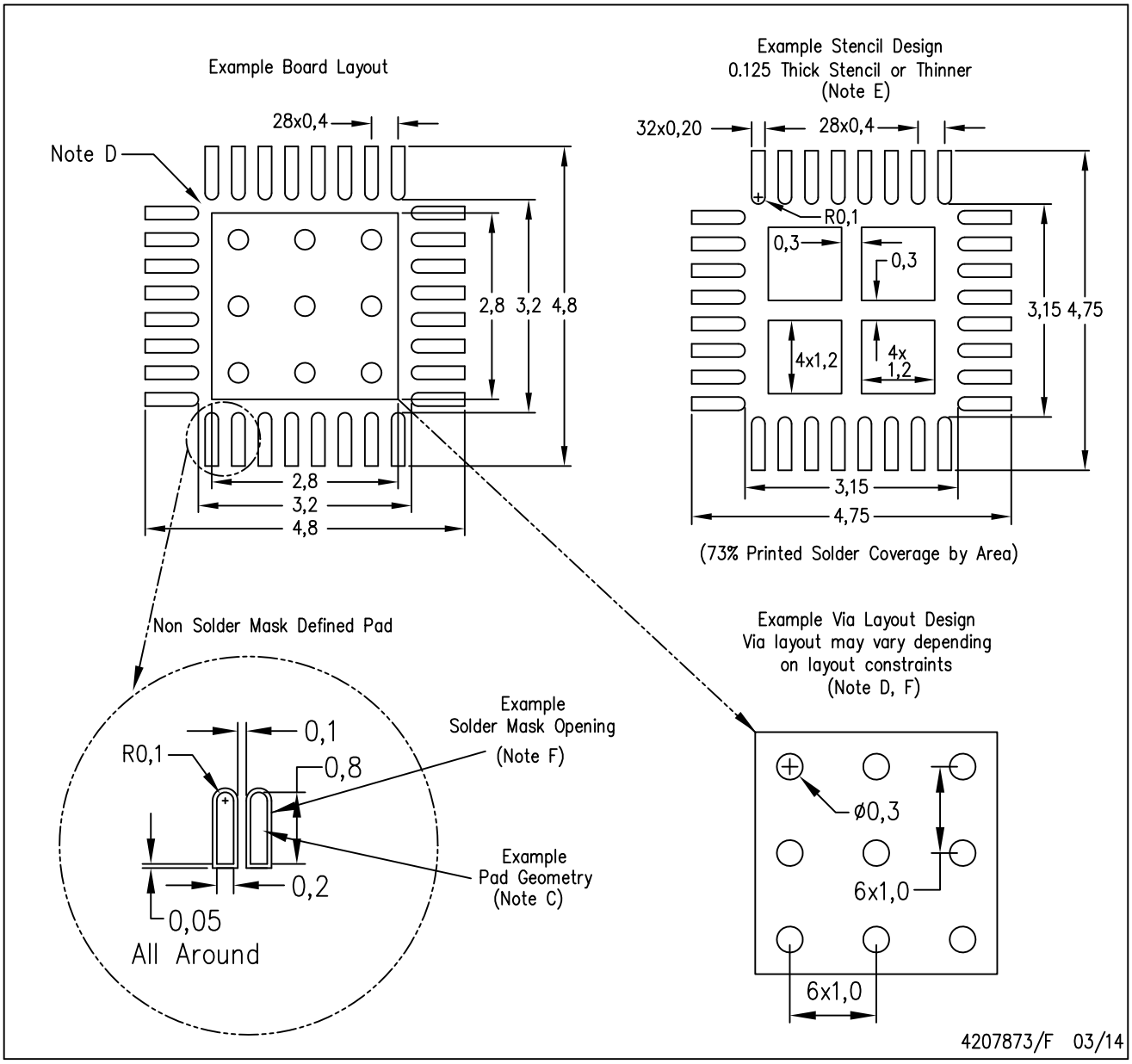
Bottom View

Exposed Thermal Pad Dimensions

4209775–2/F 03/14

NOTE: All linear dimensions are in millimeters

RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265