TEXAS INSTRUMENTS
BQ25638
JAJSSD2A – OCTOBER 2023 – REVISED DECEMBER 2023

BQ25638 I²C 制御、5A、最大 18V 入力、NVDC 電力パス管理機能および USB OTG 昇圧出力付きチャージャ

1 特長

- シングル・セル・バッテリ向けの高効率 5A、1.5MHz、同期スイッチング・モード降圧充電器
  - 5V 入力から 90% を上回る効率で 10mA の出力電流を供給
  - 80mA 刻みの最大 5A の充電電流
  - 10mA 刻みの 30～1000mA の充電終端
  - フレキシブルな JEITA プロファイルにより温度範囲全体にわたって安全に充電
- BATFET 制御によりシャットダウン、、完全システム・リセットをサポート
  - バッテリのみモードで 1.5μA の静止電流
  - 超低消費電力モードで 1.3μA のバッテリ リーク電流
  - シャットダウンで 100μA のバッテリ・リーク電流
- USB On-The-Go (OTG) をサポート
  - 3.84V～9.6V の出力を備えた昇圧モード動作
  - プログラマブル制限機能：最大 3.2A
- 幅広い入力電源をサポート
  - 3.9V～18V の広い入力動作電圧範囲と 26V の絶対最大入力電圧
  - バッテリ電圧を自動的に追従する VINDPM スレッショルド
  - 入力電流オプティマイザ (ICO) により、アダプタの過負荷を引き起こさずに入力電力を最大化
- 7mΩ の BATFET による高効率のバッテリ動作
- Narrow VDC (NVDC) 電力パス管理
  - 消耗したバッテリまたはバッテリ未接続でもシステムを即時オン
  - アダプタが全負荷になったときのバッテリ補完
- フレキシブルな自律または I²C 制御モード
- 電圧、電流、温度を監視するための 12 ビット ADC を内蔵
  - 最大 1V の外部信号に対応する ADCIN ピン
- 高精度
  - ±0.5% の充電電圧レギュレーション
  - ±5% の充電電流レギュレーション
  - ±5% の入力電流レギュレーション
- 安全
  - バッテリ温度センシング
  - サーマル・レギュレーションおよびサーマル・シャットダウン
  - バッテリ / コンバータの過電流保護
  - 充電安全タイマ

2 アプリケーション

- ゲームおよびコンピュータ用アクセサリ
- スマートフォン、タブレット
- IP カメラ、EPOS
- 携帯医療機器
- 民生用のウェアラブルおよびスマートウォッチ
- ポータブル スピーカ、TWS イヤホン

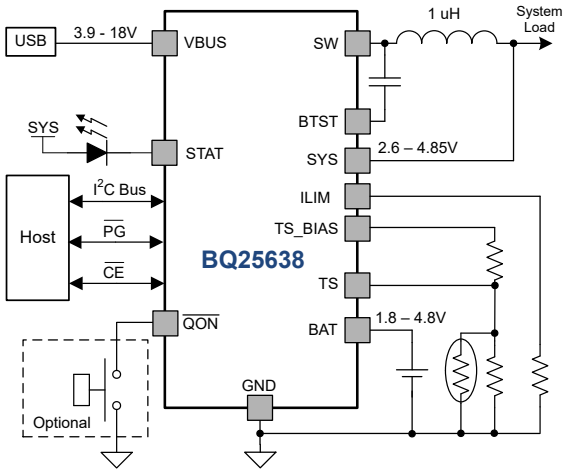
3 概要

BQ25638 は、シングル セル リチウムイオン / リチウムポリマ バッテリ用の高度に統合された 5A スイッチモード バッテリ充電管理およびシステム電力パス管理デバイスです。このソリューションは、内蔵電流検出、ループ補償、入力逆電流ブロック FET (RBFET、Q1)、ハイサイド・スイッチング FET (HSFET、Q2)、ローサイド・スイッチング FET (LSFET、Q3)、およびシステムとバッテリの間にあるバッテリ FET (BATFET、Q4) を高度に統合しています。システム電圧が設定可能な最小値を下回らないように、本デバイスは NVDC 電力パス管理機能を使用してシステム電圧をバッテリ電圧よりわずかに高い値にレギュレートします。低インピーダンスの電力パスはスイッチモード動作効率を最適化し、バッテリ充電時間を短縮し、放電フェーズ中のバッテリ寿命を延長し、。充電およびシステムの設定に I²C シリアル インターフェイスを使用できるため、BQ25638 は真に柔軟なソリューションとなります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
BQ25638	YBG (DSBGA 30)	2.0 mm × 2.4 mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値で、該当する場合はピンも含まれます。



BQ25638 のアプリケーション概略図

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4 概要 (続き)

このデバイスは、標準の USB ホスト・ポート、USB 充電ポート、USB 対応高電圧アダプタなど、幅広い入力ソースをサポートしています。このデバイスは、入力電流および電圧のレギュレーションにより、USB 2.0 および USB 3.0 の電力仕様に準拠しています。さらに、入力電流オプティマイザ (ICO) は、入力ソースの過負荷なしで最大電力点の検出をサポートします。BQ25638 は、デフォルトの入力電流制限値を設定するための ILIM ピンと、サーミスタのバイアスを制御するための TS_BIAS ピンを備えています。また、このデバイスは最大 3.2 A までの定電流制限による USB On-the-Go (OTG) の動作電力定格仕様にも合致しています。

電力パス管理により、システムはバッテリ電圧より少し高くなるように、かつプログラム可能な最低システム電圧より低くならないようにレギュレートされます。この機能により、システムはバッテリが完全に消耗したとき、または取り外したときでも、動作を継続できます。入力の電流または電圧が制限値に達すると、電力パス管理機能が自動的に充電電流を低下させます。システム負荷が引き続き増大すると、電力パスはシステムの電力要件が満たされるまで、バッテリを放電します。この補助モードにより入力ソースの過負荷を防止します。

このデバイスは、ホスト制御なしで、充電サイクルの開始から完了までを実行できます。バッテリ電圧を検知することで、本デバイスは 4 種類の段階 (トリクル充電、予備充電、定電流 (CC) 充電、定電圧 (CV) 充電) でバッテリを充電します。充電サイクルの終わりに、充電電流があらかじめ設定されたスレッショルドを下回り、かつバッテリ電圧が再充電スレッショルドを上回ると、充電器は自動的に処理を終了します。TS ピンの COOL、PRECOOL、NORMAL、WARM および PREWARM 温度ゾーンでは、終端がサポートされています。十分に充電された電圧がプログラム可能な再充電スレッショルドを下回ると、充電器は自動的に新しい充電サイクルを開始します。

この充電器は、バッテリの負温度係数 (NTC) サーミスタ監視、充電安全タイマ、過電圧および過電流保護など、バッテリ充電とシステム運用のための多様な安全機能を備えています。接合部温度がプログラム可能なスレッショルド値を超えると、サーマル・レギュレーションにより充電電流が低下します。STAT 出力は、充電状態と任意のフォルト状態を通知します。その他の安全機能としては、充電モードと OTG 昇圧モードでのバッテリ温度センシング、サーマル・シャットダウン、入力 UVLO および過電圧保護を装備しています。$\overline{PG}$ 出力は、良好な電源が存在し、プログラム可能な PG_TH 値を上回っているかどうかを示します。 $\overline{INT}$ 出力は、フォルトの発生とステータスの変化を即座にホストに通知します。

このデバイスには、充電電流と入力 / バッテリ / システム (VBUS、BAT、SYS、TS) 電圧を監視するための、12 ビットのアナログ / デジタル・コンバータ (ADC) も搭載されています。さらに、ADCIN ピンを使用して最大 1V の外部信号を監視できます。 $\overline{QON}$ ピンは BATFET イネーブルおよびリセット制御を実現し、超低消費電力モードを終了したり、またはシステムの完全なリセットを開始したりします。

BQ25638 は 30 ピン、2.0 mm × 2.4 mm の DSBGA パッケージで供給されます。

5 Pin Configuration and Functions

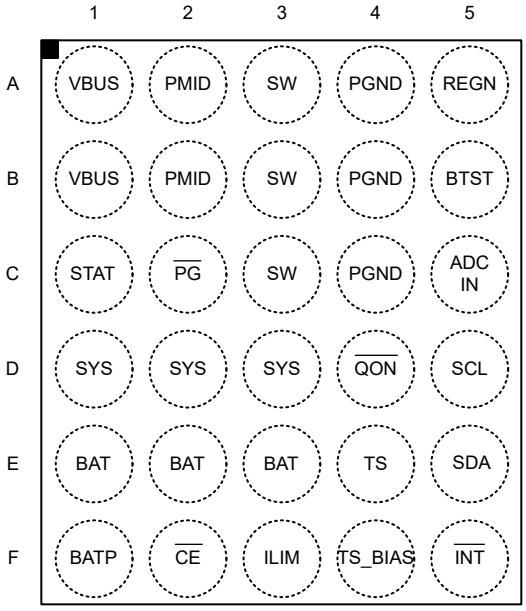


図 5-1. BQ25638 Pinout, 30-Ball YBG DSBGA Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ADCIN	C5	AI	**External ADC Input –** Connect an external analog signal up-to 1-V to monitor.
BAT	E1	P	**Positive Terminal of Battery Pack Connection –** The internal BATFET is connected between SYS and BAT. Connect a 10 µF ceramic capacitor closely to the BAT pin and GND.
	E2		
	E3		
BATP	F1	AI	**Positive Battery Voltage Sense –** Kelvin connect to positive battery terminal. Place 100 Ω series resistance between this pin and the battery positive terminal.
BTST	B5	P	**PWM High-side Driver Supply –** Internally, BTST is connected to the cathode of the boot-strap diode. Connect a 0.047 µF bootstrap capacitor from SW to BTST.
$\overline{CE}$	F2	DI	**Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and CE pin is LOW. CE pin must be pulled HIGH or LOW, do not leave floating.
TS_BIAS	F4	AO	**Bias for the TS Resistor Voltage Divider–** Provides the bias voltage for the TS resistor voltage divider.
ILIM	F3	AI	**Input Current Limit Setting Pin –** ILIM pin sets the input current limit as IINREG = KILIM / RILIM, where RILIM is connected from ILIM pin to GND. The input current is limited to the lower of the two values set by ILIM pin and IINDPM register bits. The ILIM pin can also be used to monitor input current. The input current is proportional to the voltage on ILIM pin and can be calculated by IIN = (KILIM x VILIM) / (RILIM x 0.8 V). The ILIM pin function is disabled when EN_EXTILIM bit is set to 0.
$\overline{INT}$	F5	DO	**Open Drain Active Low Interrupt Output –** Connect /INT to the logic rail via a 10-kΩ resistor. The INT pin sends active low, 256-µs pulse to the host to report charger device status and fault.
$\overline{PG}$	C2	DO	**Open Drain Active Low Power Good Indicator –** Connect to the pull up rail via a 2.2-kΩ resistor. LOW indicates a valid input source above PG_TH.
PGND	A4	P	**Ground Return**
	B4		
	C4		
PMID	A2	P	**Blocking MOSFET Connection –** Given the total input capacitance, place 1 µF on VBUS, and the rest on PMID, as close to the IC as possible. Typical value: 10 µF in parallel with 0.1 µF ceramic capacitor.
	B2		

表 5-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
$\overline{QON}$	D4	DI	**BATFET Enable or System Power Reset Control Input –** If the charger is in ultra-low power mode, a logic low on this pin with t_{SM_EXIT} duration forces the device to exit the mode. If the charger is not in ultra-low power mode, a logic low on this pin with t_{QON_RST} initiates a full system power reset if either $V_{VBUS} < V_{VBUS\_UVLO}$ or BATFET_CTRL_WVBUS = 1. $\overline{QON}$ has no effect during shutdown mode. The pin contains an internal pull-up to maintain default high logic.
REGN	A5	P	**Internal Linear Regulator Output –** Internally, REGN is connected to the anode of the boot-strap diode. Connect a 10V or higher rating 4.7 µF ceramic capacitor from REGN to power ground. The capacitor should be close to the IC. The REGN LDO output is used for the internal MOSFETs gate driving voltage and for biasing the external TS pin thermistor in BQ25639.
SCL	D5	DI	**I²C Interface Clock –** Connect SCL to the logic rail through a 10 kΩ resistor.
SDA	E5	DIO	**I²C Interface Data –** Connect SDA to the logic rail through a 10 kΩ resistor.
STAT	C1	DO	**Open Drain Charge Status Output –** Indicates various charger operations. Connect to the pull up rail via a 2.2kΩ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. Setting DIS_STAT = 1 will disable the STAT pin function, causing the pin to be pulled high. Leave floating if unused.
SW	A3	P	**Switching Node Connecting to Output Inductor –** Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 47 nF bootstrap capacitor from SW to BTST.
	B3		
	C3		
SYS	D1	P	**Charger Output Voltage to System –** Buck converter output connection point to the system. The internal BATFET is connected between SYS and BAT. Connect 20µF close to the SYS pin.
	D2		
	D3		
TS	E4	AI	**Temperature Qualification Voltage Input –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from TS pin bias reference to TS, then to GND. Charge suspends when TS pin voltage is out of range. Recommend a 103AT-2 10kΩ thermistor.
VBUS	A1	P	**Charger Input Voltage –** The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1 uF ceramic capacitor from VBUS to GND as close as possible to IC.
	B1		

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VBUS (converter not switching)	–2	26	V
	PMID (converter not switching)	–0.3	26	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SW	–2 (50ns)	21	V
	ADCIN, BATP, $\overline{CE}$, ILIM, $\overline{INT}$, $\overline{PG}$, $\overline{QON}$, REGN, SCL, SDA, STAT, TS, TS_BIAS	–0.3	6	V
Differential Voltage	BTST-SW	–0.3	6	V
	PMID-VBUS	–0.3	6	V
	SYS-BAT	–0.3	6	V
Output Sink Current	$\overline{INT}$, STAT, $\overline{PG}$		6	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	3.9		18	V
V_{BAT}	Battery voltage			4.8	V
I_{VBUS}	Input current			3.2	A
I_{SW}	Output current (SW)			5.0	A
I_{BAT}	Fast charging current			5.0	A
	RMS discharge current (continuously)			7	A
	Peak discharge current (up to 50ms)			9	A
I_{REGN}	Maximum REGN Current, V_{VBUS} ≤ 18 V			20	mA
I_{REGN}	Maximum REGN Current, 18 V ≤ V_{VBUS} ≤ 28 V			8.5	mA
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C
L_{SW}	Inductor for the switching regulator	0.68		2.2	µH
C_{VBUS}	VBUS capacitor (without de-rating)	1			µF
C_{PMID}	PMID capacitor (without de-rating)	10			µF
C_{SYS}	SYS capacitor (without de-rating)	20			µF

6.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C_{BAT}	BAT capacitor (without de-rating)	10			µF
C_{SYS}	Effective SYS capacitance with NVM_EN_MIN_CSYS=1 (after voltage de-rating)	1.5			µF

6.4 Thermal Information

THERMAL METRIC(1)		BQ25638 YBG (DSBGA) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Quiescent battery current (BAT, SYS, SW) when the charger is in the battery only mode, BATFET is enabled, ADC is disabled	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, system is powered by battery. -40 °C < T_J < 60 °C		1.5	3	µA
$I_{Q\_BAT\_ADC}$	Quiescent battery current (BAT, SYS, SW) when the charger is in the battery only mode, BATFET is enabled, ADC is enabled	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC enabled, system is powered by battery. -40 °C < T_J < 60 °C		260		µA
$I_{Q\_BAT\_SD}$	Quiescent battery current (BAT) when the charger is in shutdown mode, BATFET is disabled, ADC is disabled	VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in shutdown mode, ADC disabled, T_J < 60 °C		100	200	nA
$I_{Q\_BAT\_ULPM}$	Quiescent battery current (BAT) when the charger is in ultra low power mode, BATFET is disabled, ADC is disabled	VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in ultra low power mode, ADC disabled, T_J < 60 °C		1.3		µA
I_{Q_VBUS}	Quiescent input current (VBUS)	VBUS = 5V, VBAT = 4V, charge disabled, converter switching, ISYS = 0A, PFM enabled		450		µA
I_{SD_VBUS}	Quiescent input current (VBUS) in HIZ	VBUS = 5V, VBAT = 4V, HIZ mode, ADC disabled		5	20	µA
		VBUS = 15V, VBAT = 4V, HIZ mode, ADC disabled		20	35	µA
I_{Q_OTG}	Quiescent battery current (BAT, SYS, SW) in boost OTG mode	VBAT = 4V, VBUS = 5V, OTG mode enabled, converter switching, PFM enabled, I_{VBUS} = 0A, TS float, TS_IGNORE = 1		250		µA
I_{Q_OTG}	Quiescent battery current (BAT, SYS, SW) in boost OTG mode	VBAT = 4V, VBUS = 5V, OTG mode enabled, converter switching, PFM enabled, I_{VBUS} = 0A		220		µA

6.5 Electrical Characteristics (続き)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBUS / VBAT SUPPLY						
V_{VBUS_OP}	VBUS operating range		3.9		18	V
V_{VBUS_UVLO}	VBUS falling to turn off I2C, no battery	VBUS falling	3.0	3.15	3.3	V
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery	VBUS rising	3.2	3.35	3.5	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 0	6.1	6.5	6.7	V
		VBUS rising, VBUS_OVP = 1	18.2	18.5	18.8	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS falling, VBUS_OVP = 0	5.8	6.0	6.2	V
		VBUS falling, VBUS_OVP = 1	17.6	17.8	18.3	V
V_{SLEEP}	Sleep mode falling threshold	(VBUS - VBAT), VBUS falling	9	45	85	mV
V_{SLEEPZ}	Sleep mode rising threshold	(VBUS - VBAT), VBUS rising	115	220	340	mV
V_{BAT_UVLOZ}	BAT voltage for active I2C, turn on BATFET, no VBUS	VBAT rising	2.3	2.4	2.5	V
V_{BAT_UVLO}	BAT voltage to turnoff I2C, turn off BATFET, no VBUS	VBAT falling, VBAT_UVLO = 0	2.1	2.2	2.3	V
		VBAT falling, VBAT_UVLO = 1	1.7	1.8	1.9	V
V_{BAT_OTG}	BAT voltage rising threshold to enable OTG mode	VBAT rising, VBAT_OTG_MIN = 0	2.9	3.0	3.1	V
		VBAT rising, VBAT_OTG_MIN = 1	2.5	2.6	2.7	V
V_{BAT_OTGZ}	BAT voltage falling threshold to disable OTG mode	VBAT falling, VBAT_OTG_MIN = 0	2.7	2.8	2.9	V
		VBAT falling, VBAT_OTG_MIN = 1	2.3	2.4	2.5	V
$V_{POORSRC}$	Bad adapter detection threshold	VBUS falling	3.6	3.7	3.75	V
$I_{POORSRC}$	Bad adapter detection current source			10		mA
POWER-PATH MANAGEMENT						
$V_{SYS\_REG\_ACC}$	Typical system voltage regulation	ISYS = 0A, VBAT > VSYSMIN, Charge Disabled. Offset above VBAT		50		mV
		ISYS = 0A, V_{BAT} < VSYSMIN, Charge Disabled. Offset above VSYSMIN		230		mV
V_{SYSMIN_RNG}	VSYSMIN register range		2.56		3.84	V
$V_{SYSMIN\_REG\_STEP}$	VSYSMIN register step size			80		mV
$V_{SYSMIN\_REG\_ACC}$	Minimum DC system voltage output	ISYS = 0A, V_{BAT} < VSYSMIN = B00h (3.52V), Charge Disabled	3.52	3.75		V
V_{SYS_SHORT}	VSYS short voltage falling threshold to enter forced PFM			0.9		V
V_{SYS_SHORTZ}	VSYS short voltage rising threshold to exit forced PFM			1.1		V
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3.50		4.80	V
V_{REG_STEP}	Typical charge voltage step			10		mV
V_{REG_ACC}	Charge voltage accuracy	T_J = 25°C	–0.3		0.3	%
		T_J = 0°C - 65°C	–0.5		0.5	%
I_{CHG_RANGE}	Typical charge current regulation range		0.08		5.04	A
I_{CHG_STEP}	Typical charge current regulation step			80		mA

6.5 Electrical Characteristics (続き)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CHG_ACC}	Typical charge current accuracy	VBAT = 3.1V or 3.8V, ICHG = 1760mA	–5		5	%
		VBAT = 3.1V or 3.8V, ICHG = 1040mA	–6		6	%
		VBAT = 3.1V or 3.8V, ICHG = 480mA	–10		10	%
I_{PRECHG_RANGE}	Typical pre-charge current range		40		1000	mA
I_{PRECHG_STEP}	Typical pre-charge current step			20		mA
I_{PRECHG_ACC}	Pre-charge current accuracy when V_{BAT} below V_{SYSMIN} setting	VBAT = 2.5V, IPRECHG = 480mA	–10		10	%
		VBAT = 2.5V, IPRECHG = 200mA	–10		10	%
		VBAT = 2.5V, IPRECHG = 100mA	–30		30	%
		VBAT = 2.5V, IPRECHG = 40mA	–70		70	%
I_{TERM_RANGE}	Typical termination current range		30		1000	mA
I_{TERM_STEP}	Typical termination current step			10		mA
I_{TERM_ACC}	Termination current accuracy	ITERM = 30mA	–70		70	%
		ITERM = 100mA	–15		15	%
		ITERM = 200mA	–10		10	%
V_{BAT_SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising		2.25		V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling, VBAT_UVLO=0		2.05		V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling, VBAT_UVLO=1		1.85		V
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < V_{BAT_SHORTZ}, ITRICKLE = 0	6	20	34	mA
		VBAT < V_{BAT_SHORTZ}, ITRICKLE = 1	64	80	102	mA
V_{BAT_LOWV}	Battery LOW rising voltage threshold to start fast charge	BATLOWV = 3.0V	2.9	3.0	3.1	V
	Battery LOW falling voltage threshold to start fast charge	BATLOWV = 3.0V	2.7	2.8	2.9	V
V_{RECHG}	Battery recharge threshold below V_{REG}	VBAT falling, VRECHG = 0		100		mV
		VBAT falling, VRECHG = 1		200		mV
I_{PMID_LOAD}	PMID discharge load current		20			mA
I_{BAT_LOAD}	Battery discharge load current		20			mA
I_{SYS_LOAD}	System discharge load current		20			mA
BATFET						
V_{SUPPZ}	SYS < BAT threshold to exit supplement mode			5		mV
R_{BATFET}	MOSFET on resistance from SYS to BAT			7	12	mΩ
BATTERY PROTECTIONS						
V_{BAT_OVP}	Battery overvoltage rising threshold	As percentage of VREG	103	104	105	%
V_{BAT_OVPZ}	Battery overvoltage falling threshold	As percentage of VREG	101	102	103	%
I_{BATFET_OCP}	BATFET over-current rising threshold		7			A
I_{BAT_PK}	Battery discharging peak current rising threshold	IBAT_PK = 00	3			A
		IBAT_PK = 01	6			A
		IBAT_PK = 10	9			A
INPUT VOLTAGE / CURRENT REGULATION						

6.5 Electrical Characteristics (続き)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INDPM_RANGE}	Typical input voltage regulation range		3.8		16.8	V
V_{INDPM_STEP}	Typical input voltage regulation step			40		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM=4.6V	–3		3	%
		VINDPM=8V	–3		3	%
		VINDPM=16V	–2		2	%
$V_{INDPM\_BAT\_TRACK}$	Battery tracking VINDPM accuracy	VBAT = 3.9V, VINDPM_BAT_TRACK=1, VINDPM = 4V	4.1	4.25	4.4	V
I_{INDPM_RANGE}	Typical input current regulation range		0.1		3.2	A
I_{INDPM_STEP}	Typical input current regulation step			20		mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500mA, VBUS=5V	450	475	500	mA
		IINDPM = 900mA, VBUS=5V	750	825	900	mA
		IINDPM = 1500mA, VBUS=5V	1350	1425	1500	mA
K_{ILIM}	ILIM Pin Scale Factor, IINREG = K_{ILIM} / R_{ILIM}	INREG = 1.5 A	3000	3333	3666	AΩ
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 1		120		°C
		TREG = 0		60		°C
T_{SHUT}	Thermal Shutdown Rising Threshold	Temperature Increasing		150		°C
T_{SHUT_HYS}	Thermal Shutdown Falling Hysteresis	Temperature Decreasing by T_{SHUT_HYS}		30		°C
THERMISTOR COMPARATORS (CHARGE MODE)						
V_{TS_COLD}	TS pin rising voltage threshold for TH1 comparator to transition from TS_COOL to TS_COLD.	As Percentage to TS pin bias reference (–5°C w/ 103AT), TS_TH1 = 0	74.75	75.25	75.75	%
		As Percentage to TS pin bias reference (0°C w/ 103AT), TS_TH1 = 1	72.75	73.25	73.75	%
V_{TS_COLDZ}	TS pin falling voltage threshold for TH1 comparator to transition from TS_COLD to TS_COOL.	As Percentage to TS pin bias reference (–2.5°C w/ 103AT), TS_TH1 = 0	73.75	74.25	74.75	%
		As Percentage to TS pin bias reference (2.5°C w/ 103AT), TS_TH1 = 1	71.75	72.25	72.75	%
V_{TS_COOL}	TS pin rising voltage threshold for TH2 comparator to transition from TS_PRECOOL to TS_COOL.	As Percentage to TS pin bias reference (5°C w/ 103AT), TS_TH2 = 0	70.5	70.75	71.25	%
		As Percentage to TS pin bias reference (7.5°C w/ 103AT), TS_TH2 = 1	67.25	69.75	70.25	%
		As Percentage to TS pin bias reference (10°C w/ 103AT), TS_TH2 = 2	67.75	68.25	68.75	%
		As Percentage to TS pin bias reference (12.5°C w/ 103AT), TS_TH2 = 3	65.25	66.25	66.75	%
V_{TS_COOLZ}	TS pin falling voltage threshold for TH2 comparator to transition from TS_COOL to TS_PRECOOL.	As Percentage to TS pin bias reference (7.5°C w/ 103AT), TS_TH2 = 0	67.25	69.75	70.25	%
		As Percentage to TS pin bias reference (10°C w/ 103AT), TS_TH2 = 1	67.75	68.25	68.75	%
		As Percentage to TS pin bias reference (12.5°C w/ 103AT), TS_TH2 = 2	65.25	66.25	66.75	%
		As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH2 = 3	64.75	65.25	65.75	%

6.5 Electrical Characteristics (続き)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TS\_PRECOOL}$	TS pin rising voltage threshold for TH3 comparator to transition from TS_NORMAL to TS_PRECOOL.	As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH3 = 0	64.75	65.25	65.75	%
		As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH3 = 1	63.75	64.25	64.75	%
		As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH3 = 2	61.75	62.25	62.75	%
		As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH3 = 3	60.25	60.75	61.25	%
$V_{TS\_PRECOOLZ}$	TS pin falling voltage threshold for TH3 comparator to transition from TS_PRECOOL to TS_NORMAL.	As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH3 =0	63.75	64.25	64.75	%
		As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH3 = 1	61.75	62.25	62.75	%
		As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH3 = 2	60.25	60.75	61.25	%
		As Percentage to TS pin bias reference (25°C w/ 103AT), TS_TH3 = 3	58.5	59.00	59.5	%
$V_{TS\_PREWARM}$	TS pin falling voltage threshold for TH4 comparator to transition from TS_NORMAL to TS_PREWARM.	As Percentage to TS pin bias reference (32.5°C w/ 103AT), TS_TH4 = 0	53.25	53.75	54.25	%
		As Percentage to TS pin bias reference (35°C w/ 103AT), TS_TH4 = 1	51.50	52.00	52.50	%
		As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4 = 2	50.00	50.50	51.00	%
		As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH4 = 3	47.75	48.25	48.75	%
$V_{TS\_PREWARMZ}$	TS pin rising voltage threshold for TH4 comparator to transition from TS_PREWARM to TS_NORMAL.	As Percentage to TS pin bias reference (30°C w/ 103AT), TS_TH4 = 0	55.00	55.50	56.00	%
		As Percentage to TS pin bias reference (32.5°C w/ 103AT), TS_TH4 = 1	53.25	53.75	54.25	%
		As Percentage to TS pin bias reference (35°C w/ 103AT), TS_TH4 = 2	51.50	52.00	52.50	%
		As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4 = 3	50.00	50.50	51.00	%
V_{TS_WARM}	TS pin falling voltage threshold for TH5 comparator to transition from TS_PREWARM to TS_WARM.	As Percentage to TS pin bias reference (42.5°C w/ 103AT), TS_TH5 = 0	46.25	46.75	47.25	%
		As Percentage to TS pin bias reference (45°C w/ 103AT), TS_TH5 = 1	44.25	44.75	45.25	%
		As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH5 = 2	42.50	43.00	43.50	%
		As Percentage to TS pin bias reference (50°C w/ 103AT), TS_TH5 = 3	40.75	41.25	41.75	%
V_{TS_WARMZ}	TS pin rising voltage threshold for TH5 comparator to transition from TS_WARM to TS_PREWARM.	As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH5 = 0	47.75	48.25	48.75	%
		As Percentage to TS pin bias reference (42.5°C w/ 103AT), TS_TH5 = 1	46.25	46.75	47.25	%
		As Percentage to TS pin bias reference (45°C w/ 103AT), TS_TH5 = 2	44.25	44.75	45.25	%
		As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH5 = 3	42.50	43.00	43.50	%
V_{TS_HOT}	TS pin falling voltage threshold for TH6 comparator to transition from TS_WARM to TS_HOT.	As Percentage to TS pin bias reference (55°C w/ 103AT), TS_TH6 = 0	37.25	37.75	38.25	%
		As Percentage to TS pin bias reference (60°C w/ 103AT), TS_TH6 = 1	34.00	34.50	35.00	%

6.5 Electrical Characteristics (続き)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TS_HOTZ}	TS pin rising voltage threshold for TH6 comparator to transition from TS_HOT to TS_WARM.	As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_TH6 = 0	39.25	39.75	40.25	%
		As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_TH6 = 1	35.75	36.25	36.75	%
THERMISTOR COMPARATORS (OTG MODE)						
$V_{TS\_OTG\_COLD}$	TS pin rising voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_COLD.	As Percentage to TS pin bias reference (–20°C w/ 103AT), TS_TH_OTG_COLD = 0	79.50	80.00	80.50	%
		As Percentage to TS pin bias reference (–10°C w/ 103AT), TS_TH_OTG_COLD = 1	76.50	77.00	77.50	%
$V_{TS\_OTG\_COLDZ}$	TS pin falling voltage threshold to transition from TS_OTG_COLD to TS_OTG_NORMAL.	As Percentage to TS pin bias reference (–15°C w/ 103AT), TS_TH_OTG_COLD = 0	78.00	78.50	79.00	%
		As Percentage to TS pin bias reference (–5°C w/ 103AT), TS_TH_OTG_COLD = 1	74.75	75.25	75.75	%
$V_{TS\_OTG\_HOT}$	TS pin falling voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_HOT.	As Percentage to TS pin bias reference (55°C w/ 103AT), TS_OTG_HOT = 00	37.25	37.75	38.25	%
		As Percentage to TS pin bias reference (60°C w/ 103AT), TS_OTG_HOT = 01	34.00	34.50	35.00	%
		As Percentage to TS pin bias reference (65°C w/ 103AT), TS_OTG_HOT = 10	30.75	31.25	31.75	%
$V_{TS\_OTG\_HOTZ}$	TS pin rising voltage threshold to transition from TS_OTG_HOT to TS_OTG_NORMAL.	As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_OTG_HOT = 00	39.25	39.75	40.25	%
		As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_OTG_HOT = 01	35.75	36.25	36.75	%
		As Percentage to TS pin bias reference (62.5°C w/ 103AT), TS_OTG_HOT = 10	32.50	33.00	33.50	%
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency	1.35	1.5	1.65	MHz
MOSFET TURN-ON RESISTANCE						
R_{Q1_ON}	VBUS to PMID on resistance	T_j = –40°C-85°C (typical value is under 25°C)		15	20	mΩ
R_{Q2_ON}	Buck high-side switching MOSFET turn on resistance between PMID and SW	T_j = –40°C-85°C (typical value is under 25°C)		20	27	mΩ
R_{Q3_ON}	Buck low-side switching MOSFET turn on resistance between SW and PGND	T_j = –40°C-85°C (typical value is under 25°C)		16	20	mΩ
OTG MODE CONVERTER						
V_{OTG_RANGE}	Typical OTG mode voltage regulation range		3.8		9.6	V
V_{OTG_STEP}	Typical OTG mode voltage regulation step			80		mV
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 9V	–2		2	%
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 5V	–3		3	%

6.5 Electrical Characteristics (続き)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OTG_RANGE}	Typical OTG mode current regulation range		0.1		3.2	A
I_{OTG_STEP}	Typical OTG mode current regulation step			20		mA
I_{OTG_ACC}	OTG mode current regulation accuracy	IOTG = 1.8A	–3		3	%
		IOTG = 1.5A	–5		5	%
		IOTG = 1.0A	–10		10	%
V_{OTG_UVP}	OTG mode undervoltage falling threshold at PMID			3.4		V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.4	4.6		V
		V_{VBUS} = 9V, I_{REGN} = 20mA	4.8	5.0	5.2	V
V_{REGNZ_OK}	REGN not good falling threshold	Converter switching		3.2		V
		Converter not switching		2.3		V
I_{REGN_LIM}	REGN LDO current limit	V_{VBUS} = 5V, VREGN = 4.3V	20			mA
$I_{TS\_BIAS\_FAULT}$	Rising threshold to transition from TSBIAS good condition to fault condition	REGN=5V; ISINK applied on TS_BIAS pin	2.5	4.5	8	mA
$I_{TS\_BIAS\_FAULTZ}$	Falling threshold to transition from TSBIAS fault condition to good condition	REGN=5V; ISINK applied on TS_BIAS pin	2	3.85	7	mA
PG THRESHOLD						
PG_TH	VBUS voltage falling threshold to release $\overline{PG}$ pin pulldown	PG_TH = 000b		3.7		V
		PG_TH = 001b		7.4		V
		PG_TH = 010b		8.0		V
		PG_TH = 011b		10.4		V
		PG_TH = 100b		11.0		V
		PG_TH = 101b		13.4		V
		PG_TH = 110b		14.0		V
		PG_TH = 111b		13.7		V
PG_THz	VBUS voltage rising threshold to enable $\overline{PG}$ pin pulldown	PG_TH = 000b		3.9		V
		PG_TH = 001b		7.9		V
		PG_TH = 010b		8.5		V
		PG_TH = 011b		10.9		V
		PG_TH = 100b		11.5		V
		PG_TH = 101b		13.9		V
		PG_TH = 110b		14.5		V
		PG_TH = 111b		14.2		V
ADC MEASUREMENT ACCURACY AND PERFORMANCE						
t_{ADC_CONV}	Conversion-time, Each Measurement	ADC_SAMPLE = 00		24		ms
		ADC_SAMPLE = 01		12		ms
		ADC_SAMPLE = 10		6		ms
		ADC_SAMPLE = 11		3		ms

6.5 Electrical Characteristics (続き)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

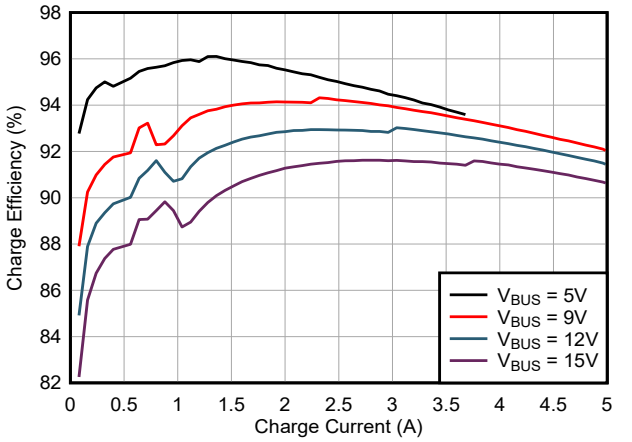
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC_RES	Effective Resolution	ADC_SAMPLE = 00	11	12		bits
		ADC_SAMPLE = 01	10	11		bits
		ADC_SAMPLE = 10	9	10		bits
		ADC_SAMPLE = 11	8	9		bits
ADC MEASUREMENT RANGE AND LSB						
IBUS_ADC	ADC Bus Current Reading (both forward and OTG)	Range	–5		5	A
		LSB		2.5		mA
VBUS_ADC	ADC VBUS Voltage Reading	Range	0		20	V
		LSB		5		mV
VPMID_ADC	ADC PMID Voltage Reading	Range	0		20	V
		LSB		5		mV
VBAT_ADC	ADC BAT Voltage Reading	Range	0		5	V
		LSB		1.25		mV
VBAT_ADC	ADC BAT Voltage Reading Accuracy	Accuracy @ 4V, ADC_SAMPLE = 00	–0.5		0.5	%
VSYS_ADC	ADC SYS Voltage Reading	Range	0		5	V
		LSB		1.25		mV
IBAT_ADC	ADC BAT Current Reading	Range	–10		5	A
		LSB		5		mA
TS_ADC	ADC TS Voltage Reading	Range as a percent of REGN	0		99.9	%
	ADC TS Voltage Reading	LSB		0.098		%
TDIE_ADC	ADC Die Temperature Reading	Range	–40		150	°C
		LSB		0.5		°C
ADCIN_ADC	ADC ADCIN Voltage Reading	Range	0		1	V
ADCIN_ADC	ADC ADCIN Voltage Reading	LSB		0.25		mV
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL		0.78			V
V_{IL}	Input low threshold level, SDA and SCL				0.42	V
V_{OL_SDA}	Output low threshold level	Sink current = 5mA, 1.2V VDD			0.3	V
I_{BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC OUTPUT PIN ($\overline{INT}$, $\overline{PG}$, STAT)						
V_{OL}	Output low threshold level	Sink current = 5mA			0.3	V
I_{OUT_BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC INPUT PIN ($\overline{CE}$, $\overline{QON}$)						
V_{IH_CE}	Input high threshold level, /CE		0.78			V
V_{IL_CE}	Input low threshold level, /CE				0.4	V
$I_{IN\_BIAS\_CE}$	High-level leakage current, /CE	Pull up rail 1.8V			1	µA
V_{IH_QON}	Input high threshold level, /QON		1.3			V
V_{IL_QON}	Input low threshold level, /QON				0.4	V
V_{QON}	Internal /QON pull up	/QON is pulled up to VAA internally		5		V
R_{QON}	Internal /QON pull up resistance			250		kΩ

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VBUS / VBAT POWER UP						
t_{VBUS_OVP}	VBUS OVP deglitch time to set VBUS_OVP_STAT and VBUS_OVP_FLAG			200		µs
$t_{POORSRC}$	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{TOP_OFF}	Typical top-off timer accuracy		14	17.5	21	min
			28	35	42	min
			39	52	63	min
t_{SAFETY_TRKCHG}	Charge safety timer accuracy in trickle charge		1	1.15	1.3	hr
t_{SAFETY_PRECHG}	Charge safety timer accuracy in pre-charge	PRECHG_TMR = 0	2.1	2.3	2.6	hr
		PRECHG_TMR = 1	0.53	0.6	0.65	hr
t_{SAFETY}	Charge safety timer accuracy in fast charge	CHG_TMR = 0	12.5	14	15.5	hr
		CHG_TMR = 1	25	27	31	hr
BATFET CONTROL						
t_{BATFET_DLY}	Time after writing to BATFET_CTRL before BATFET turned off for ultra-low power mode or shutdown	BATFET_DLY = 1		12		s
		BATFET_DLY = 0		24		ms
t_{SM_EXIT}	Deglitch time for $\overline{QON}$ to be pulled low in order to exit from ultra-low power mode	TSM_EXIT = 0	0.6	0.7	0.8	s
		TSM_EXIT = 1	8.7	10.5	12.3	ms
t_{QON_RST}	Time $\overline{QON}$ is held low to initiate system power reset	TQON_RST = 0	9.3	11	12.8	s
		TQON_RST = 1	17.5	21	24.5	s
t_{BATFET_RST}	Duration that BATFET is disabled during system power reset			400		ms
I2C INTERFACE						
f_{SCL}	SCL clock frequency	See Serial Interface section for more details			1.0	MHz
C_b	Capacitive load for each bus line				550	pF
DIGITAL CLOCK AND WATCHDOG						
t_{LP_WDT}	Watchdog Reset time (EN_HIZ = 1, WATCHDOG = 160s)		100	160		s
t_{WDT}	Watchdog Reset time (EN_HIZ = 0, WATCHDOG = 160s)		136	160		s

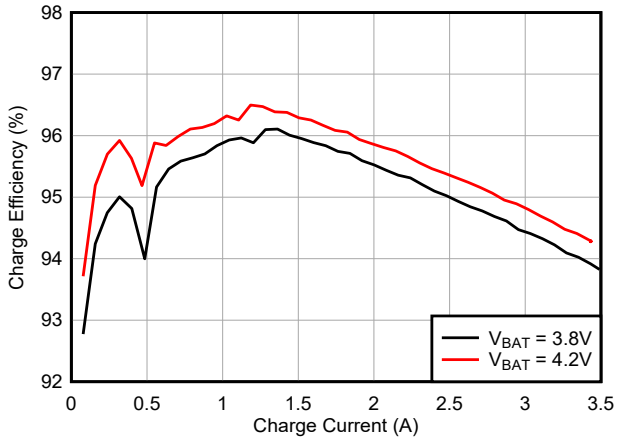
6.7 Typical Characteristics

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS} = 20µF, L = 1µH (SRP3212-1R0M21) (unless otherwise specified)



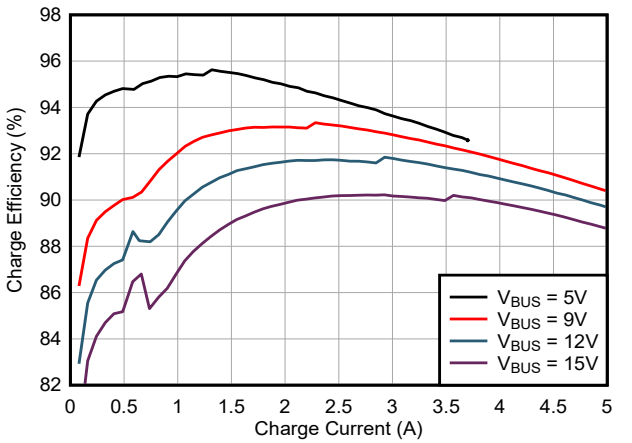
VBAT = 3.8 V DCR = 10 mΩ (Würth 74437346010)

図 6-1. Charge Efficiency vs Charge Current



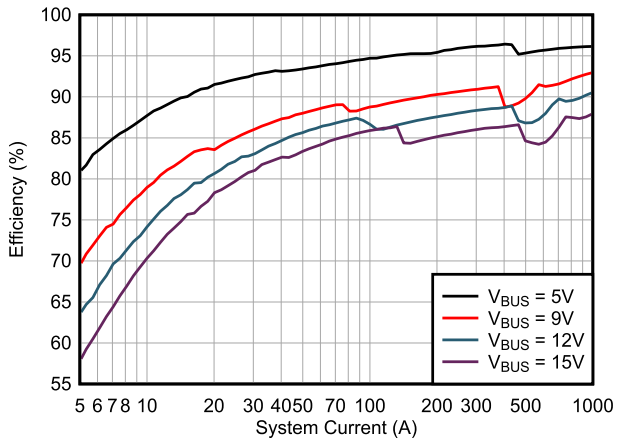
VBUS = 5 V DCR = 10 mΩ (Würth 74437346010)

図 6-2. Charge Efficiency vs Charge Current



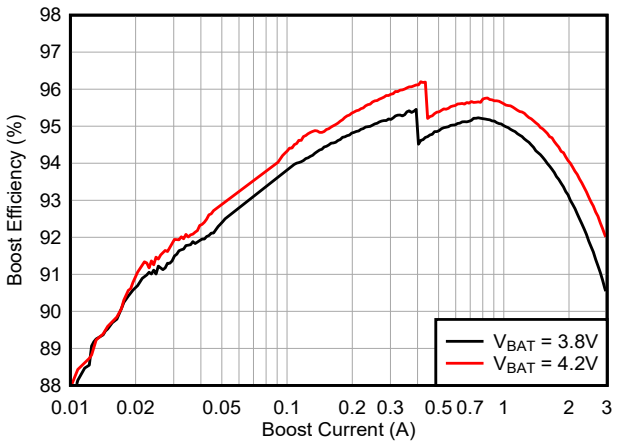
VBAT = 3.8 V DCR = 19 mΩ

図 6-3. Charge Efficiency vs Charge Current



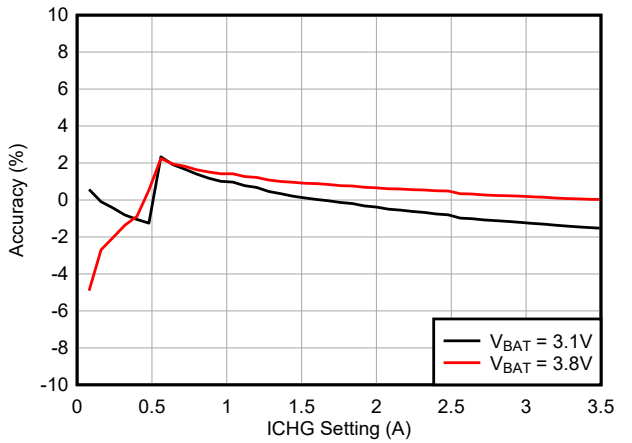
VBAT = 4.2V DCR = 19 mΩ

図 6-4. System Efficiency vs System Current



VOTG = 5.12 V DCR = 19 mΩ

図 6-5. Boost Mode Efficiency vs VBUS Load Current

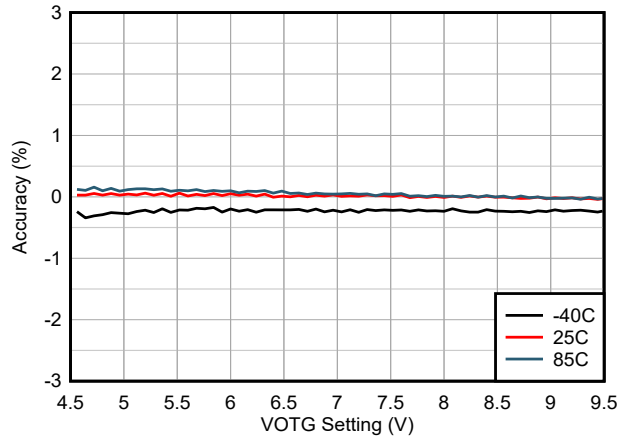


VBUS = 5 V

図 6-6. Charge Current Accuracy vs Charge Current I²C Setting

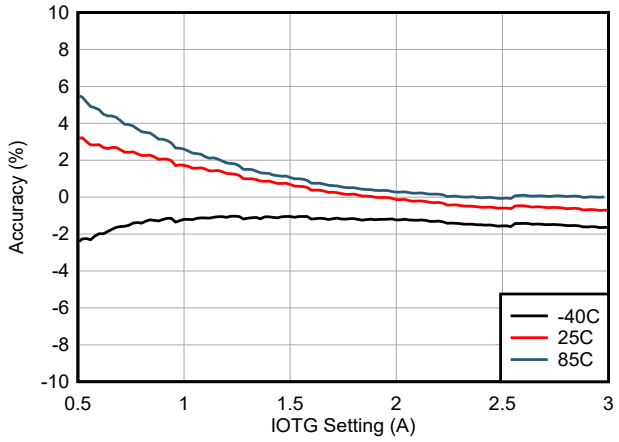
6.7 Typical Characteristics (continued)

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS} = 20µF, L = 1µH (SRP3212-1R0M21) (unless otherwise specified)



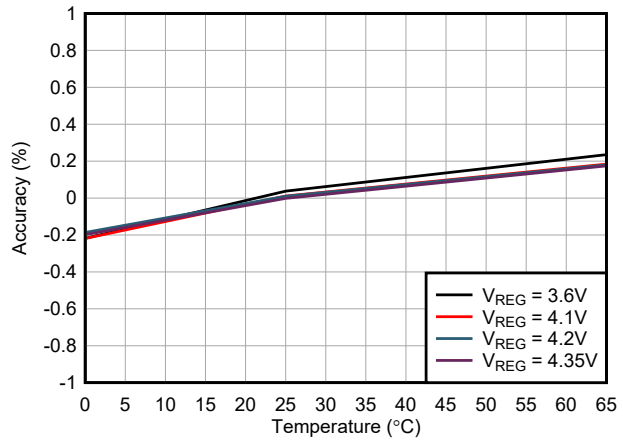
VBAT = 3.8 V

図 6-7. Boost Mode Voltage Accuracy vs VOTG I²C Setting



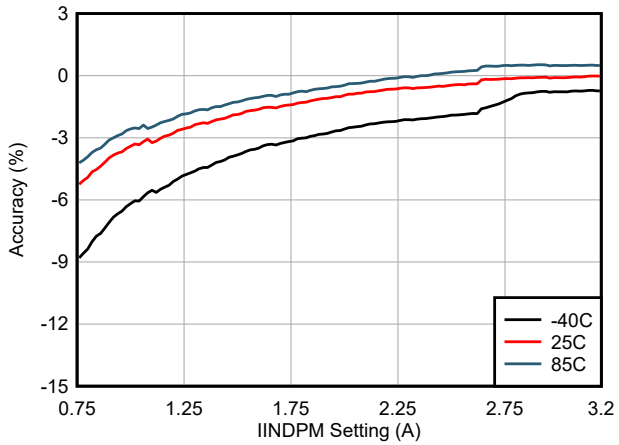
VBAT = 3.8 V

図 6-8. Boost Mode Current Limit Accuracy vs IOTG I²C Setting



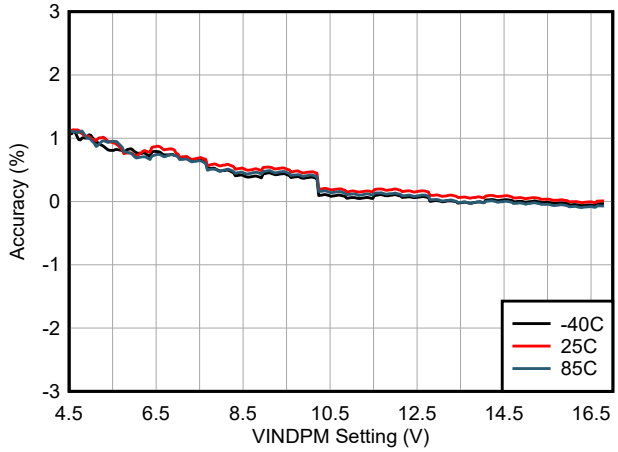
VBUS = 5 V

図 6-9. BAT Regulation Voltage vs Temperature



VBUS = 5 V

図 6-10. Input Current Limit vs IINDPM I²C Setting



VBAT = 3.8 V

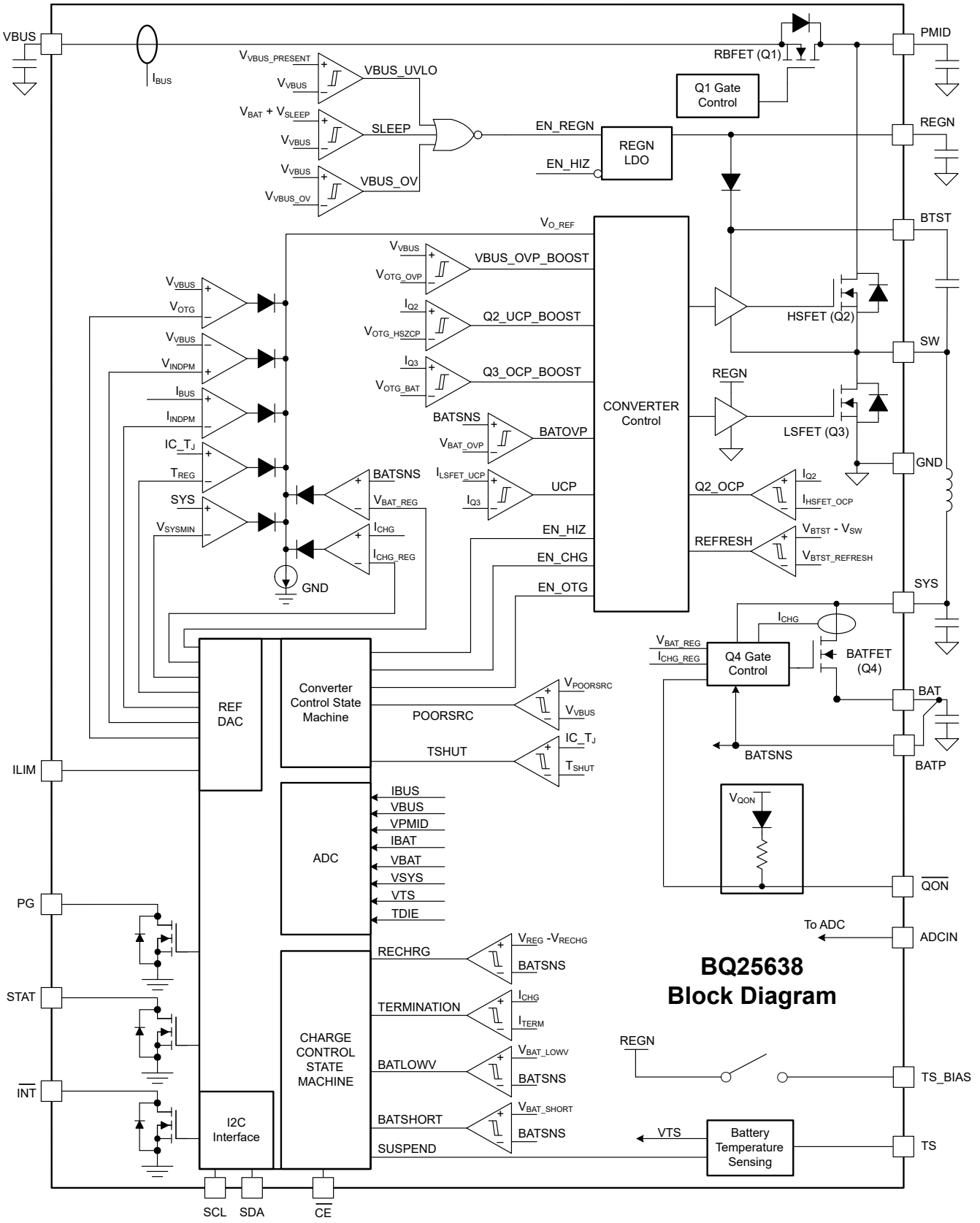
図 6-11. Input Voltage Limit vs VINDPM I²C Setting

7 Detailed Description

7.1 Overview

BQ25638 is a highly-integrated 5 A switch mode battery charger with NVDC power path management for single cell Li-Ion and Li-polymer batteries. It features fast charging with high input voltage supporting a wide range of portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery running time during discharging phase. Its input voltage and input current regulation deliver maximum charging power to the battery without overloading the input source.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power-On-Reset (POR)

BQ25638 powers internal bias circuits from the higher voltage of VBUS versus BAT. When either voltage rises above its undervoltage lockout (UVLO) threshold, all registers are reset to their POR values and the I^2C interface is enabled for communication. A non-maskable $\overline{INT}$ pulse is generated, after which the host can access all of the registers.

7.3.2 Device Power Up from Battery

If only battery is present and the voltage is above depletion threshold (V_{BAT_UVLOZ}), BQ25638 performs a power-on reset then turns on BATFET to connect the battery to system. The REGN stays off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

7.3.3 Device Power Up from Input Source

When an input source is plugged in with VBAT < V_{BAT_UVLOZ}, BQ25638 performs a power-on reset then checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. REGN LDO power up (セクション 7.3.3.1)
2. Poor source qualification (セクション 7.3.3.2)
3. Input voltage limit threshold setting (セクション 7.3.3.3)
4. Converter power-up (セクション 7.3.3.4)

7.3.3.1 REGN LDO Power Up

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- VBUS above V_{VBUS_UVLOZ}
- VBUS above V_{BAT} + V_{SLEEPZ}
- EN_HIZ = 0
- After 220-ms delay is completed

If any one of the above conditions is not valid, the REGN LDO and the converter power stage remain off with the converter disabled. In this state, the battery supplies power to the system.

7.3.3.2 Poor Source Qualification

After the REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to move forward to the next power on steps.

1. VBUS voltage below V_{VBUS_OVP}
2. VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$

7.3.3.3 Input Voltage Limit Threshold Setting (VINDPM Threshold)

BQ25638 supports a wide range of input voltage limit (3.8 V – 16.8V). Its POR default VINDPM is set at 4.4V. The charger also supports dynamic VINDPM tracking, which tracks the battery voltage to ensure a sufficient margin between input and battery voltages for proper operation of the buck converter. This function is enabled by default, and can be disabled by clearing the VINDPM_BAT_TRACK register bit to 0. When enabled, the actual input voltage limit will be the higher of the VINDPM register and $V_{INDPM\_BAT\_TRACK}$ (VBAT + 350 mV offset).

7.3.3.4 Converter Power-Up

After the input current and voltage limits are set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery. Converter startup requires the following conditions:

- VBUS has passed poor source qualification (セクション 7.3.3.2)
- VBUS > V_{BAT} + V_{SLEEPZ}
- V_{VBUS} < V_{VBUS_OVP}
- EN_HIZ = 0
- V_{SYS} < V_{SYS_OVP}
- T_J < T_{SHUT}

BQ25638 provides soft start when system rail is ramped up. Concurrently, the system short protection limits the output current to approximately 0.5A when the system rail is below V_{SYS_SHORT}.

This device uses a highly efficient 1.5 MHz, fixed frequency pulse width modulated (PWM) step-down switching regulator. The internally compensated feedback loop keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

In order to improve light-load efficiency, the device switches to PFM control at light load condition. The DIS_PFM_FWD and DIS_PFM_OTG bits can be used to disable the PFM operation in buck and boost respectively.

7.3.3.5 Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overloading the input source. The algorithm automatically identifies maximum input current limit of power source without entering VINDPM to avoid input source overload.

This feature is enabled by default (EN_ICO=1) and can be disabled by setting EN_ICO bit to 0. The algorithm runs automatically when EN_ICO bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected (EN_ICO = 1 is required for FORCE_ICO to work).

The actual input current limit used by the Dynamic Power Management is reported in ICO_IINDPM register while Input Current Optimizer is enabled (EN_ICO = 1) or set by IINDPM register when the algorithm is disabled (EN_ICO = 0). In addition, the current limit is clamped by ILIM pin unless EN_EXTILIM bit is 0 to disable ILIM pin function .

When the algorithm is enabled, it runs continuously to adjust the input current limit of Dynamic Power Management (IINDPM) using ICO_IINDPM register until ICO_STAT[1:0] and ICO_FLAG bits are set (the ICO_FLAG bit indicates any change in ICO_STAT[1:0] bits). The algorithm operates depending on battery voltage:

1. When the battery voltage is below VSYSMIN, the algorithm starts ICO_IINDPM register with IINDPM which is the maximum input current limit allowed by system.
2. When the battery voltage is above VSYSMIN, the algorithm starts ICO_IINDPM register with 500 mA which is the minimum input current limit to minimize adapter overload.

When the optimal input current is identified, the ICO_STAT[1:0] and ICO_FLAG bits are set to indicate the input current limit in ICO_IINDPM register will not be changed until the algorithm is forced to run by the following events (these events also reset the ICO_STAT[1:0] bits to '01'):

1. A new input source is plugged-in, or EN_HIZ bit is toggled
2. IINDPM register is changed
3. VINDPM register is changed
4. FORCE_ICO bit is set to 1
5. VBUS_OVP event

If the optimal current is not identified (for example if output power < maximum input power), the ICO routine is suspended until more power is needed from the input. In this case, the ICO_STAT bits are set to '11'.

7.3.3.6 Switching Frequency and Dithering Feature

Normally, the device switches with a fixed frequency. The charger also supports a frequency dithering function to improve EMI performance and help pass IEC-CISPR 22 specification. This function is disabled by default with setting EN_DITHER=00b. It can be enabled by setting EN_DITHER=01/10/11b, the switching frequency

is not fixed when dithering is enabled, it varies within determined range by EN_DITHER setting, 01/10/11b is corresponding to ±2%/4%/6% switching frequency. The larger dithering range is selected, the smaller EMI noise peak will be, but at same time slightly larger VBUS/VSYS capacitor voltage ripple is generated. Therefore the dithering frequency range selection is a trade-off between EMI noise peak and VSYS/VBUS voltage ripple, recommend to choose the lowest dithering range which can pass IEC-CISPR 22 specification. The patented dithering pattern can improve EMI performance from switching frequency and up to 30MHz high frequency range which covers the entire conductive EMI noise range.

7.3.4 Power Path Management

BQ25638 accommodates a wide range of input sources from USB, wall adapter, to car charger. It provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

7.3.4.1 Narrow VDC Architecture

BQ25638 uses the Narrow VDC architecture (NVDC) with BATFET separating the system from battery. The minimum system voltage is set by VSYSMIN register setting. Even with a fully depleted battery, the system is regulated to the minimum system voltage. If charging is enabled, the BATFET operates in linear mode (LDO mode). The default minimum system voltage at POR is 3.52V.

As the battery voltage rises above the minimum system voltage, the BATFET is turned fully on and the voltage difference between the system and battery is the R_{DSON} of BATFET multiplied by the charging current. When battery charging is disabled and VBAT is above minimum system voltage setting, or charging is terminated, the system is regulated 50mV (typical) above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

7.3.4.2 Dynamic Power Management

To maximize input current without overloading the adapter, the charger features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When an input source is over-loaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters supplement mode where the BATFET turns on and the battery starts discharging to support the system from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT and/or IDPM_STAT is/are set high. 図 7-1 shows the DPM response with 9-V/1.2-A adapter, 3.2-V battery, 2.8-A charge current, and 3.4-V minimum system voltage setting.

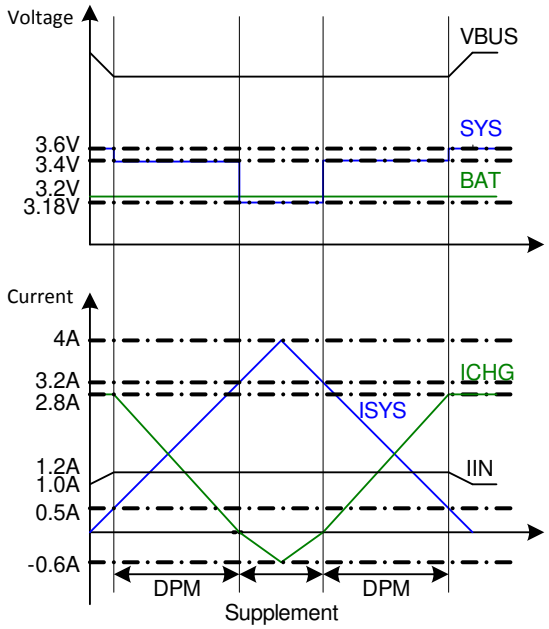


図 7-1. DPM Response

7.3.4.2.1 Input Current Limit on ILIM Pin

For safe operation, the device has an additional hardware pin on ILIM to limit the maximum input current on ILIM pin. The maximum input current is set by a resistor from ILIM pin to GND as:

$$I_{INREG} = \frac{K_{ILIM}}{R_{ILIM}} \quad (1)$$

The actual input current is limited to the lower of the two values set by ILIM pin and IINDPM register bits. The device regulates ILIM pin at 0.8 V. If ILIM voltage exceeds 0.8 V, the device enters input current regulation (refer to Dynamic Power Management).

The ILIM pin can also be used to monitor input current. The input current is proportional to the voltage on ILIM pin and can be calculated by:

$$IIN = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8} \quad (2)$$

The ILIM pin function is disabled when EN_EXTILIM bit is set to 0. When the pin is disabled, both input current limit and monitoring functions are not available.

An RC filter in parallel with R_{ILIM} is required when input current setting on ILIM pin is either:

1. Below 400 mA or
2. Above 2 A with 2.2-µH inductor

The value of the RC filter is 1.2 kΩ and 330 nF, respectively.

7.3.4.3 High Impedance (HIZ) Mode

The host may place the device into high impedance mode by writing EN_HIZ = 1. In high impedance mode, RBFET (Q1), HSFET (Q2) and LSFET (Q3) are turned off. The RBFET and HSFET block current flow to and from VBUS, putting the VBUS pin into a high impedance state. The BATFET (Q4) is turned on to connect the BAT to SYS. During high impedance mode, REGN is disabled and the digital clock is slowed to conserve power.

7.3.5 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 5-A charge current. The 7 mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

7.3.5.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit = 1 and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in 表 7-1. The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through I^2C.

表 7-1. Charging Parameter Default Settings

	VREG	VRECHG	ITRICKLE	IPRECHG	ICHG	ITERM	TOPOFF TIMER
BQ25638	4.2 V	VREG - 100mV	80 mA	200 mA	2,000 mA	200 mA	Disabled

A new charge cycle starts when the following conditions are valid:

- Converter starts per the conditions in セクション 7.3.3.4
- EN_CHG = 1
- $\overline{CE}$ pin is low
- No thermistor fault on TS
- No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM or thermal regulation. When a fully charged battery is discharged below VRECHG, the device automatically starts a new charging cycle. After charging terminates, toggling $\overline{CE}$ pin or EN_CHG bit will also initiate a new charging cycle.

The STAT output indicates the charging status. Refer to セクション 7.3.8.2 for details of STAT pin operation. In addition, the status register (CHG_STAT) indicates the different charging phases as :

- 000 – Not Charging
- 001 – Trickle Charge ($V_{BAT} < V_{BAT\_SHORTZ}$)
- 010 – Pre-charge ($V_{BAT\_SHORTZ} < V_{BAT} < V_{BAT\_LOWV}$)
- 011 – Fast Charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Top-off Timer Active Charging
- 111 – Charge Termination Done

When the CHG_STAT transitions to any of these states, including when the charge cycle completes, an INT pulse is asserted to notify the host.

7.3.5.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage and an optional top-off charging phase. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

If the charger device is in DPM regulation or thermal regulation during charging, the charging current can be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

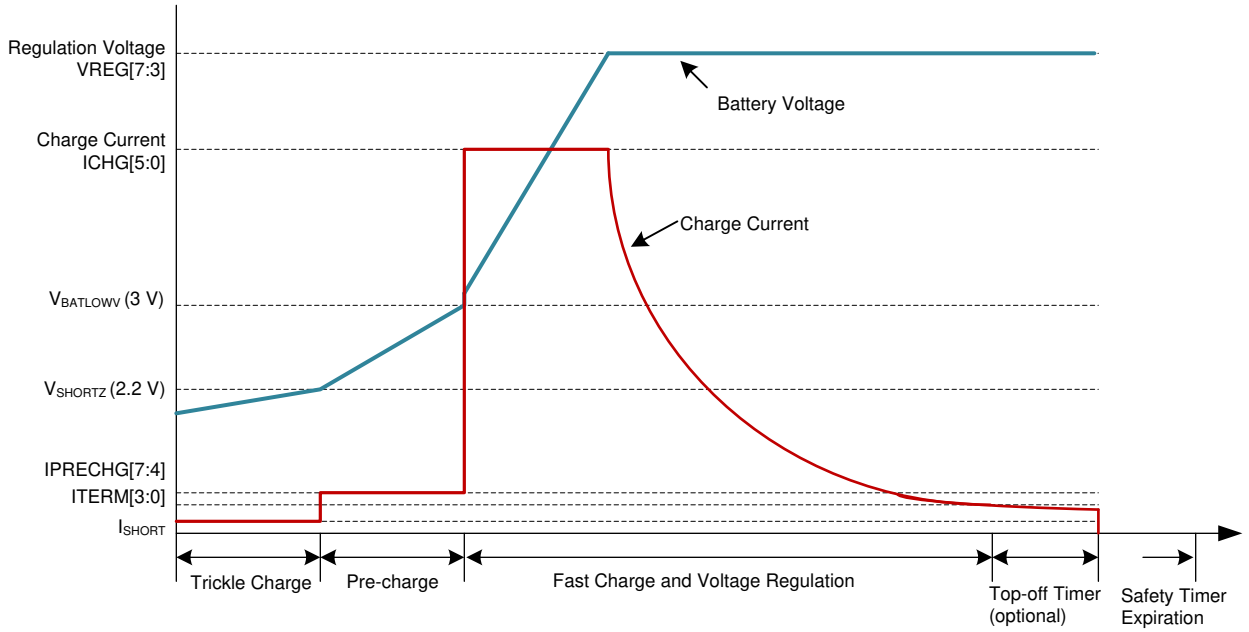


図 7-2. Battery Charging Profile

7.3.5.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, the converter is in constant-voltage regulation and the battery current is below ITERM. Because constant-voltage regulation is required for termination, the device does not terminate while IINDPM, VINDPM or thermal regulation loops are active. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage supplement mode. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

When termination occurs, the status register CHG_STAT is set to 111, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents, due to the comparator offset, the actual termination current may be 10 mA-20 mA higher than the termination target. An optional snubber circuit can be added from the SW pin to ground, to improve termination accuracy at low currents. Suggested values for the snubber circuit are 28 Ω and 3 nF.

In order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. When the top-off timer is enabled and termination occurs, the status register CHG_STAT is set to 110. The top-off timer follows safety timer constraints, such that if the safety timers suspend, so will the top-off timer. Similarly, if the safety timers count at half-clock rate, so will the top-off timer. Refer to セクション 7.3.5.5 for the list of conditions. The host can read CHG_STAT to find out the termination status.

Top-off timer gets reset by any of the following conditions:

1. Charging cycle stop and restart (toggle CE pin, toggle EN_CHG bit, charged battery falls below recharge threshold or adapter removed and replugged)
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. CHG_FLAG is set to 1 when entering top-off timer segment and again when the top-off timer expires.

7.3.5.4 Thermistor Qualification

The charger provides a single thermistor input (TS) for battery temperature monitor. The TS pin can be ignored by setting TS_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS is always good for charging and OTG modes, and TS_STAT will always report TS_NORMAL. The TS pin may be left floating if TS_IGNORE is set to 1.

When TS_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information according to the configurable profile described in セクション 7.3.5.4.1. When the battery temperature crosses from one temperature range to another, TS_STAT is updated accordingly, and the charger sets the FLAG bit for the newly-entered temperature range, unless it is TS_NORMAL, which has no FLAG. If TS_MASK is set to 0, any change to TS_STAT, including a transition to TS_NORMAL, will generate an $\overline{INT}$ pulse.

7.3.5.4.1 Advanced Temperature Profile in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges. As battery technology continues to evolve, battery manufacturers have released temperature safety specifications that extend beyond the JEITA standard. BQ25638 features a highly flexible temperature-based charging profile to meet these advanced specifications while remaining backwards compatible with the original JEITA standard.

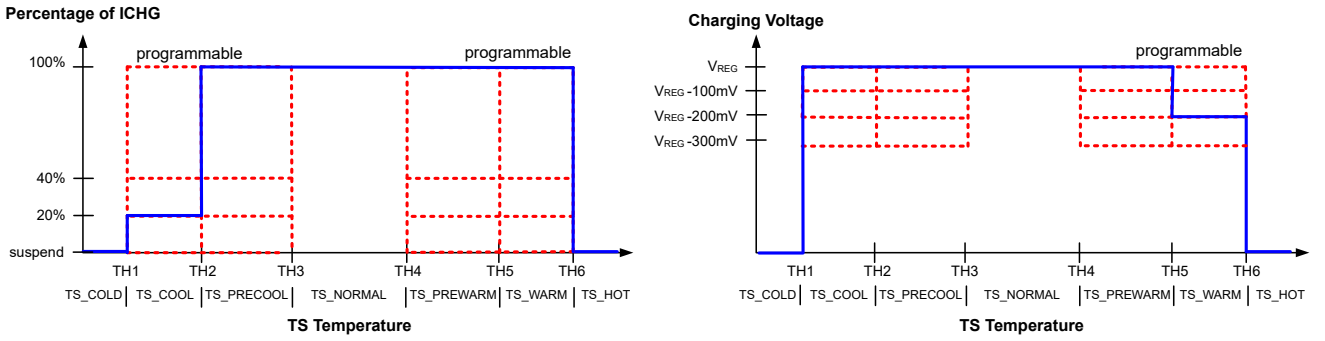


図 7-3. Advanced TS Charging Values

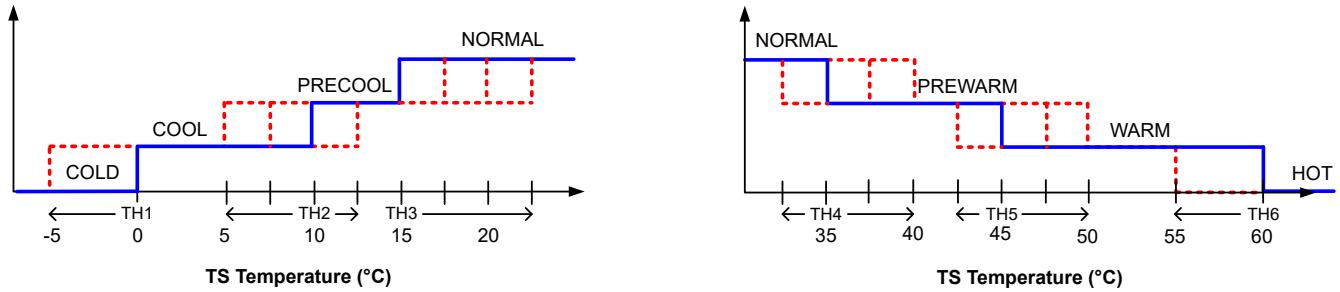


図 7-4. Advanced TS Charging Regions

表 7-2. TS Threshold Settings (default values in blue)

REGION	CONTROL REGISTER	CONTROL VALUE
COLD	TS_TH1	-5ºC
		0ºC
COOL	TS_TH2	5ºC
		7.5ºC
		10ºC
		12.5ºC

表 7-2. TS Threshold Settings (default values in blue) (続き)

REGION	CONTROL REGISTER	CONTROL VALUE
PRECOOL	TS_TH3	**15ºC**
		17.5ºC
		20ºC
		22.5ºC
PREWARM	TS_TH4	32.5ºC
		35ºC
		37.5ºC
		40ºC
WARM	TS_TH5	42.5ºC
		45ºC
		47.5ºC
		50ºC
HOT	TS_TH6	55ºC
		60ºC

Charging termination and the charging safety timer are adjusted within the temperature zones to reflect changes to the charging current. When IPRECHG and ICHG are reduced to 20% or 40% in the cool or warm temperature zones, the charging safety timer will count at half rate. If charging is suspended, the safety timer is suspended, the STAT pin blinks and CHG_STAT is set to 000 (not charging). Charging termination is still enabled (when EN_TERM=1) with termination current (ITERM) unchanged when charging current is reduced in cool or warm tempreature zones.

7.3.5.4.2 TS Pin Thermistor Configuration

The typical TS resistor network is illustrated below.

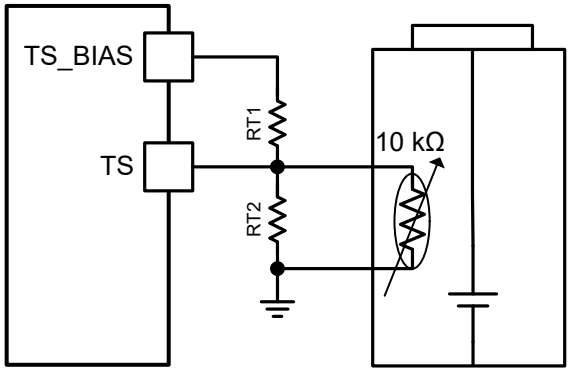


図 7-5. TS Resistor Network

The value of RT1 and RT2 are determined from the resistance of the recommended 103AT-2 thermistor at 0ºC and 60 ºC ($RTH_{0ºC}$= 27.28 kΩ and $RTH_{60ºC}$ = 3.02 kΩ) and the corresponding voltage thresholds V_{TS_COLD} and V_{TS_HOT} (expressed as percentage of REGN with value between 0 and 1).

$$RT2 = \frac{RTH_{0ºC} \times RTH_{60ºC} \times \left(\frac{1}{V_{TS\_0ºC}} - \frac{1}{V_{TS\_60ºC}}\right)}{RTH_{60ºC} \times \left(\frac{1}{V_{TS\_60ºC}} - 1\right) - RTH_{0ºC} \times \left(\frac{1}{V_{TS\_0ºC}} - 1\right)} \quad (3)$$

$$RT1 = \frac{\frac{1}{V_{TS\_0ºC}} - 1}{\frac{1}{R_{T2}} + \frac{1}{RTH_{0ºC}}} \quad (4)$$

$$RT2 = \frac{RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{1}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{1}{VT1} - 1\right)} \quad (5)$$

$$RT1 = \frac{\frac{1}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (6)$$

Assuming a 103AT-2 NTC thermistor on the battery pack, the RT1 and RT2 are calculated to be 5.24 kΩ and 30.31 kΩ respectively.

If the thermistor is biased from TS_BIAS, the maximum current should be checked against $I_{TS\_BIAS\_FAULT}$. For the worst-case condition of thermistor at 0 Ω impedance (very hot), the bias current is:

$$I_{BIAS\_MAX} = \frac{V_{REGN}}{RT1} \quad (7)$$

For 5.30 kΩ RT1, this has a maximum I_{BIAS} of 0.94 mA, which is well below the minimum $I_{TS\_BIAS\_FAULT}$ threshold. The 103AT-2 NTC thermistor is the recommended thermistor and has 10 kΩ nominal impedance. Using a lower impedance thermistor will change the value of R1 and may produce a bias current that exceeds the TS_BIAS pin fault threshold. TS_STAT[2:0] is set to 111.

7.3.5.4.3 Cold/Hot Temperature Window in OTG Mode

For battery protection during boost OTG, the device monitors the battery temperature to be within the TS_TH_OTG_COLD to TS_TH_OTG_HOT thresholds. For a 103AT-2 NTC thermistor with RT1 of 5.3 kΩ and RT2 of 31.1 kΩ, TS_TH_OTG_COLD default is -10°C and TS_TH_OTG_HOT default is 60°C. When temperature is outside of this range, the OTG mode is suspended with REGN remaining on. In addition, VBUS_STAT bits are set to 000, TS_STAT is set to 001 (TS_OTG_COLD) or 010 (TS_OTG_HOT), and TS_FLAG is set. In boost OTG, the converter stops switching. Once the battery temperature returns to normal temperature, the boost OTG is restarted and TS_STAT returns to 000 (TS_NORMAL).

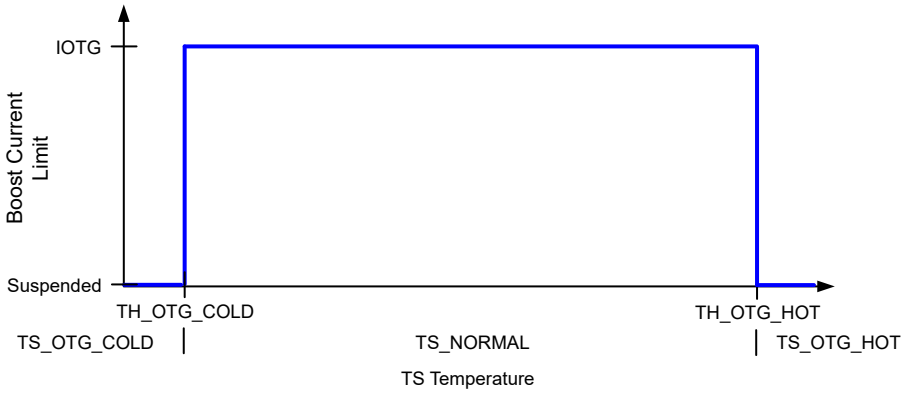


図 7-6. TS Pin Thermistor Sense Threshold in Boost Mode

7.3.5.4.4 JEITA Charge Rate Scaling

The TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM and TS_ISET_WARM cool and warm charge current fold backs are based on a 1C charging rate. The 1C rate is the battery capacity in mA-hours

divided by 1 hour, so that a 500 mA-hour battery would have a 1C charging rate of 500 mA. The same battery would have a 2C charging rate of 1,000 mA. In order to convert the charging foldback, the host must set the CHG_RATE register to the C rate for the battery. This scales the foldback accordingly.

When TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM or TS_ISET_WARM is set to either 00 (suspend) or 11 (unchanged), the CHG_RATE setting has no effect. A summary is provided in 表 7-3

表 7-3. ICHG Fold Back

TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM or TS_ISET_WARM	CHG_RATE	FOLD-BACK CURRENT AS PERCENTAGE OF ICHG
00	Any	0% (Suspended)
01 (20%)	00 (1C)	20%
	01 (2C)	10%
	10 (4C)	5%
	11 (6C)	3.3%
10 (40%)	00 (1C)	40%
	01 (2C)	20%
	10 (4C)	10%
	11 (6C)	6.6%
11	Any	100%

7.3.5.4.5 TS_BIAS Pin

The device has the TS_BIAS pin to isolate the battery temperature sensing thermistor and associated resistor-divider from REGN. The 103AT-2 thermistor with typical resistor-divider network requires about 400 µA to bias. The charger provides TS_BIAS pin, which is internally connected to the REGN LDO via a back-to-back MOSFET. When no temperature measurement is being taken, the switch is disabled to disconnect the thermistor and resistor-divider from the REGN LDO, saving the 400 µA bias current from being expended unnecessarily. Additionally, if TS_IGNORE = 1, TS_BIAS pin gets disconnected from REGN.

The TS_BIAS pin has short-circuit protection. If a short is detected on the TS_BIAS pin, the switch will be disabled to to disconnect the short from REGN. If this condition occurs, TS_STAT is set to 111. Charging and OTG modes are suspended until the short is removed.

7.3.5.5 Charging Safety Timers

BQ25638 has three built-in safety timers to prevent extended charging cycle due to abnormal battery conditions. The fast charge safety timer and pre-charge safety timers are set through I^2C CHG_TMR and PRECHG_TMR fields, respectively. The trickle charge timer is fixed as 1 hour.

The trickle charging, pre-charging and fast charging safety timers can be disabled by setting EN_SAFETY_TMRS = 0. EN_SAFETY_TMRS can be enabled anytime regardless of which charging stage the charger is in. Each timer will start to count as soon as the following two conditions are simultaneously true: EN_SAFETY_TMRS=1 and the corresponding charging stage is active.

When either the fast charging, trickle charging or pre-charging safety timer expires, the SAFETY_TMR_STAT and SAFETY_TMR_FLAG bits are set to 1.

Events that cause a reduction in charging current will also cause the charging safety timer to count at half-clock rate if EN_TMR2X bit is set.

During faults which suspend charging, the charge, pre-charge and trickle safety timers are also suspended, regardless of the state of the EN_TMR2X bit. Once the fault goes away, charging resumes and the safety timer resumes where it stopped.

The charging safety timer and the charging termination can be disabled at the same time. Under this condition, the charging will keep running until it is disabled by the host.

7.3.6 USB On-The-Go (OTG)

7.3.6.1 Boost OTG Mode

The device supports boost converter operation to deliver power from the battery to VBUS. The output voltage is set in VOTG and the maximum current is set in IOTG. VBUS_STAT is set to 111 upon a successful entry into boost OTG. The boost operation is enabled when the following conditions are met:

1. BAT above V_{BAT_OTG}
2. VBUS less than $V_{BAT}+V_{SLEEP}$
3. Boost mode operation is enabled (EN_OTG = 1)
4. $V_{TS\_OTG\_HOT} < V_{TS} < V_{TS\_OTG\_COLD}$
5. $V_{REGN} > V_{REGN\_OK}$
6. 30 ms delay after EN_OTG = 1
7. Boost mode regulation voltage (VOTG) is greater than 105% of battery voltage.

Any of the following conditions will cause an exit from boost OTG. Unless otherwise indicated, exit is into battery-only mode by setting EN_OTG = 0.:

- OTG mode is disabled (EN_OTG=0) .
- Entry into shutdown, ultra-low power mode or system power reset by setting EN_OTG = 0 and then enter into shutdown, ultra-low power mode or system power reset as selected.

7.3.7 Integrated 12-bit ADC for Monitoring

BQ25638 provides an integrated 12-bit ADC for the host to monitor various system parameters. The ADC_RATE bit allows continuous conversion or one-shot behavior.

To enable the ADC, the EN_ADC bit must be set to ‘1’. The ADC is disabled by default (EN_ADC=0) to conserve power. The ADC is allowed to operate if either VBUS > $V_{POORSRC}$ or VBAT > V_{BAT_LOWV} is valid. If EN_ADC is set to ‘1’ before VBUS or VBAT reach their respective valid thresholds, then EN_ADC stays '0'. When the charger enters HIZ mode, the ADC is disabled, with EN_ADC set to '0'. The host can re-enable the ADC during HIZ mode by setting EN_ADC = 1. To minimize quiescent current during HIZ mode, the ADC should be disabled by setting EN_ADC=0.

At battery only condition, if the TS_ADC channel is enabled, the ADC will only operate when battery voltage is higher than 3.2V (the minimal value to turn on REGN), otherwise, the ADC will operate when the battery voltage is higher than V_{BAT_LOWV}.

The ADC_DONE_STAT, ADC_DONE_FLAG bits will be set when a conversion is complete in one-shot mode only. During continuous conversion mode, the ADC_DONE_STAT, ADC_DONE_FLAG bits have no meaning and will remain at 0. In one-shot mode, the EN_ADC bit will be set to 0 at the completion of the conversion, at the same time as the ADC_DONE_FLAG bit is set. In continuous mode, the EN_ADC bit remains at 1 until the user disables the ADC by setting it to 0.

The device offers an optional ADCIN input to monitor the value of an external signal up-to 1V.

7.3.8 Status Outputs ($\overline{INT}$, $\overline{PG}$, STAT)

7.3.8.1 $\overline{PG}$ Pin Power Good Indicator

The $\overline{PG}$ pin goes LOW to indicate a good input source when:

- V_{VBUS} is above V_{VBUS_UVLOZ}
- V_{VBUS} is above battery (not in sleep)
- V_{VBUS} is below V_{VBUS_OVP} threshold
- V_{VBUS} is above $V_{POORSRC}$ when $I_{POORSRC}$ current is applied (not a poor source)
- V_{VBUS} is above programmable PG_TH threshold

7.3.8.2 Charging Status Indicator (STAT)

BQ25638 indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. The STAT pin function can be disabled via the DIS_STAT bit. When disabled, the open-drain STAT pin is put into a high-impedance state, which will cause the pin to be pulled HIGH if there is an external pull-up. The pin can be left floating if DIS_STAT is set to 1 (disable.)

表 7-4. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Not charging, no fault detected. (Includes charging complete, EN_CHG = 0, $\overline{CE}$ high, EN_HIZ = 1, no adapter present, in OTG mode.)	HIGH
Charge suspend Boost Mode suspend	Blinking at 1 Hz

7.3.8.3 Interrupt to Host ($\overline{INT}$)

In many applications, the host does not continually poll the charger status registers. Instead, the $\overline{INT}$ pin may be used to notify the host of a status change with a 256-µs $\overline{INT}$ pulse. Upon receiving the interrupt pulse, the host may read the flag registers (Charger_Flag_X and FAULT_Flag_X) to determine the event that caused the interrupt, and for each flagged event, read the corresponding status registers (Charger_Status_X and FAULT_Status_X) to determine the current state. Once set to 1, the flag bits remain latched until they are read by the host, which clears them. The status bits, however, are updated whenever there is a change to status and always represent the current state of the system.

The $\overline{INT}$ events can be masked off to prevent $\overline{INT}$ pulses from being sent out when they occur, with the exception of the initial power-up interrupt. Interrupt events are masked by setting their mask bit in registers (Charger_Mask_X and FAULT_Mask_X.) Events always cause the corresponding flag bit to be set to 1, regardless of whether or not the interrupt pulse has been masked.

7.3.9 BATFET Control

The device has an integrated, bi-directionally blocking BATFET that can be turned off to remove leakage current from the battery to the system. The BATFET is controlled by the BATFET_CTRL register bits, and supports shutdown mode, ultra-low power mode and system power reset.

表 7-5. BATFET Control Modes

MODE	BATFET	I^2C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =1	EXIT
Normal	On	Active	N/A			N/A
Ultra-low power mode	Off	Active	Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY and enters ultra-low power mode.	Writing BATFET_CTRL = 10 has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters ultra-low power mode. Writing BATFET_CTRL = 00 before adapter is removed aborts ultra-low power mode.	Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters ultra-low power mode. Writing BATFET_CTRL = 00 before adapter is removed turns BATFET on and aborts ultra-low power mode.	$\overline{QON}$, I^2C, adapter plug-in

表 7-5. BATFET Control Modes (続き)

MODE	BATFET	I²C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS =1	EXIT
System reset	On to Off to On	Active	Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding $\overline{QON}$ low for t_{QON_RST} initiates immediate reset (BATFET_DLY is not applied.)	Writing BATFET_CTRL = 11 is ignored and BATFET_CTRL resets to 00. Holding $\overline{QON}$ low for t_{QON_RST} is ignored.	Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding $\overline{QON}$ low for t_{QON_RST} initiates immediate reset. Converter is placed in HIZ during system reset and exits HIZ when system reset completes.	N/A
Shutdown mode	Off	Off	Writing BATFET_CTRL = 01 turns off BATFET after BATFET_DLY and enters shutdown.	Writing BATFET_CTRL = 01 with adapter present is ignored, regardless of BATFET_CTRL_WVBUS setting, and BATFET_CTRL is reset to 00.		Adapter plug-in

7.3.9.1 Shutdown Mode

For the lowest battery leakage current, the host can shut down the device by setting the register bits BATFET_CTRL to 01. In this mode, the BATFET is turned off to prevent the battery from powering the system, the I²C is disabled and the charger is totally shut down. The charger can only be woken up by plugging in an adapter. When the adapter is plugged in, the device starts back up with all register settings in their POR default.

After the host sets BATFET_CTRL to 01, the BATFET turns off after waiting either 20 ms or 10s as configured by BATFET_DLY register bit. Shutdown mode can only be entered when $V_{VBUS} < V_{VBUS\_UVLO}$, regardless of the BATFET_CTRL_WVBUS setting, which has no effect on shutdown mode entry. If the host writes BATFET_CTRL = 01 with $V_{VBUS} > V_{VBUS\_UVLOZ}$, the request is ignored and the BATFET_CTRL bits are set back to 00.

If the host writes BATFET_CTRL to 01 while boost OTG, BQ25638 first exits from boost OTG by setting EN_OTG = 0 and then enters shutdown mode.

$\overline{QON}$ has no effect during shutdown mode. The internal pull-up on the $\overline{QON}$ pin is disabled during shutdown to prevent leakage through the pin.

7.3.9.2 Ultra-Low Power Mode

In ultra-low power mode, the BATFET is turned off to prevent the battery from powering the system. The host may place BQ25638 into ultra-low power mode by setting BATFET_CTRL = 10. ultra-low power mode has slightly higher quiescent current than shutdown mode, but $\overline{QON}$ or an I²C command may be used to exit from ultra-low power mode. The device is taken out of ultra-low power mode by either of these methods:

- Pulling the $\overline{QON}$ pin low for t_{SM_EXIT}
- Write BATFET_CTRL to 00 via I²C
- $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter plug-in)

When the charger exits from ultra-low power mode, the registers are reset to their POR values.

Ultra-low power mode is only entered when the adapter is not present. Setting BATFET_CTRL = 10 while $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter present) will either disable the BATFET or have no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

7.3.9.3 System Power Reset

The BATFET functions as a load switch between battery and system when the converter is not running. By changing the state of BATFET from on to off, systems connected to SYS can be power cycled. Any of the following conditions will initiate a system power reset:

- BATFET_CTRL_WVBUS = 1 and $\overline{QON}$ is pulled low for t_{QON_RST}
- BATFET_CTRL_WVBUS = 1 and BATFET_CTRL = 11
- BATFET_CTRL_WVBUS = 0 and VBUS < V_{VBUS_UVLO} simultaneously with $\overline{QON}$ pulled low for t_{QON_RST}
- BATFET_CTRL_WVBUS = 0 and VBUS < V_{VBUS_UVLO} and BATFET_CTRL = 11

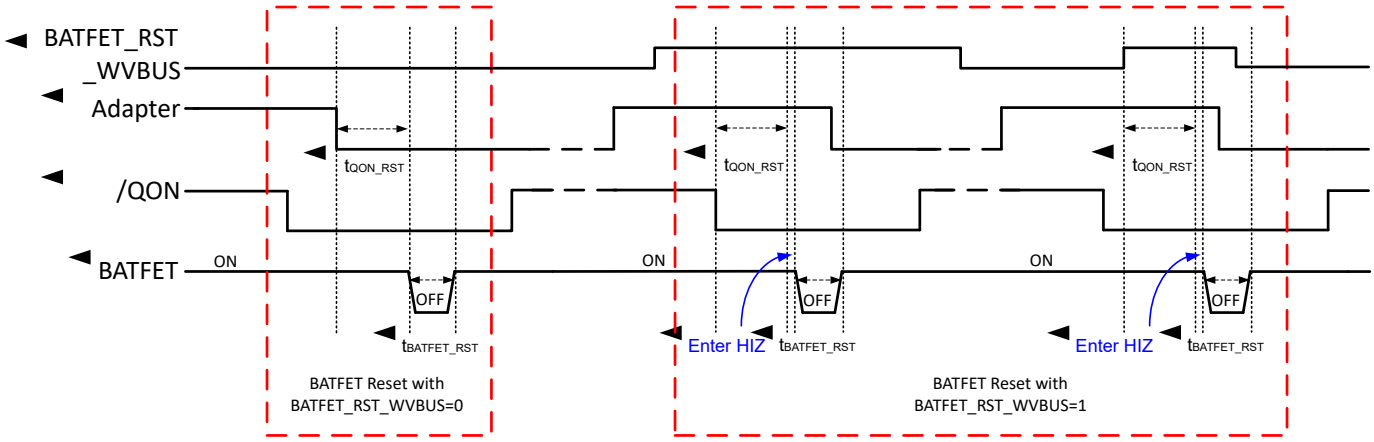


図 7-7. System Power Reset Timing

When BATFET_CTRL_WVBUS is set to 1, system power reset will proceed if either BATFET_CTRL is set to 11 or $\overline{QON}$ is pulled low for t_{QON_RST}, regardless of whether or not VBUS is present. There is a delay of t_{BATFET_DLY} before initiating the system power reset. If $\overline{QON}$ is pulled low, there is no delay after the t_{QON_RST} completes, regardless of BATFET_DLY setting.

The system power reset can be initiated from the battery only condition, from OTG mode or from the forward charging mode with adapter present. If the system power is reset when the charger is in boost OTG mode, the boost OTG mode will first be terminated by setting EN_OTG = 0.

7.3.10 Protections

7.3.10.1 Voltage and Current Monitoring in Battery Only and HIZ Modes

The device monitors a reduced set of voltages and currents when operating from battery without an adapter or when operating from battery in high impedance mode.

7.3.10.1.1 Battery Overcurrent Protection

BQ25638 has a two-level battery overcurrent protection. The I_{BAT_PK} threshold is set by IBAT_PK and provides a fast (100 µs) protection for the battery discharging. I_{BATFET_OCP} provides a slower (50 ms), fixed-threshold protection for the BATFET. If the battery discharge current becomes higher than either threshold for its deglitch time, the BAT_FAULT_STAT and BAT_FAULT_FLAG fault register bits are set to 1, and the BATFET enters hiccup mode with 100ms off-time and ~1% on-time. The BAT_FAULT_STAT will return to 0 once the BATFET is disabled for the hiccup mode. Once the BATFET is turned back on, the I_{BAT_PK} and I_{BATFET_OCP} thresholds are re-evaluated with their respective deglitch times. In boost OTG mode, if the battery discharging current is higher than either I_{BAT_PK} or I_{BATFET_OCP} for their respective deglitch times, the charger exits OTG mode by clearing the EN_OTG bit.

7.3.10.1.2 Battery Undervoltage Lockout

In battery-only mode, BQ25638 will disable the BATFET if V_{BAT} falls below V_{BAT_UVLO}, separating the system from the battery. I^2C is disabled as well. Upon exit from the undervoltage lockout condition when either V_{BAT}

rises above V_{BAT_UVLOZ} or V_{VBUS} rises above V_{VBUS_UVLOZ}, I^2C will be re-enabled and the registers are reset to their POR values.

7.3.10.2 Voltage and Current Monitoring in Forward Mode

The device closely monitors VBUS, SYS and BAT voltages, as well as VBUS, BAT and internal FET currents to ensure safe forward mode operation.

7.3.10.2.1 Input Overvoltage

If VBUS voltage rises above V_{VBUS_OVP}, the converter stops switching immediately to protect the internal power MOSFETs and I_{PMID_LOAD} discharge current is applied to bring down VBUS voltage. VBUS_FAULT_FLAG is set to 1 and the VBUS_FAULT_STAT bit transitions to 1. When VBUS falls back below V_{VBUS_OVPZ}, VBUS_OVP_STAT will transition to 0 and the converter will resume switching.

7.3.10.2.2 System Overvoltage Protection (SYSOVP)

When VSYS rises above V_{SYS_OVP} in forward converter operation, the converter stops switching immediately to limit voltage overshoot and applies I_{SYS_LOAD} to pull down the system voltage. VSYS_FAULT_FLAG is set to 1 and the VSYS_FAULT_STAT transitions to 1. Once VSYS drops below V_{SYS_OVP}, the converter resumes switching, the 30 mA discharge current is removed and VSYS_FAULT_STAT transitions to 0.

7.3.10.2.3 Forward Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In forward mode, if the current through Q2 exceeds I_{HSFET_OCP}, the converter will immediately turn off the high-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

7.3.10.2.4 System Short

When the SYS voltage falls below V_{SYS_SHORT}, the charger immediately enters PFM operation to limit the output current to approximately 0.5A or less. SYS_FAULT_STAT and SYS_FAULT_FLAG bits are set to 1. If V_{SYS} rises above V_{SYS_SHORTZ}, the converter exits forced PFM mode, and the SYS_FAULT_STAT bit is set to 0.

7.3.10.2.5 Battery Overvoltage Protection (BATOVP)

When V_{BAT} transitions above V_{BAT_OVP}, BQ25638 immediately disables charging by disabling the BATFET and applies I_{BAT_LOAD} current source to discharge excess BAT voltage. BAT_FAULT_FLAG is set to 1 and BAT_FAULT_STAT transitions to 1. Once V_{BAT} falls below V_{BAT_OVPZ}, charging resumes and BAT_FAULT_STAT transitions back to 0.

7.3.10.2.6 Sleep and Poor Source Comparators

The sleep comparator is used to suspend the converter if the adapter voltage is insufficient to maintain buck converter operation while charging the battery. If V_{VBUS} falls below V_{BAT} + V_{SLEEP} the converter stops switching, the $\overline{PG}$ pin transitions high. If V_{VBUS} rises back above V_{BAT} + V_{SLEEPZ}, the converter restarts, the $\overline{PG}$ pin transitions low.

If V_{VBUS} falls below $V_{POORSRC}$, the converter stops switching and the $\overline{PG}$ pin transitions high (if not already suspended and high due to the sleep comparator), and the VBUS_STAT transitions to 000 and the device transitions to battery-only mode. If V_{VBUS} rises above $V_{POORSRC}$, it is a new adapter attach, and poor source qualification will be run. VBUS_STAT and the $\overline{PG}$ pin state will be determined by the adapter attach sequence as outlined in セクション 7.3.3.

7.3.10.3 Voltage and Current Monitoring in Reverse Mode

The device closely monitors VBUS, SYS and BAT voltages, as well as VBUS, BAT and FET currents to ensure safe reverse mode operation.

7.3.10.3.1 Boost Mode Overvoltage Protection

During OTG operation, BQ25638 uses two comparators to sense output overvoltage at VBUS and PMID. If either VBUS or PMID voltage rises above their OVP threshholds, the converter stops switching and attempts to discharge the voltage.

If the OVP condition persists on VBUS or PMID, OTG_FAULT_FLAG is set to 1, OTG_FAULT_STAT transitions to 1 and the converter powers down into a fault condition and the device exits from OTG mode by setting EN_OTG = 0.

7.3.10.3.2 Boost Mode Duty Cycle Protection

After an initial startup blanking period, BQ25638 monitors the PMID voltage during boost OTG mode to ensure that PMID voltage remains sufficiently above VSYS to maintain the minimum duty cycle. If V_{PMID} falls below V_{BOOST_DUTY} (105% V_{SYS} typical), the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

7.3.10.3.3 Boost Mode PMID Undervoltage Protection

During boost OTG mode, BQ25638 converter monitors PMID for undervoltage. If the PMID voltage falls below V_{OTG_UVP}, the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

7.3.10.3.4 Boost Mode Battery Undervoltage

If V_{BAT} falls below V_{BAT_OTGZ} during OTG mode, the charger exits OTG mode by setting EN_OTG = 0, and BAT_FAULT_STAT and BAT_FAULT_FLAG are set to 1. Setting EN_OTG = 1 while $V_{BAT} < V_{BAT\_OTG}$ will not enter OTG and the EN_OTG bit will be cleared to 0. When the battery is charged above V_{BAT_OTG}, OTG mode may be entered by setting EN_OTG = 1.

7.3.10.3.5 Boost Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In OTG mode, if the current through Q3 exceeds I_{LSFET_OCP}, the converter will immediately turn off the low-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

7.3.10.3.6 Boost Mode SYS Short

If VSYS falls below VSYS_SHORT in boost OTG mode, BQ25638 immediately stops the boost converter, enters hiccup mode, and sets SYS_FAULT_FLAG to 1.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

7.3.10.4 Thermal Regulation and Thermal Shutdown

7.3.10.4.1 Thermal Protection in Buck Mode

The device monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in buck mode. When the internal junction temperature exceeds the T_{REG} thermal regulation limit (TREG register configuration), the device lowers the charging current. During thermal regulation, the safety timer runs at half the clock rate, and the TREG_FLAG and TREG_STAT bits are set to 1. Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET and converter are re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

7.3.10.4.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT}, the boost mode is disabled by setting EN_OTG bit low and BATFET

is turned off, and TSHUT_FLAG is set to 1. When IC junction temperature is below T_{SHUT} - T_{SHUT_HYS}, the BATFET is enabled automatically to allow system to restore and the host can re-enable EN_OTG bit to recover.

7.3.10.4.3 Thermal Protection in Battery-only Mode

The device monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in battery-only mode. The device has thermal shutdown to turn off the BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET is re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

7.4 Device Functional Modes

7.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck converter continues to operate to supply system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog expires, the device returns to default mode. The ICHG value is divided in half when the watchdog timer expires, and a number of other fields are reset to their POR default values as shown in the notes column of the register tables in . The watchdog timer will be reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK).

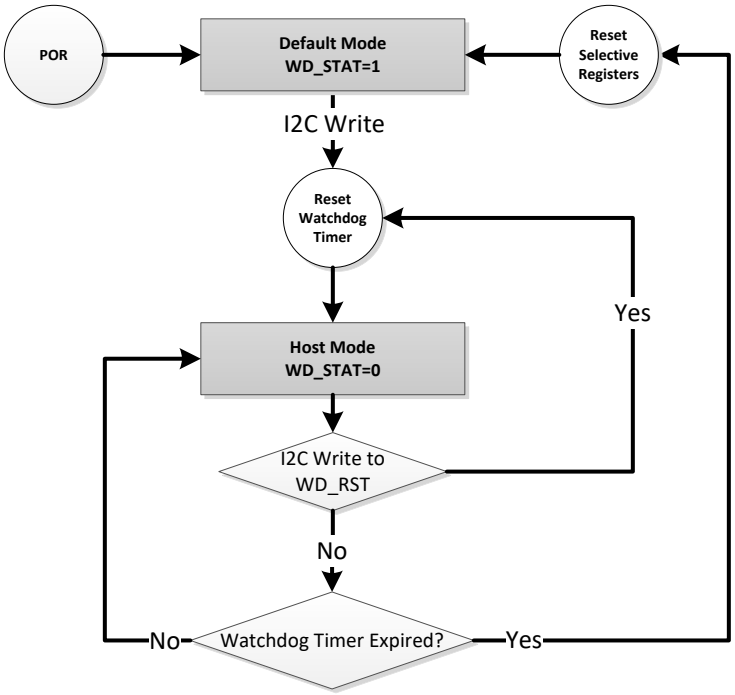


図 7-8. Watchdog Timer Flow Chart

7.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit will go back from 1 to 0 automatically.

7.5 Programming

7.5.1 Serial Interface

BQ25638 uses I^{2}C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^{2}C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL).

The device has 7-bit I^{2}C address 0x6B, receiving control inputs from a host device such as a micro-controller or digital signal processor through register addresses defined in the Register Map. The host device initiates all transfers and the charger responds. Register reads outside of these adresses return 0xFF. When the bus is free, both SDA and SCL lines are HIGH.

The I^{2}C interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s) and fast mode plus (up to 1 Mbits/s.) These lines are pulled up to a reference voltage via pull-up resistor. The device I^{2}C detection thresholds support a communication reference voltage between 1.2V - 5V.

Due to the ultra low I_Q when the device operates in low power mode, it is necessary to use an increased timing between I^{2}C read commands on the I^{2}C bus when operating in fast mode or fast mode plus. The recommended minimum t_{buf} (bus free time between a STOP and START condition) depends on the I^{2}C mode:

- Standard mode (100 kbits/s):
  - No additional requirements
- Fast mode (400 kbits/s):
  - Increase I^{2}C t_{buf} to at least 80 µs
  - If using repeated start commands, ensure I^{2}C tsu:STA is at least 80 µs
- Fast mode plus (1 Mbits/s):
  - Increase I^{2}C t_{buf} to at least 120 µs
  - If using repeated start commands, ensure I^{2}C tsu:STA is at least 120 µs

7.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

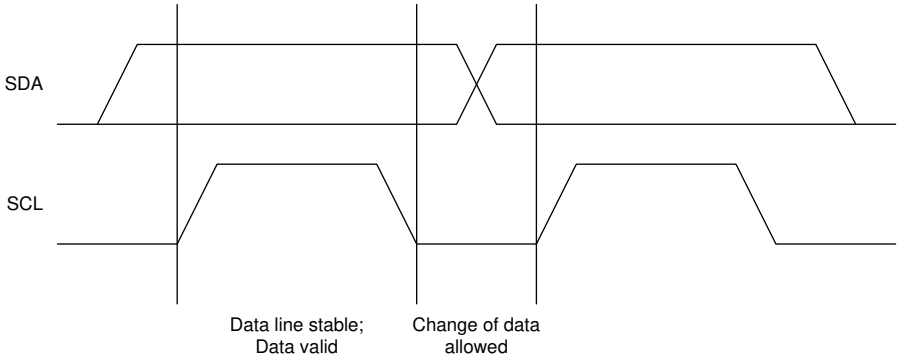


図 7-9. Bit Transfer on the I^{2}C Bus

7.5.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

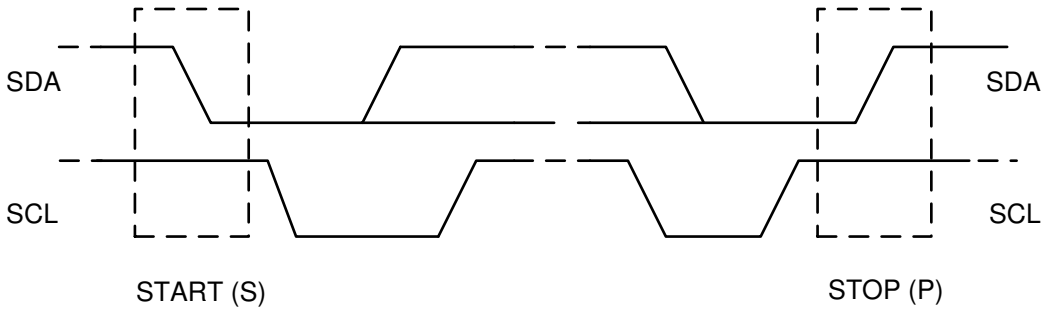


図 7-10. START and STOP Conditions on the I²C Bus

7.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

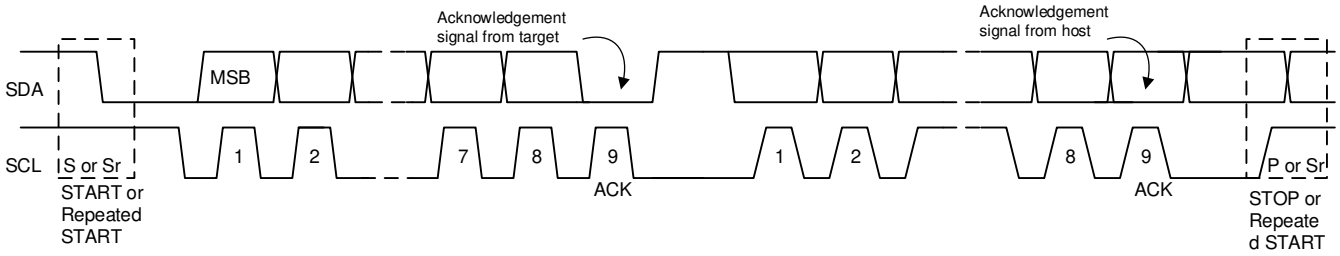


図 7-11. Data Transfer on the I²C Bus

7.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the host to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The transmitter releases the SDA line during the acknowledge clock pulse so the host can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.5.1.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 011' (0x6B). The address bit arrangement is shown below.

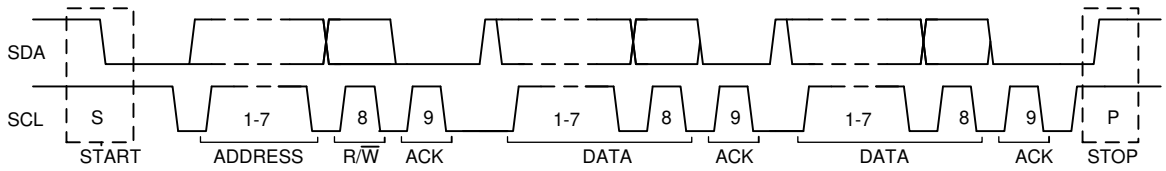


図 7-12. Complete Data Transfer on the I²C Bus

7.5.1.6 Single Write and Read

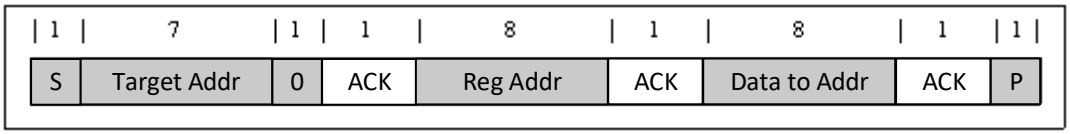


図 7-13. Single Write

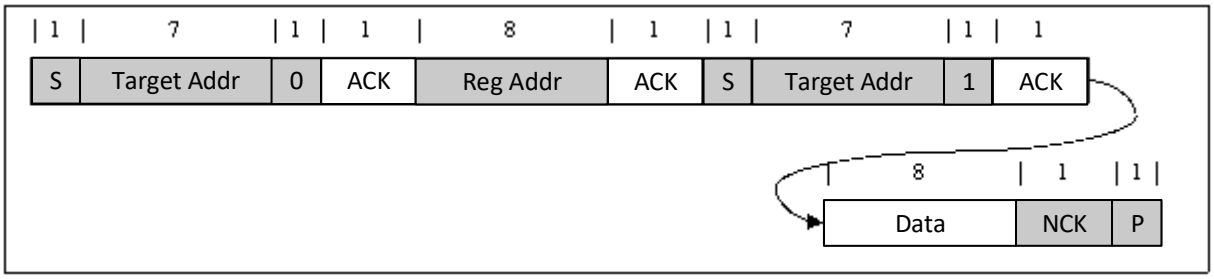


図 7-14. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

7.5.1.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map may be read in a single operation with a 39-byte read that starts at register address 0x01.

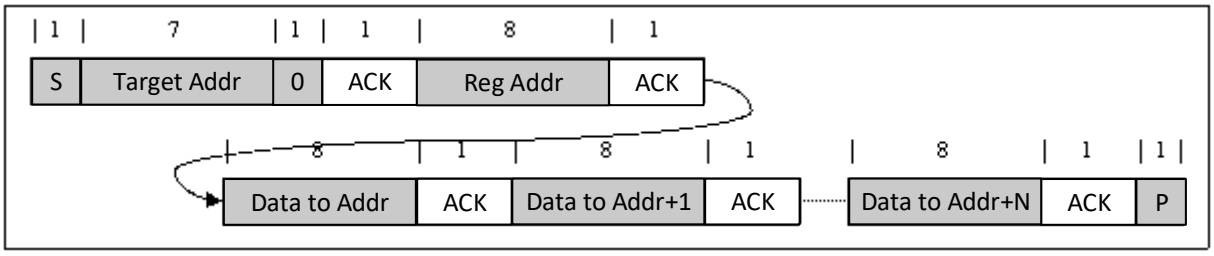


図 7-15. Multi-Write

図 7-16. Multi-Read

7.6 BQ25638 Registers

表 7-6 lists the memory-mapped registers for the BQ25638 registers. All register offset addresses not listed in 表 7-6 should be considered as reserved locations and the register contents should not be modified.

表 7-6. BQ25638 Registers

Address	Acronym	Register Name	Section
0x2	REG0x02_Charge_Current_Limit	Charge Current Limit	Go
0x4	REG0x04_Charge_Voltage_Limit	Charge Voltage Limit	Go
0x6	REG0x06_Input_Current_Limit	Input Current Limit	Go
0x8	REG0x08_Input_Voltage_Limit	Input Voltage Limit	Go
0xA	REG0x0A_IOTG_regulation	IOTG regulation	Go
0xC	REG0x0C_VOTG_regulation	VOTG regulation	Go
0xE	REG0x0E_Minimal_System_Voltage	Minimal System Voltage	Go
0x10	REG0x10_Precharge_Control	Precharge Control	Go
0x12	REG0x12_Termination_Control	Termination Control	Go
0x14	REG0x14_Charge_Timer_Control	Charge Timer Control	Go
0x15	REG0x15_Charger_Control_0	Charger Control 0	Go
0x16	REG0x16_Charger_Control_1	Charger Control 1	Go
0x17	REG0x17_Charger_Control_2	Charger Control 2	Go
0x18	REG0x18_Charger_Control_3	Charger Control 3	Go
0x19	REG0x19_Charger_Control_4	Charger Control 4	Go
0x1A	REG0x1A_Charger_Control_5	Charger Control 5	Go
0x1C	REG0x1C_NTC_Control_0	NTC Control 0	Go
0x1D	REG0x1D_NTC_Control_1	NTC Control 1	Go
0x1E	REG0x1E_NTC_Control_2	NTC Control 2	Go
0x1F	REG0x1F_NTC_Control_3	NTC Control 3	Go
0x20	REG0x20_Charger_Status_0	Charger Status 0	Go
0x21	REG0x21_Charger_Status_1	Charger Status 1	Go
0x22	REG0x22_FAULT_Status	FAULT Status	Go
0x23	REG0x23_Charger_Flag_0	Charger Flag 0	Go
0x24	REG0x24_Charger_Flag_1	Charger Flag 1	Go
0x25	REG0x25_FAULT_Flag	FAULT Flag	Go
0x26	REG0x26_Charger_Mask_0	Charger Mask 0	Go
0x27	REG0x27_Charger_Mask_1	Charger Mask 1	Go
0x28	REG0x28_FAULT_Mask	FAULT Mask	Go
0x29	REG0x29_ICO_Current_Limit	ICO Current Limit	Go
0x2B	REG0x2B_ADC_Control	ADC Control	Go
0x2C	REG0x2C_ADC_Channel_Disable	ADC Channel Disable	Go
0x2D	REG0x2D_IBUS_ADC	IBUS ADC	Go
0x2F	REG0x2F_IBAT_ADC	IBAT ADC	Go
0x31	REG0x31_VBUS_ADC	VBUS ADC	Go
0x33	REG0x33_VPMID_ADC	VPMID ADC	Go
0x35	REG0x35_VBAT_ADC	VBAT ADC	Go
0x37	REG0x37_VSYS_ADC	VSYS ADC	Go
0x39	REG0x39_TS_ADC	TS ADC	Go
0x3B	REG0x3B_TDIE_ADC	TDIE ADC	Go
0x3D	REG0x3D_ADCIN_ADC	ADCIN ADC	Go
0x3F	REG0x3F_Part_Information	Part Information	Go
0x80	REG0x80_Virtual_Control_0	Virtual Control 0	Go

表 7-6. BQ25638 Registers (続き)

Address	Acronym	Register Name	Section
0x81	REG0x81_Virtual_Control_1	Virtual Control 1	Go

Complex bit access types are encoded to fit into small table cells. 表 7-7 shows the codes that are used for access types in this section.

表 7-7. BQ25638 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 REG0x02_Charge_Current_Limit Register (Address = 0x2) [Reset = 0x0640]

REG0x02_Charge_Current_Limit is shown in 図 7-17 and described in 表 7-8.

Return to the Summary Table.

図 7-17. REG0x02_Charge_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				ICHG			
R-0x0				R/W-0x19			
7	6	5	4	3	2	1	0
ICHG				RESERVED			
R/W-0x19				R-0x0			

表 7-8. REG0x02_Charge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved
11:6	ICHG	R/W	0x19	This 16-bit register follows the little-endian convention. Watchdog Timer expiration sets ICHG to 1/2 its previous value (rounded down) Reset by: REG_RESET WATCHDOG	Charge Current Regulation Limit: NOTE: When Q4_FULLON=1, this register has a minimum value of 320mA POR: 2000mA (19h) Range: 80mA-5040mA (1h-3Fh) Clamped Low Bit Step: 80mA
5:0	RESERVED	R	0x0		Reserved

7.6.2 REG0x04_Charge_Voltage_Limit Register (Address = 0x4) [Reset = 0x0D20]

REG0x04_Charge_Voltage_Limit is shown in 図 7-18 and described in 表 7-9.

Return to the Summary Table.

図 7-18. REG0x04_Charge_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED				VREG			

図 7-18. REG0x04_Charge_Voltage_Limit Register (続き)

R-0x0						R/W-0x1A4	
7	6	5	4	3	2	1	0
VREG						RESERVED	
R/W-0x1A4						R-0x0	

表 7-9. REG0x04_Charge_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved
11:3	VREG	R/W	0x1A4	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Battery Voltage Regulation Limit: POR: 4200mV (1A4h) Range: 3500mV-4800mV (15Eh-1E0h) Clamped Low Clamped High Bit Step: 10mV
2:0	RESERVED	R	0x0		Reserved

7.6.3 REG0x06_Input_Current_Limit Register (Address = 0x6) [Reset = 0x0A00]

REG0x06_Input_Current_Limit is shown in 図 7-19 and described in 表 7-10.

Return to the Summary Table.

図 7-19. REG0x06_Input_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				IINDPM			
R-0x0				R/W-0xA0			
7	6	5	4	3	2	1	0
IINDPM				RESERVED			
R/W-0xA0				R-0x0			

表 7-10. REG0x06_Input_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved
11:4	IINDPM	R/W	0xA0	This 16-bit register follows the little-endian convention Reset by: REG_RESET Adapter Unplug	Input Current Regulation Limit: POR: 3200mA (A0h) Range: 100mA-3200mA (5h-A0h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0x0		Reserved

7.6.4 REG0x08_Input_Voltage_Limit Register (Address = 0x8) [Reset = 0x0DC0]

REG0x08_Input_Voltage_Limit is shown in 図 7-20 and described in 表 7-11.

Return to the Summary Table.

図 7-20. REG0x08_Input_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED		VINDPM					
R-0x0		R/W-0x6E					
7	6	5	4	3	2	1	0
VINDPM			RESERVED				
R/W-0x6E			R-0x0				

図 7-20. REG0x08_Input_Voltage_Limit Register (続き)

表 7-11. REG0x08_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0x0		Reserved
13:5	VINDPM	R/W	0x6E	This 16-bit register follows the little-endian convention	Absolute Input Voltage Regulation Limit: POR: 4400mV (6Eh) Range: 3800mV-16800mV (5Fh-1A4h) Clamped Low Clamped High Bit Step: 40mV
4:0	RESERVED	R	0x0		Reserved

7.6.5 REG0x0A_IOTG_regulation Register (Address = 0xA) [Reset = 0x04B0]

REG0x0A_IOTG_regulation is shown in 図 7-21 and described in 表 7-12.

Return to the Summary Table.

図 7-21. REG0x0A_IOTG_regulation Register

15	14	13	12	11	10	9	8
RESERVED				IOTG			
R-0x0				R/W-0x4B			
7	6	5	4	3	2	1	0
IOTG				RESERVED			
R/W-0x4B				R-0x0			

表 7-12. REG0x0A_IOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved
11:4	IOTG	R/W	0x4B	This 16-bit register follows the little-endian convention Reset by: REG_RESET WATCHDOG	OTG mode current regulation limit: POR: 1500mA (4Bh) Range: 100mA-3200mA (5h-A0h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0x0		Reserved

7.6.6 REG0x0C_VOTG_regulation Register (Address = 0xC) [Reset = 0x1000]

REG0x0C_VOTG_regulation is shown in 図 7-22 and described in 表 7-13.

Return to the Summary Table.

図 7-22. REG0x0C_VOTG_regulation Register

15	14	13	12	11	10	9	8
RESERVED			VOTG				
R-0x0			R/W-0x40				
7	6	5	4	3	2	1	0
VOTG		RESERVED					
R/W-0x40		R-0x0					

表 7-13. REG0x0C_VOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:13	RESERVED	R	0x0		Reserved
12:6	VOTG	R/W	0x40	This 16-bit register follows the little-endian convention Reset by: REG_RESET	OTG mode regulation voltage: POR: 5120mV (40h) Range: 3840mV-9600mV (30h-78h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0x0		Reserved

7.6.7 REG0x0E_Minimal_System_Voltage Register (Address = 0xE) [Reset = 0x0B00]

REG0x0E_Minimal_System_Voltage is shown in 図 7-23 and described in 表 7-14.

Return to the Summary Table.

図 7-23. REG0x0E_Minimal_System_Voltage Register

15	14	13	12	11	10	9	8
RESERVED				VSYSMIN			
R-0x0				R/W-0x2C			
7	6	5	4	3	2	1	0
VSYSMIN				RESERVED			
R/W-0x2C				R-0x0			

表 7-14. REG0x0E_Minimal_System_Voltage Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved
11:6	VSYSMIN	R/W	0x2C	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Minimal System Voltage: POR: 3520mV (2Ch) Range: 2560mV-3840mV (20h-30h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0x0		Reserved

7.6.8 REG0x10_Precharge_Control Register (Address = 0x10) [Reset = 0x00A0]

REG0x10_Precharge_Control is shown in 図 7-24 and described in 表 7-15.

Return to the Summary Table.

図 7-24. REG0x10_Precharge_Control Register

15	14	13	12	11	10	9	8
RESERVED						IPRECHG	
R-0x0						R/W-0xA	
7	6	5	4	3	2	1	0
IPRECHG				RESERVED			
R/W-0xA				R-0x0			

表 7-15. REG0x10_Precharge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:10	RESERVED	R	0x0		Reserved

表 7-15. REG0x10_Precharge_Control Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
9:4	IPRECHG	R/W	0xA	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Pre-charge current regulation limit: NOTE: When Q4_FULLON=1, this register has a minimum value of 320mA POR: 200mA (Ah) Range: 40mA-1000mA (2h-32h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0x0		Reserved

7.6.9 REG0x12_Termination_Control Register (Address = 0x12) [Reset = 0x00A0]

REG0x12_Termination_Control is shown in 図 7-25 and described in 表 7-16.

Return to the Summary Table.

図 7-25. REG0x12_Termination_Control Register

15	14	13	12	11	10	9	8
RESERVED						ITERM	
R-0x0						R/W-0x14	
7	6	5	4	3	2	1	0
ITERM						RESERVED	
R/W-0x14						R-0x0	

表 7-16. REG0x12_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:10	RESERVED	R	0x0		Reserved
9:3	ITERM	R/W	0x14	Reset by: REG_RESET	Termination Current Threshold: NOTE: When Q4_FULLON=1, this register has a minimum value of 240mA POR: 200mA (14h) Range: 30mA-1000mA (3h-64h) Clamped Low Clamped High Bit Step: 10mA
2:0	RESERVED	R	0x0		Reserved

7.6.10 REG0x14_Charge_Timer_Control Register (Address = 0x14) [Reset = 0x0C]

REG0x14_Charge_Timer_Control is shown in 図 7-26 and described in 表 7-17.

Return to the Summary Table.

図 7-26. REG0x14_Charge_Timer_Control Register

7	6	5	4	3	2	1	0
DIS_STAT	RESERVED	RESERVED	RESERVED	EN_TMR2X	EN_SAFETY_TMRS	PRECHG_TMR	CHG_TMR
R/W-0x0	R-0x0	R-0x0	R-0x0	R/W-0x1	R/W-0x1	R/W-0x0	R/W-0x0

表 7-17. REG0x14_Charge_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DIS_STAT	R/W	0x0	Reset by: REG_RESET	Disable the /STAT pin output 0b = Enable (Default) 1b = Disable

表 7-17. REG0x14_Charge_Timer_Control Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
6	RESERVED	R	0x0		Reserved
5	RESERVED	R	0x0		Reserved
4	RESERVED	R	0x0		Reserved
3	EN_TMR2X	R/W	0x1	Reset by: REG_RESET	2X charging timer control 0b = Trickle charge, pre-charge and fast charge timer not slowed by 2X during input DPM or thermal regulation. 1b = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default)
2	EN_SAFETY_TMRS	R/W	0x1	Reset by: REG_RESET WATCHDOG	Enable fast charge, pre-charge and trickle charge timers 0b = Disable 1b = Enable (default)
1	PRECHG_TMR	R/W	0x0	Reset by: REG_RESET	Pre-charge safety timer setting 0b = 2.3 hrs (default) 1b = 0.6 hrs
0	CHG_TMR	R/W	0x0	Reset by: REG_RESET	Fast charge safety timer setting 0b = 14 hrs (default) 1b = 27 hrs

7.6.11 REG0x15_Charger_Control_0 Register (Address = 0x15) [Reset = 0x26]

REG0x15_Charger_Control_0 is shown in 図 7-27 and described in 表 7-18.

Return to the Summary Table.

図 7-27. REG0x15_Charger_Control_0 Register

7	6	5	4	3	2	1	0
Q1_FULLON	Q4_FULLON	ITRICKLE	TOPOFF_TMR		EN_TERM	VINDPM_BAT_TRACK	VRECHG
R/W-0x0	R/W-0x0	R/W-0x1	R/W-0x0		R/W-0x1	R/W-0x1	R/W-0x0

表 7-18. REG0x15_Charger_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	Q1_FULLON	R/W	0x0		Forces RBFET (Q1) into low resistance state (15 mΩ) , regardless of IINDPM setting. 0b = RBFET RDSON determined by IINDPM setting 1b = RBFET RDSON is always 15 mOhm
6	Q4_FULLON	R/W	0x0		Forces BATFET (Q4) into low resistance state (7 mΩ), regardless of ICHG setting. 0b = BATFET RDSON determined by charge current 1b = BATFET RDSON is always 7 mOhm
5	ITRICKLE	R/W	0x1	When Q4_FULLON, this setting is forced to 80mA Reset by: REG_RESET	Trickle charging current setting: 0b = 20mA 1b = 80mA
4:3	TOPOFF_TMR	R/W	0x0	Reset by: REG_RESET	Top-off timer control: 00b = Disabled (default) 01b = 17.5 mins 10b = 35 mins 11b = 52 mins

表 7-18. REG0x15_Charger_Control_0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
2	EN_TERM	R/W	0x1	Reset by: REG_RESET WATCHDOG	Enable termination 0b = Disable 1b = Enable (default)
1	VINDPM_BAT_TRACK	R/W	0x1	Reset by: REG_RESET	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of the VINDPM register value and VBAT + VINDPM_BAT_TRACK. 0b = Disable function (VINDPM set by register) 1b = VBAT + 350 mV (default)
0	VRECHG	R/W	0x0	Reset by: REG_RESET	Battery Recharge Threshold Offset (Below VREG) 0b = 100mV (default) 1b = 200mV

7.6.12 REG0x16_Charger_Control_1 Register (Address = 0x16) [Reset = 0xA1]

REG0x16_Charger_Control_1 is shown in 図 7-28 and described in 表 7-19.

Return to the Summary Table.

図 7-28. REG0x16_Charger_Control_1 Register

7	6	5	4	3	2	1	0
EN_AUTO_IBAT_DSCHG	FORCE_IBAT_DSCHG	EN_CHG	EN_HIZ	FORCE_PMID_DSCHG	WD_RST	WATCHDOG	
R/W-0x1	R/W-0x0	R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1	

表 7-19. REG0x16_Charger_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_AUTO_IBAT_DSCHG	R/W	0x1	Reset by: REG_RESET	Enable the auto battery discharging during the battery OVP fault 0b = The charger will NOT apply a discharging current on BAT during battery OVP triggered 1b = The charger will apply a discharging current on BAT during battery OVP triggered (default)
6	FORCE_IBAT_DSCHG	R/W	0x0	Reset by: REG_RESET WATCHDOG	Enable BAT pull down current source 0b = Disable 1b = Enable
5	EN_CHG	R/W	0x1	Reset by: REG_RESET WATCHDOG	Charger enable configuration 0b = Charge Disable 1b = Charge Enable (default)
4	EN_HIZ	R/W	0x0	Reset by: REG_RESET WATCHDOG Adapter Plug In	Enable HIZ mode. This bit will be reset to 0, when the adapter is plugged in at VBUS. 0b = Disable (default) 1b = Enable
3	FORCE_PMID_DSCHG	R/W	0x0	Reset by: REG_RESET WATCHDOG	Enable PMID pull down current source (~30mA) 0b = Disable 1b = Enable
2	WD_RST	R/W	0x0	Reset by: REG_RESET	I2C watch dog timer reset 0b = Normal (default) 1b = Reset (this bit goes back to 0 after timer reset)

表 7-19. REG0x16_Charger_Control_1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
1:0	WATCHDOG	R/W	0x1	Reset by: REG_RESET	Watchdog timer setting 00b = Disable 01b = 40s (default) 10b = 80s 11b = 160s

7.6.13 REG0x17_Charger_Control_2 Register (Address = 0x17) [Reset = 0x4F]

REG0x17_Charger_Control_2 is shown in 図 7-29 and described in 表 7-20.

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図 7-29. REG0x17_Charger_Control_2 Register

7	6	5	4	3	2	1	0
REG_RST	TREG	EN_DITHER		SET_CONV_STRN		SET_BATFET_STRN	VBUS_OVP
R/W-0x0	R/W-0x1	R/W-0x0		R/W-0x3		R/W-0x1	R/W-0x1

表 7-20. REG0x17_Charger_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0x0		Reset registers to default values and reset timer Value resets to 0 after reset completes. 0b = Not reset (default) 1b = Reset
6	TREG	R/W	0x1	Reset by: REG_RESET	Thermal regulation thresholds. 0b = 60°C 1b = 120°C
5:4	EN_DITHER	R/W	0x0	Reset by: REG_RESET	Frequency Dither configuration: 00b = Disable 01b = 1X 10b = 2X 11b = 3X
3:2	SET_CONV_STRN	R/W	0x3	Reset by: REG_RESET	Adjust the drive strength of the converter to adjust efficiency versus EMI. 00b = reduce drive strength three steps 01b = reduce drive strength two steps 10b = reduce drive strength one step 11b = maximum drive strength (default)
1	SET_BATFET_STRN	R/W	0x1	Reset by: REG_RESET	Adjust the drive strength of the BATFET to control speed of turn on and turn off. 0b = reduce drive strength 1b = maximum drive strength (default)
0	VBUS_OVP	R/W	0x1	Reset by: REG_RESET	Set VBUS overvoltage protection threshold 0b = 6.3V 1b = 18.5V

7.6.14 REG0x18_Charger_Control_3 Register (Address = 0x18) [Reset = 0x04]

REG0x18_Charger_Control_3 is shown in 図 7-30 and described in 表 7-21.

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図 7-30. REG0x18_Charger_Control_3 Register

7	6	5	4	3	2	1	0
RESERVED	EN_OTG	DIS_PFM_OTG	DIS_PFM_FWD	BATFET_CTRL_WVBUS	BATFET_DLY	BATFET_CTRL	

図 7-30. REG0x18_Charger_Control_3 Register (続き)

R-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1	R/W-0x0

表 7-21. REG0x18_Charger_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6	EN_OTG	R/W	0x0	Reset by: REG_RESET WATCHDOG	OTG mode control 0b = OTG Disable (default) 1b = OTG Enable
5	DIS_PFM_OTG	R/W	0x0	Reset by: REG_RESET	Disable PFM in OTG boost mode 0b = Enable (Default) 1b = Disable
4	DIS_PFM_FWD	R/W	0x0	Reset by: REG_RESET	Disable PFM in forward buck mode 0b = Enable (Default) 1b = Disable
3	BATFET_CTRL_WVBUS	R/W	0x0		Start system power reset with or without adapter present. 0b = Start system power reset after adapter is removed from VBUS. (default) 1b = Start system power reset whether or not adapter is present on VBUS.
2	BATFET_DLY	R/W	0x1	Reset by: REG_RESET	Delay time added to the taking action in bits [1:0] of the BATFET_CTRL 0b = Add 24ms delay 1b = Add 12s delay
1:0	BATFET_CTRL	R/W	0x0	Reset by: REG_RESET	BATFET control The control logic of the BATFET to force the device enter different modes. 00b = Idle 01b = Shutdown Mode 10b = Ultra-Low Power Mode 11b = System Power Reset

7.6.15 REG0x19_Charger_Control_4 Register (Address = 0x19) [Reset = 0x85]

REG0x19_Charger_Control_4 is shown in 図 7-31 and described in 表 7-22.

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図 7-31. REG0x19_Charger_Control_4 Register

7	6	5	4	3	2	1	0
IBAT_PK		VBAT_UVLO	VBAT_OTG_MIN	RESERVED	EN_EXT_ILIM	FORCE_ICO	EN_ICO
R/W-0x2		R/W-0x0	R/W-0x0	R-0x0	R/W-0x1	R/W-0x0	R/W-0x1

表 7-22. REG0x19_Charger_Control_4 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	IBAT_PK	R/W	0x2	Reset by: REG_RESET	Battery discharging over current protection threshold setting 00b = 3A 01b = 6A 10b = 9A 11b = Reserved
5	VBAT_UVLO	R/W	0x0	Reset by: REG_RESET	Select the VBAT UVLO falling thresholds 0b = 2.2V (default) 1b = 1.8V

表 7-22. REG0x19_Charger_Control_4 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
4	VBAT_OTG_MIN	R/W	0x0	Reset by: REG_RESET	Select the minimal battery voltage to start the OTG mode 0b = 3V rising / 2.8 falling (default) 1b = 2.4V rising / 2.2 falling
3	RESERVED	R	0x0		Reserved
2	EN_EXT_ILIM	R/W	0x1	Reset by: REG_RESET WATCHDOG	Enable External ILIM pin input current regulation 0b = Disable 1b = Enable
1	FORCE_ICO	R/W	0x0	Reset by: REG_RESET WATCHDOG	Force Start Input Current Optimizer (ICO): Note: This bit can only be set and always returns to 0 after ICO starts. This bit is only valid when EN_ICO = 1 0b = Do not force ICO 1b = Force ICO start
0	EN_ICO	R/W	0x1	Reset by: REG_RESET	Input Current Optimization (ICO) Algorithm Control: 0b = Disable ICO 1b = Enable ICO

7.6.16 REG0x1A_Charger_Control_5 Register (Address = 0x1A) [Reset = 0x00]

REG0x1A_Charger_Control_5 is shown in 図 7-32 and described in 表 7-23.

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図 7-32. REG0x1A_Charger_Control_5 Register

7	6	5	4	3	2	1	0
PG_TH			TQON_RST	TSM_EXIT	FORCE_ISYS_DSCHG	BATLOWV	
R/W-0x0			R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	

表 7-23. REG0x1A_Charger_Control_5 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:5	PG_TH	R/W	0x0	Reset by: REG_RESET	Programmable PG indicator falling threshold: 000b = 3.7V 001b = 7.4V 010b = 8V 011b = 10.4V 100b = 11V 101b = 13.4V 110b = 14V 111b = Reserved
4	TQON_RST	R/W	0x0		System Reset (tQON_RST) control: 0b = 11s 1b = 21s
3	TSM_EXIT	R/W	0x0		Ultra-Low Power Mode exit (tSM_EXIT) control: 0b = 700ms 1b = 10.5s
2	FORCE_ISYS_DSCHG	R/W	0x0	Reset by: REG_RESET WATCHDOG	Enable SYS pull down current source 0b = Disable 1b = Enable

表 7-23. REG0x1A_Charger_Control_5 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
1:0	BATLOWV	R/W	0x0		Battery precharge to fast-charge threshold: 00b = 3.0V 01b = 2.8V 10b = 2.7V 11b = 2.5V

7.6.17 REG0x1C_NTC_Control_0 Register (Address = 0x1C) [Reset = 0x0F]

REG0x1C_NTC_Control_0 is shown in 図 7-33 and described in 表 7-24.

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図 7-33. REG0x1C_NTC_Control_0 Register

7	6	5	4	3	2	1	0
TS_IGNORE	CHG_RATE		TS_TH_OTG_HOT		TS_TH_OTG_COLD	TS_TH1	TS_TH6
R/W-0x0	R/W-0x0		R/W-0x1		R/W-0x1	R/W-0x1	R/W-0x1

表 7-24. REG0x1C_NTC_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	TS_IGNORE	R/W	0x0	Reset by: REG_RESET WATCHDOG	Ignore the TS feedback, the charger will consider the TS is always good to allow charging and OTG modes, TS_STAT always reports TS_NORMAL 0b = Not ignore 1b = Ignore
6:5	CHG_RATE	R/W	0x0	Reset by: REG_RESET	The charge rate used when device is in fast-charge. Once device enters JEITA region where charge current is reduced, the resulting current is = (ICHG * foldback ratio)/CHG_RATE: 00b = 1C 01b = 2C 10b = 4C 11b = 6C
4:3	TS_TH_OTG_HOT	R/W	0x1	Reset by: REG_RESET	OTG Mode TS_HOT falling voltage threshold (as a percentage of REGN) to transition from normal operation into suspended OTG mode. 00b = 55°C 01b = 60°C 10b = 65°C 11b = Disable
2	TS_TH_OTG_COLD	R/W	0x1	Reset by: REG_RESET	OTG Mode TS_COLD rising voltage threshold (as a percentage of REGN) to transition from normal operation into suspended OTG mode. 0b = -10°C 1b = -20°C
1	TS_TH1	R/W	0x1	Reset by: REG_RESET	TS TH1 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ 0b = -5°C 1b = 0°C
0	TS_TH6	R/W	0x1	Reset by: REG_RESET	TS TH6 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ 0b = 55°C 1b = 60°C

7.6.18 REG0x1D_NTC_Control_1 Register (Address = 0x1D) [Reset = 0x85]

REG0x1D_NTC_Control_1 is shown in 図 7-34 and described in 表 7-25.

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図 7-34. REG0x1D_NTC_Control_1 Register

7	6	5	4	3	2	1	0
TS_TH2		TS_TH3		TS_TH4		TS_TH5	
R/W-0x2		R/W-0x0		R/W-0x1		R/W-0x1	

表 7-25. REG0x1D_NTC_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_TH2	R/W	0x2	Reset by: REG_RESET	TS TH2 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ 00b = 5°C 01b = 7.5°C 10b = 10°C 11b = 12.5°C
5:4	TS_TH3	R/W	0x0	Reset by: REG_RESET	TS TH3 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ 00b = 15°C 01b = 17.5°C 10b = 20°C 11b = 22.5°C
3:2	TS_TH4	R/W	0x1	Reset by: REG_RESET	TS TH4 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ 00b = 32.5°C 01b = 35°C 10b = 37.5°C 11b = 40°C
1:0	TS_TH5	R/W	0x1	Reset by: REG_RESET	TS TH5 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ 00b = 42.5°C 01b = 45°C 10b = 47.5°C 11b = 50°C

7.6.19 REG0x1E_NTC_Control_2 Register (Address = 0x1E) [Reset = 0x7F]

REG0x1E_NTC_Control_2 is shown in 図 7-35 and described in 表 7-26.

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図 7-35. REG0x1E_NTC_Control_2 Register

7	6	5	4	3	2	1	0
TS_VSET_WARM		TS_ISET_WARM		TS_VSET_PREWARM		TS_ISET_PREWARM	
R/W-0x1		R/W-0x3		R/W-0x3		R/W-0x3	

表 7-26. REG0x1E_NTC_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_VSET_WARM	R/W	0x1	Reset by: REG_RESET	TS_WARM (TH5 - TH6) Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged
5:4	TS_ISET_WARM	R/W	0x3	Reset by: REG_RESET	TS_WARM (TH5 - TH6) Current Setting 00b = Charge Suspend 01b = Set ICHG to 20% 10b = Set ICHG to 40% 11b = ICHG unchanged
3:2	TS_VSET_PREWARM	R/W	0x3	Reset by: REG_RESET	TS_PREWARM (TH4 - TH5) Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged
1:0	TS_ISET_PREWARM	R/W	0x3	Reset by: REG_RESET	TS_PREWARM (TH4 - TH5) Current Setting 00b = Charge Suspend 01b = Set ICHG to 20% 10b = Set ICHG to 40% 11b = ICHG unchanged

7.6.20 REG0x1F_NTC_Control_3 Register (Address = 0x1F) [Reset = 0xDF]

REG0x1F_NTC_Control_3 is shown in 図 7-36 and described in 表 7-27.

Return to the Summary Table.

図 7-36. REG0x1F_NTC_Control_3 Register

7	6	5	4	3	2	1	0
TS_VSET_COOL		TS_ISET_COOL		TS_VSET_PRECOOL		TS_ISET_PRECOOL	
R/W-0x3		R/W-0x1		R/W-0x3		R/W-0x3	

表 7-27. REG0x1F_NTC_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_VSET_COOL	R/W	0x3	Reset by: REG_RESET	TS_COOL (TH1 - TH2) Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged
5:4	TS_ISET_COOL	R/W	0x1	Reset by: REG_RESET	TS_COOL (TH1 - TH2) Current Setting 00b = Charge Suspend 01b = Set ICHG to 20% 10b = Set ICHG to 40% 11b = ICHG unchanged
3:2	TS_VSET_PRECOOL	R/W	0x3	Reset by: REG_RESET	TS_PRECOOL (TH2 - TH3) Voltage Setting: 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged
1:0	TS_ISET_PRECOOL	R/W	0x3	Reset by: REG_RESET	TS_PRECOOL (TH2 - TH3) Current Setting: 00b = Charge Suspend 01b = Set ICHG to 20% 10b = Set ICHG to 40% 11b = ICHG unchanged

7.6.21 REG0x20_Charger_Status_0 Register (Address = 0x20) [Reset = 0x00]

REG0x20_Charger_Status_0 is shown in 図 7-37 and described in 表 7-28.

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図 7-37. REG0x20_Charger_Status_0 Register

7	6	5	4	3	2	1	0
PG_STAT	ADC_DONE_STAT	TREG_STAT	VSYS_STAT	IINDPM_STAT	VINDPM_STAT	SAFETY_TMR_STAT	WD_STAT
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

表 7-28. REG0x20_Charger_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG_STAT	R	0x0	Power Good Indicator Status: 0b = VBUS below PG_TH 1b = VBUS above PG_TH
6	ADC_DONE_STAT	R	0x0	ADC Conversion Status (in one-shot mode only) Note: Always reads 0 in continuous mode 0b = Conversion not complete 1b = Conversion complete
5	TREG_STAT	R	0x0	IC Thermal regulation status 0b = Normal 1b = Device in thermal regulation
4	VSYS_STAT	R	0x0	VSYS Regulation Status (forward mode) 0b = Not in VSYSMIN regulation (BAT>VSYSMIN) 1b = In VSYSMIN regulation (BAT<VSYSMIN)
3	IINDPM_STAT	R	0x0	IINDPM status (forward mode) or IOTG status (OTG mode) 0b = Normal 1b = In IINDPM regulation or IOTG regulation
2	VINDPM_STAT	R	0x0	VINDPM status (forward mode) or VOTG status (OTG mode, backup mode) 0b = Normal 1b = In VINDPM regulation or VOTG regualtion
1	SAFETY_TMR_STAT	R	0x0	Fast charge, trickle charge and pre-charge timer status 0b = Normal 1b = Safety timer expired
0	WD_STAT	R	0x0	I2C watch dog timer status 0b = Normal 1b = WD timer expired

7.6.22 REG0x21_Charger_Status_1 Register (Address = 0x21) [Reset = 0x00]

REG0x21_Charger_Status_1 is shown in 図 7-38 and described in 表 7-29.

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図 7-38. REG0x21_Charger_Status_1 Register

7	6	5	4	3	2	1	0
ICO_STAT		CHG_STAT			VBUS_STAT		
R-0x0		R-0x0			R-0x0		

表 7-29. REG0x21_Charger_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	ICO_STAT	R	0x0	Input Current Optimizer (ICO) Status: 00b = ICO Disabled 01b = ICO Optimization in Progress 10b = Maximum input current detected 11b = ICO Routine Suspended
5:3	CHG_STAT	R	0x0	Charge Status: 000b = Not Charging 001b = Trickle Charge 010b = Pre-charge 011b = Fast Charge (CC) 100b = Taper Charge (CV) 101b = Reserved 110b = Top-off Timer Active Charging 111b = Charge Termination Done
2:0	VBUS_STAT	R	0x0	VBUS status: 000b = Not powered from VBUS 100b = Unknown adaptor (IINDPM Default) 111b = In boost OTG

7.6.23 REG0x22_FAULT_Status Register (Address = 0x22) [Reset = 0x00]

REG0x22_FAULT_Status is shown in 図 7-39 and described in 表 7-30.

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図 7-39. REG0x22_FAULT_Status Register

7	6	5	4	3	2	1	0
VBUS_FAULT_STAT	BAT_FAULT_STAT	VSYS_FAULT_STAT	OTG_FAULT_STAT	TSHUT_STAT	TS_STAT		
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0		

表 7-30. REG0x22_FAULT_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_STAT	R	0x0	VBUS over-voltage status 0b = Normal 1b = Device in over voltage protection
6	BAT_FAULT_STAT	R	0x0	Battery fault status 0b = Normal 1b = Dead or over-voltage battery detected
5	VSYS_FAULT_STAT	R	0x0	VSYS under voltage and over voltage status 0b = Normal 1b = SYS in SYS short circuit or over voltage
4	OTG_FAULT_STAT	R	0x0	OTG under voltage and over voltage status. 0b = Normal 1b = Fault Detected
3	TSHUT_STAT	R	0x0	IC temperature shutdown status 0b = Normal 1b = Device in thermal shutdown protection

表 7-30. REG0x22_FAULT_Status Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2:0	TS_STAT	R	0x0	The TS temperature zone. 000b = TS_NORMAL 001b = TS_COLD or TS_OTG_COLD 010b = TS_HOT or TS_OTG_HOT 011b = TS_COOL 100b = TS_WARM 101b = TS_PRECOOL 110b = TS_PREWARM 111b = RESERVED

7.6.24 REG0x23_Charger_Flag_0 Register (Address = 0x23) [Reset = 0x00]

REG0x23_Charger_Flag_0 is shown in 図 7-40 and described in 表 7-31.

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図 7-40. REG0x23_Charger_Flag_0 Register

7	6	5	4	3	2	1	0
PG_FLAG	ADC_DONE_FLAG	TREG_FLAG	VSYS_FLAG	IINDPM_FLAG	VINDPM_FLAG	SAFETY_TMR_FLAG	WD_FLAG
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

表 7-31. REG0x23_Charger_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG_FLAG	R	0x0	Power Good indicator flag: Access: R (ClearOnRead) 0b = Normal 1b = PG status changed
6	ADC_DONE_FLAG	R	0x0	ADC convertersion flag (only in one-shot mode) Access: R (ClearOnRead) 0b = Conversion not completed 1b = Conversion completed
5	TREG_FLAG	R	0x0	IC Thermal regulation flag Access: R (ClearOnRead) 0b = Normal 1b = TREG signal rising threshold detected
4	VSYS_FLAG	R	0x0	VSYS min regulation flag Access: R (ClearOnRead) 0b = Normal 1b = Entered or exited VSYS min regulation
3	IINDPM_FLAG	R	0x0	IINDPM or IOTG flag Access: R (ClearOnRead) 0b = Normal 1b = IINDPM signal rising edge detected
2	VINDPM_FLAG	R	0x0	VINDPM or VOTG flag Access: R (ClearOnRead) 0b = Normal 1b = VINDPM regulation signal rising edge detected
1	SAFETY_TMR_FLAG	R	0x0	Fast charge, trickle charge and pre-charge timer flag Access: R (ClearOnRead) 0b = Normal 1b = Fast chargeg timer expired rising edge detected

表 7-31. REG0x23_Charger_Flag_0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	WD_FLAG	R	0x0	I2C watchdog timer flag Access: R (ClearOnRead) 0b = Normal 1b = WD timer signal rising edge detected

7.6.25 REG0x24_Charger_Flag_1 Register (Address = 0x24) [Reset = 0x00]

REG0x24_Charger_Flag_1 is shown in 図 7-41 and described in 表 7-32.

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図 7-41. REG0x24_Charger_Flag_1 Register

7	6	5	4	3	2	1	0
RESERVED	ICO_FLAG	RESERVED		CHG_FLAG	RESERVED		VBUS_FLAG
R-0x0	R-0x0	R-0x0		R-0x0	R-0x0		R-0x0

表 7-32. REG0x24_Charger_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	ICO_FLAG	R	0x0	Input Current Optimizer (ICO) flag Access: R (ClearOnRead) 0b = Normal 1b = ICO_STAT[1:0] changed (transition to any state)
5:4	RESERVED	R	0x0	Reserved
3	CHG_FLAG	R	0x0	Charge status flag Access: R (ClearOnRead) 0b = Normal 1b = Charge status changed
2:1	RESERVED	R	0x0	Reserved
0	VBUS_FLAG	R	0x0	VBUS status flag Access: R (ClearOnRead) 0b = Normal 1b = VBUS status changed

7.6.26 REG0x25_FAULT_Flag Register (Address = 0x25) [Reset = 0x00]

REG0x25_FAULT_Flag is shown in 図 7-42 and described in 表 7-33.

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図 7-42. REG0x25_FAULT_Flag Register

7	6	5	4	3	2	1	0
VBUS_FAULT_FLAG	BAT_FAULT_FLAG	VSYS_FAULT_FLAG	OTG_FAULT_FLAG	TSHUT_FLAG	RESERVED		TS_FLAG
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0		R-0x0

表 7-33. REG0x25_FAULT_Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_FLAG	R	0x0	VBUS over-voltage flag Access: R (ClearOnRead) 0b = Normal 1b = Entered VBUS OVP

表 7-33. REG0x25_FAULT_Flag Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
6	BAT_FAULT_FLAG	R	0x0	VBAT over-voltage flag Access: R (ClearOnRead) 0b = Normal 1b = Entered VBAT OVP
5	VSYS_FAULT_FLAG	R	0x0	VSYS over voltage and SYS short flag Access: R (ClearOnRead) 0b = Normal 1b = Stopped switching due to system over-voltage or SYS short fault
4	OTG_FAULT_FLAG	R	0x0	OTG under voltage and over voltage flag Access: R (ClearOnRead) 0b = Normal 1b = Stopped OTG due to VBUS under voltage or over voltage fault
3	TSHUT_FLAG	R	0x0	IC thermal shutdown flag Access: R (ClearOnRead) 0b = Normal 1b = TS shutdown signal rising threshold detected
2:1	RESERVED	R	0x0	Reserved
0	TS_FLAG	R	0x0	TS status flag Access: R (ClearOnRead) 0b = Normal 1b = A change to TS status was detected

7.6.27 REG0x26_Charger_Mask_0 Register (Address = 0x26) [Reset = 0x00]

REG0x26_Charger_Mask_0 is shown in 図 7-43 and described in 表 7-34.

Return to the Summary Table.

図 7-43. REG0x26_Charger_Mask_0 Register

7	6	5	4	3	2	1	0
PG_MASK	ADC_DONE_MASK	TREG_MASK	VSYS_MASK	IINDPM_MASK	VINDPM_MASK	SAFETY_TMR_MASK	WD_MASK
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

表 7-34. REG0x26_Charger_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_MASK	R/W	0x0	Reset by: REG_RESET	Power Good indicator INT mask 0b = PG status change does produce INT pulse 1b = PG status change does not produce INT pulse
6	ADC_DONE_MASK	R/W	0x0	Reset by: REG_RESET	ADC conversion INT mask (only in one-shot mode) 0b = ADC conversion done does produce INT pulse 1b = ADC conversion done does not produce INT pulse
5	TREG_MASK	R/W	0x0	Reset by: REG_RESET	IC thermal regulation INT mask 0b = Entering TREG does produce INT 1b = Entering TREG does not produce INT
4	VSYS_MASK	R/W	0x0	Reset by: REG_RESET	VSYS min regulation INT mask 0b = Enter or exit VSYSMIN regulation does produce INT pulse 1b = Enter or exit VSYSMIN regulation does not produce INT pulse

表 7-34. REG0x26_Charger_Mask_0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
3	IINDPM_MASK	R/W	0x0	Reset by: REG_RESET	IINDPM or IOTG INT mask 0b = Enter IINDPM or IOTG does produce INT pulse 1b = Enter IINDPM or IOTG does not produce INT pulse
2	VINDPM_MASK	R/W	0x0	Reset by: REG_RESET	VINDPM or VOTG INT mask 0b = Enter VINDPM does produce INT pulse 1b = Enter VINDPM does not produce INT pulse
1	SAFETY_TMR_MASK	R/W	0x0	Reset by: REG_RESET	Fast charge, trickle charge and pre-charge timer INT mask 0b = Fast charge, trickle charge or pre-charge timer expiration does produce INT 1b = Fast charge, trickle charge or pre-charge timer expiration does not produce INT
0	WD_MASK	R/W	0x0	Reset by: REG_RESET	I2C watch dog timer INT mask 0b = I2C watch dog timer expired does produce INT pulse 1b = I2C watch dog timer expired does not produce INT pulse

7.6.28 REG0x27_Charger_Mask_1 Register (Address = 0x27) [Reset = 0x00]

REG0x27_Charger_Mask_1 is shown in 図 7-44 and described in 表 7-35.

Return to the Summary Table.

図 7-44. REG0x27_Charger_Mask_1 Register

7	6	5	4	3	2	1	0
RESERVED	ICO_MASK	RESERVED		CHG_MASK	RESERVED		VBUS_MASK
R-0x0	R/W-0x0	R-0x0		R/W-0x0	R-0x0		R/W-0x0

表 7-35. REG0x27_Charger_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6	ICO_MASK	R/W	0x0	Reset by: REG_RESET	Input Current Optimizer (ICO) INT mask 0b = ICO_STAT change does produce INT 1b = ICO_STAT change does not produce INT
5:4	RESERVED	R	0x0		Reserved
3	CHG_MASK	R/W	0x0	Reset by: REG_RESET	Charge status INT mask 0b = Charging status change does produce INT 1b = Charging status change does not produce INT
2:1	RESERVED	R	0x0		Reserved
0	VBUS_MASK	R/W	0x0	Reset by: REG_RESET	VBUS status INT mask 0b = VBUS status change does produce INT 1b = VBUS status change does not produce INT

7.6.29 REG0x28_FAULT_Mask Register (Address = 0x28) [Reset = 0x00]

REG0x28_FAULT_Mask is shown in 図 7-45 and described in 表 7-36.

Return to the Summary Table.

図 7-45. REG0x28_FAULT_Mask Register

7	6	5	4	3	2	1	0

図 7-45. REG0x28_FAULT_Mask Register (続き)

VBUS_FAULT_MASK	BAT_FAULT_MASK	VSYS_FAULT_MASK	OTG_FAULT_MASK	TSHUT_MASK	RESERVED	TS_MASK
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R-0x0	R/W-0x0

表 7-36. REG0x28_FAULT_Mask Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VBUS_FAULT_MASK	R/W	0x0	Reset by: REG_RESET	VBUS over-voltage INT mask 0b = Entering VBUS OVP does produce INT 1b = Entering VBUS OVP does not produce INT
6	BAT_FAULT_MASK	R/W	0x0	Reset by: REG_RESET	IBAT/VBAT over-current/over-voltage INT mask 0b = Entering IBAT OCP or VBAT OVP does produce INT 1b = Entering IBAT OCP or VBAT OVP does not produce INT
5	VSYS_FAULT_MASK	R/W	0x0	Reset by: REG_RESET	VSYS over voltage and SYS short INT mask 0b = System over-voltage or SYS short fault does produce INT 1b = Neither system over voltage nor SYS short fault produces INT
4	OTG_FAULT_MASK	R/W	0x0	Reset by: REG_RESET	OTG under voltage and over voltage INT mask 0b = OTG VBUS under voltage or over voltage fault does produce INT 1b = Neither OTG VBUS under voltage nor over voltage fault produces INT
3	TSHUT_MASK	R/W	0x0	Reset by: REG_RESET	IC thermal shutdown INT mask 0b = TSHUT does produce INT 1b = TSHUT does not produce INT
2:1	RESERVED	R	0x0		Reserved
0	TS_MASK	R/W	0x0	Reset by: REG_RESET	Temperature charging profile INT mask 0b = A change to TS temperature zone does produce INT 1b = A change to the TS temperature zone does not produce INT

7.6.30 REG0x29_ICO_Current_Limit Register (Address = 0x29) [Reset = 0x0000]

REG0x29_ICO_Current_Limit is shown in 図 7-46 and described in 表 7-37.

Return to the Summary Table.

図 7-46. REG0x29_ICO_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				ICO_IINDPM			
R-0x0				R-0x0			
7	6	5	4	3	2	1	0
ICO_IINDPM				RESERVED			
R-0x0				R-0x0			

表 7-37. REG0x29_ICO_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved

表 7-37. REG0x29_ICO_Current_Limit Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
11:4	ICO_IINDPM	R	0x0	This 16-bit register follows the little-endian convention Reset by: Adapter Unplug	Optimized Input Current Limit when ICO is enabled: POR: 0mA (0h) Range: 100mA-3200mA (5h-A0h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0x0		Reserved

7.6.31 REG0x2B_ADC_Control Register (Address = 0x2B) [Reset = 0x30]

REG0x2B_ADC_Control is shown in 図 7-47 and described in 表 7-38.

Return to the Summary Table.

図 7-47. REG0x2B_ADC_Control Register

7	6	5	4	3	2	1	0
EN_ADC	ADC_RATE	ADC_SAMPLE		ADC_AVG	ADC_AVG_INIT	RESERVED	DIS_ADCIN_ADC
R/W-0x0	R/W-0x0	R/W-0x3		R/W-0x0	R/W-0x0	R-0x0	R/W-0x0

表 7-38. REG0x2B_ADC_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_ADC	R/W	0x0	Reset by: REG_RESET WATCHDOG	ADC Control 0b = Disable (default) 1b = Enable
6	ADC_RATE	R/W	0x0	Reset by: REG_RESET	ADC conversion rate control 0b = Continuous conversion (default) 1b = One shot conversion
5:4	ADC_SAMPLE	R/W	0x3	Reset by: REG_RESET	ADC sample speed 00b = 11 bit effective resolution 01b = 10 bit effective resolution 10b = 9 bit effective resolution 11b = 8 bit effective resolution (default)
3	ADC_AVG	R/W	0x0	Reset by: REG_RESET	ADC average control 0b = Single value (default) 1b = Running average
2	ADC_AVG_INIT	R/W	0x0	Reset by: REG_RESET	ADC acerage initial value control 0b = Start average using the existing register value 1b = Start average using a new ADC conversion
1	RESERVED	R	0x0		Reserved
0	DIS_ADCIN_ADC	R/W	0x0	Reset by: REG_RESET	ADCIN ADC channel disable 0b = Enable 1b = Disable

7.6.32 REG0x2C_ADC_Channel_Disable Register (Address = 0x2C) [Reset = 0x00]

REG0x2C_ADC_Channel_Disable is shown in 図 7-48 and described in 表 7-39.

Return to the Summary Table.

図 7-48. REG0x2C_ADC_Channel_Disable Register

7	6	5	4	3	2	1	0
DIS_IBUS_ADC	DIS_IBAT_ADC	DIS_VBUS_ADC	DIS_VBAT_ADC	DIS_VSYS_ADC	DIS_TS_ADC	DIS_TDIE_ADC	DIS_VPMID_ADC
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

図 7-48. REG0x2C_ADC_Channel_Disable Register (続き)

表 7-39. REG0x2C_ADC_Channel_Disable Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DIS_IBUS_ADC	R/W	0x0	Reset by: REG_RESET	IBUS ADC channel disable 0b = Enable 1b = Disable
6	DIS_IBAT_ADC	R/W	0x0	Reset by: REG_RESET	IBAT ADC control 0b = Enable 1b = Disable
5	DIS_VBUS_ADC	R/W	0x0	Reset by: REG_RESET	VBUS ADC control 0b = Enable 1b = Disable
4	DIS_VBAT_ADC	R/W	0x0	Reset by: REG_RESET	VBAT ADC control 0b = Enable 1b = Disable
3	DIS_VSYS_ADC	R/W	0x0	Reset by: REG_RESET	VSYS ADC control 0b = Enable 1b = Disable
2	DIS_TS_ADC	R/W	0x0	Reset by: REG_RESET	TS ADC control 0b = Enable 1b = Disable
1	DIS_TDIE_ADC	R/W	0x0	Reset by: REG_RESET	TDIE ADC control 0b = Enable 1b = Disable
0	DIS_VPMID_ADC	R/W	0x0	Reset by: REG_RESET	VPMID ADC control 0b = Enable 1b = Disable

7.6.33 REG0x2D_IBUS_ADC Register (Address = 0x2D) [Reset = 0x0000]

REG0x2D_IBUS_ADC is shown in 図 7-49 and described in 表 7-40.

Return to the Summary Table.

図 7-49. REG0x2D_IBUS_ADC Register

15	14	13	12	11	10	9	8
IBUS_ADC							
R-0x0							
7	6	5	4	3	2	1	0
IBUS_ADC							RESERVED
R-0x0							R-0x0

表 7-40. REG0x2D_IBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	IBUS_ADC	R	0x0	IBUS ADC reading Reported in 2 's Complement. When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value. POR: 0mA(0h) Format: 2s Complement Range: -5000mA - 5000mA (7830h-7D0h) Clamped Low Clamped High Bit Step: 2.5mA
0	RESERVED	R	0x0	Reserved

7.6.34 REG0x2F_IBAT_ADC Register (Address = 0x2F) [Reset = 0x0000]

REG0x2F_IBAT_ADC is shown in 図 7-50 and described in 表 7-41.

Return to the Summary Table.

図 7-50. REG0x2F_IBAT_ADC Register

15	14	13	12	11	10	9	8
IBAT_ADC							
R-0x0							
7	6	5	4	3	2	1	0
IBAT_ADC						RESERVED	
R-0x0						R-0x0	

表 7-41. REG0x2F_IBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	IBAT_ADC	R	0x0	IBAT ADC reading Reported in 2 's Complement. The IBAT ADC reports positive value for the battery charging current, and negative value for the battery discharging current. POR: 0mA (0h) Format: 2s Complement Range: -10000mA-5025mA (1830h-3EDh) Clamped Low Clamped High Bit Step: 5mA
2:0	RESERVED	R	0x0	Reserved

7.6.35 REG0x31_VBUS_ADC Register (Address = 0x31) [Reset = 0x0000]

REG0x31_VBUS_ADC is shown in 図 7-51 and described in 表 7-42.

Return to the Summary Table.

図 7-51. REG0x31_VBUS_ADC Register

15	14	13	12	11	10	9	8
RESERVED	VBUS_ADC						
R-0x0	R-0x0						
7	6	5	4	3	2	1	0
VBUS_ADC						RESERVED	
R-0x0						R-0x0	

表 7-42. REG0x31_VBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:2	VBUS_ADC	R	0x0	VBUS ADC reading POR: 0mV (0h) Range: 0mV-20000mV (0h-FA0h) Clamped High Bit Step: 5mV
1:0	RESERVED	R	0x0	Reserved

7.6.36 REG0x33_VPMID_ADC Register (Address = 0x33) [Reset = 0x0000]

REG0x33_VPMID_ADC is shown in 図 7-52 and described in 表 7-43.

Return to the Summary Table.

図 7-52. REG0x33_VPMID_ADC Register

15	14	13	12	11	10	9	8
RESERVED	VPMID_ADC						
R-0x0	R-0x0						
7	6	5	4	3	2	1	0
VPMID_ADC						RESERVED	
R-0x0						R-0x0	

表 7-43. REG0x33_VPMID_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:2	VPMID_ADC	R	0x0	VPMID ADC reading POR: 0mV (0h) Range: 0mV-20000mV (0h-FA0h) Clamped High Bit Step: 5mV
1:0	RESERVED	R	0x0	Reserved

7.6.37 REG0x35_VBAT_ADC Register (Address = 0x35) [Reset = 0x0000]

REG0x35_VBAT_ADC is shown in 図 7-53 and described in 表 7-44.

Return to the Summary Table.

図 7-53. REG0x35_VBAT_ADC Register

15	14	13	12	11	10	9	8
RESERVED			VBAT_ADC				
R-0x0			R-0x0				
7	6	5	4	3	2	1	0
VBAT_ADC							RESERVED
R-0x0							R-0x0

表 7-44. REG0x35_VBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved

表 7-44. REG0x35_VBAT_ADC Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
12:1	VBAT_ADC	R	0x0	VBAT ADC reading POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV
0	RESERVED	R	0x0	Reserved

7.6.38 REG0x37_VSYS_ADC Register (Address = 0x37) [Reset = 0x0000]

REG0x37_VSYS_ADC is shown in 図 7-54 and described in 表 7-45.

Return to the Summary Table.

図 7-54. REG0x37_VSYS_ADC Register

15	14	13	12	11	10	9	8
RESERVED			VSYS_ADC				
R-0x0			R-0x0				
7	6	5	4	3	2	1	0
VSYS_ADC							RESERVED
R-0x0							R-0x0

表 7-45. REG0x37_VSYS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:1	VSYS_ADC	R	0x0	VSYS ADC reading POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV
0	RESERVED	R	0x0	Reserved

7.6.39 REG0x39_TS_ADC Register (Address = 0x39) [Reset = 0x0000]

REG0x39_TS_ADC is shown in 図 7-55 and described in 表 7-46.

Return to the Summary Table.

図 7-55. REG0x39_TS_ADC Register

15	14	13	12	11	10	9	8
RESERVED				TS_ADC			
R-0x0				R-0x0			
7	6	5	4	3	2	1	0
TS_ADC							
R-0x0							

表 7-46. REG0x39_TS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved

表 7-46. REG0x39_TS_ADC Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
11:0	TS_ADC	R	0x0	TS ADC reading POR: 0%(0h) Range: 0% - 99.90234375% (0h-3FFh) Clamped High Bit Step: 0.09765625%

7.6.40 REG0x3B_TDIE_ADC Register (Address = 0x3B) [Reset = 0x0000]

REG0x3B_TDIE_ADC is shown in 図 7-56 and described in 表 7-47.

Return to the Summary Table.

図 7-56. REG0x3B_TDIE_ADC Register

15	14	13	12	11	10	9	8
RESERVED				TDIE_ADC			
R-0x0				R-0x0			
7	6	5	4	3	2	1	0
TDIE_ADC							
R-0x0							

表 7-47. REG0x3B_TDIE_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved
11:0	TDIE_ADC	R	0x0	TDIE ADC reading Reported in 2 's Complement. POR: 0°C(0h) Format: 2s Complement Range: -40°C - 150°C (FB0h-12Ch) Clamped Low Clamped High Bit Step: 0.5°C

7.6.41 REG0x3D_ADCIN_ADC Register (Address = 0x3D) [Reset = 0x0000]

REG0x3D_ADCIN_ADC is shown in 図 7-57 and described in 表 7-48.

Return to the Summary Table.

図 7-57. REG0x3D_ADCIN_ADC Register

15	14	13	12	11	10	9	8
RESERVED				ADCIN_ADC			
R-0x0				R-0x0			
7	6	5	4	3	2	1	0
ADCIN_ADC							
R-0x0							

表 7-48. REG0x3D_ADCIN_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved

表 7-48. REG0x3D_ADCIN_ADC Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
11:0	ADCIN_ADC	R	0x0	ADCIN ADC reading POR: 0mV(0h) Range: 0mV - 1000mV (0h-FA0h) Clamped High Bit Step: 0.25mV

7.6.42 REG0x3F_Part_Information Register (Address = 0x3F) [Reset = 0x08]

REG0x3F_Part_Information is shown in 図 7-58 and described in 表 7-49.

Return to the Summary Table.

図 7-58. REG0x3F_Part_Information Register

7	6	5	4	3	2	1	0
TEST_REV		PN				DEV_REV	
R-0x0		R-0x2				R-0x0	

表 7-49. REG0x3F_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TEST_REV	R	0x0	Test Revision
5:2	PN	R	0x2	Device Part number
1:0	DEV_REV	R	0x0	Device Revision

7.6.43 REG0x80_Virtual_Control_0 Register (Address = 0x80) [Reset = 0x11]

REG0x80_Virtual_Control_0 is shown in 図 7-59 and described in 表 7-50.

Return to the Summary Table.

図 7-59. REG0x80_Virtual_Control_0 Register

7	6	5	4	3	2	1	0
REG_RST	RESERVED	RESERVED	EN_EXTILIM	RESERVED	WD_RST	WATCHDOG	
R/W-0x0	R-0x0	R-0x0	R/W-0x1	R-0x0	R/W-0x0	R/W-0x1	

表 7-50. REG0x80_Virtual_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0x0		Reset registers to default values and reset timer Value resets to 0 after reset completes. 0b = Not reset (default) 1b = Reset
6	RESERVED	R	0x0		Reserved
5	RESERVED	R	0x0		Reserved
4	EN_EXTILIM	R/W	0x1	Reset by: REG_RESET	Enable the external ILIM_HIZ pin input current regulation 0b = Disable 1b = Enable (default)
3	RESERVED	R	0x0		Reserved
2	WD_RST	R/W	0x0	Reset by: REG_RESET	I2C watch dog timer reset 0b = Normal (default) 1b = Reset (this bit goes back to 0 after timer reset)

表 7-50. REG0x80_Virtual_Control_0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
1:0	WATCHDOG	R/W	0x1	Reset by: REG_RESET	Watchdog timer setting 00b = Disable 01b = 40s (default) 10b = 80s 11b = 160s

7.6.44 REG0x81_Virtual_Control_1 Register (Address = 0x81) [Reset = 0x80]

REG0x81_Virtual_Control_1 is shown in 図 7-60 and described in 表 7-51.

Return to the Summary Table.

図 7-60. REG0x81_Virtual_Control_1 Register

7	6	5	4	3	2	1	0
EN_CHG	RESERVED					FORCE_PMID_DSCHG	EN_OTG
R/W-0x1	R-0x0					R/W-0x0	R/W-0x0

表 7-51. REG0x81_Virtual_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_CHG	R/W	0x1	Reset by: REG_RESET WATCHDOG	Enable PMID pull down current source (~30mA) 0b = Charge Disable 1b = Charge Enable (default)
6:2	RESERVED	R	0x0		Reserved
1	FORCE_PMID_DSCHG	R/W	0x0	Reset by: REG_RESET	Enable PMID pull down current source (~30mA) 0b = Disable (default) 1b = Enable
0	EN_OTG	R/W	0x0	Reset by: REG_RESET WATCHDOG	OTG mode control 0b = OTG Disable (default) 1b = OTG Enable

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A typical application consists of the device configured as an I²C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphone and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

8.2 Typical Application

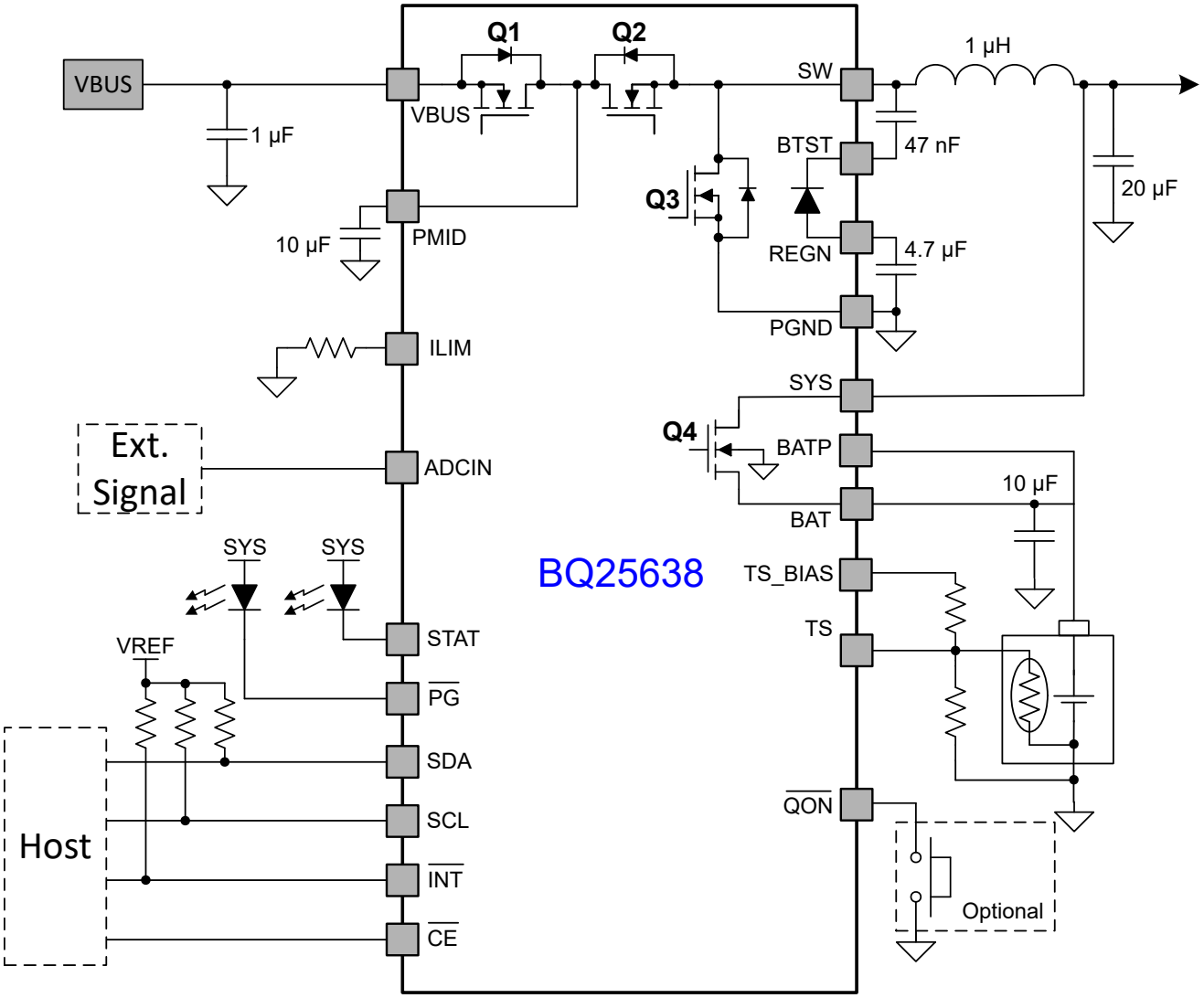


図 8-1. BQ25638 Typical Application

8.2.1 Design Requirements

表 8-1. Design Requirements

PARAMETER	VALUE
VBUS range	3.9 - 18.0 V
Input current limit (REG0x06-0x07)	3200 mA
Fast charge current (REG0x02-0x03)	5040 mA
Minimum system voltage (REG0x0E-0x0F)	3520 mV
Battery regulation voltage (REG0x04-0x05)	4200 mV

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{8}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \tag{9}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

8.2.2.2 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{Cin} occurs where the duty cycle is closest to 50% and can be estimated using 式 10.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{10}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15 V input voltage. 10-µF ceramic capacitor is suggested for typical of 4.0A charging current.

8.2.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. 式 11 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{11}$$

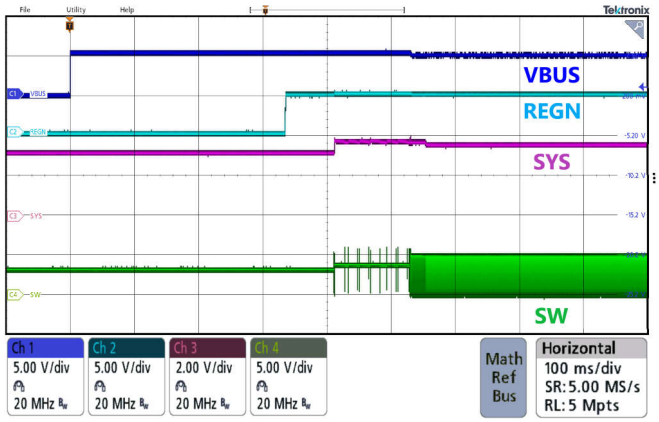
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{12}$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

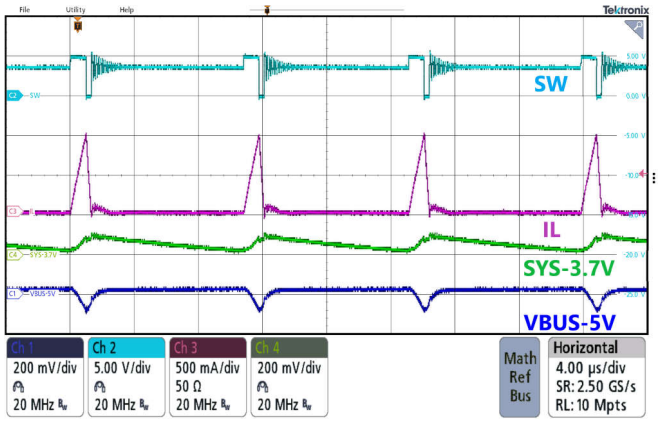
The charger device has internal loop compensation optimized for ≥ 10-µF ceramic output capacitor. The preferred ceramic capacitor is 10-V rating, X7R or X5R.

8.2.3 Application Curves



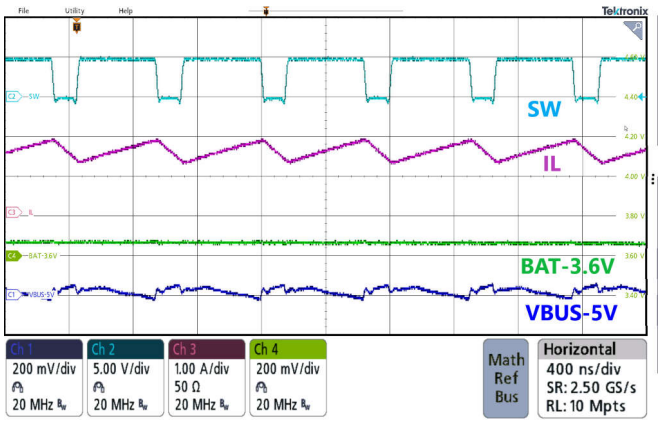
V_{VBUS} = 5 V V_{VBAT} = 3.2 V
I_{CHG} = 2 A

図 8-2. Power-Up with Charge Enabled



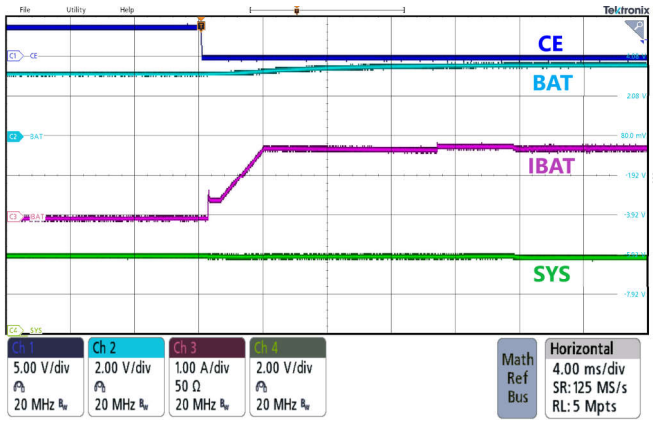
V_{VBUS} = 5 V Charge Disabled
I_{SYS} = 50 mA

図 8-3. PFM Switching in Buck Mode



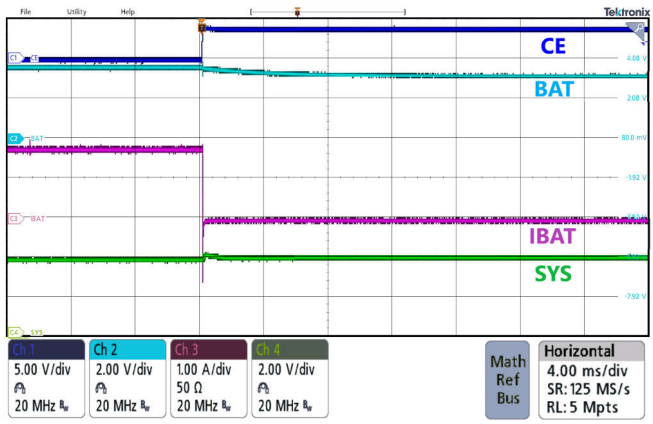
V_{VBUS} = 5 V V_{BAT} = 3.2 V
I_{CHG} = 2 A

図 8-4. PWM Switching in Buck Mode



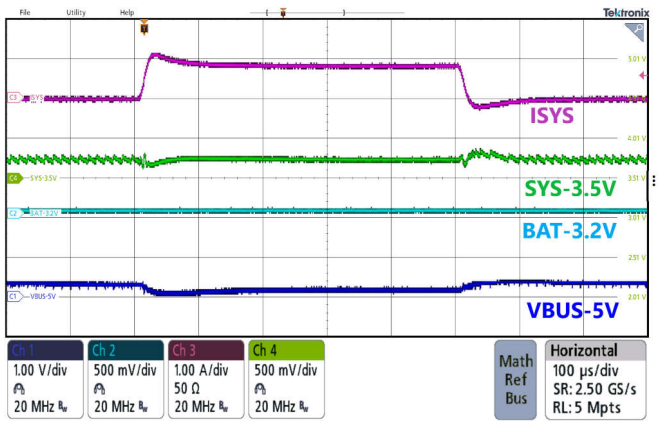
V_{VBUS} = 5 V V_{VBAT} = 3.2 V
I_{CHG} = 2 A

図 8-5. Charge Enable



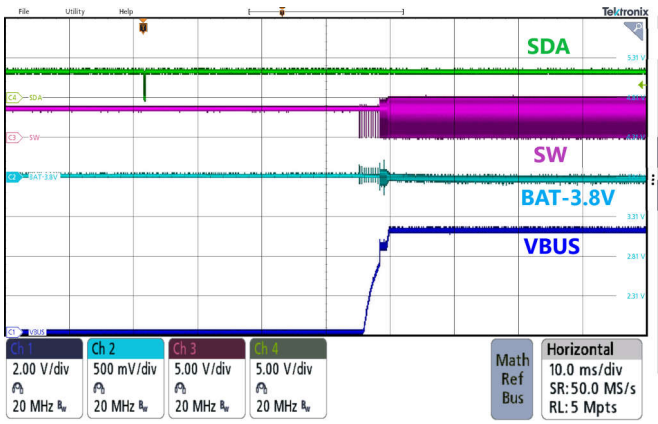
V_{VBUS} = 5 V V_{VBAT} = 3.2 V
I_{CHG} = 2 A

図 8-6. Charge Disable



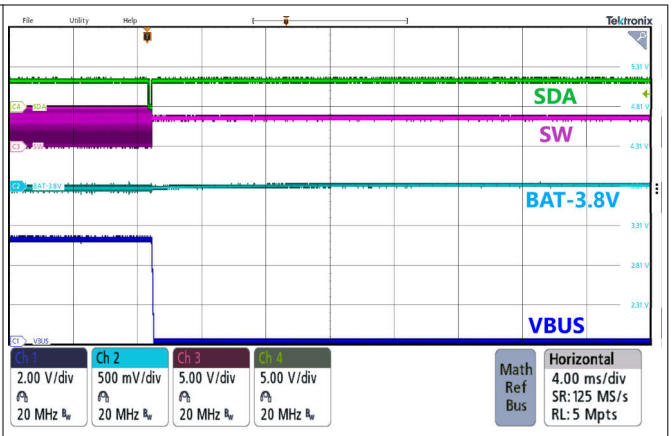
V_{VBUS} = 5 V V_{BAT} = 3.2 V
I_{SYS} = 0 A to 1A Charge Disabled

図 8-7. System Load Transient Response



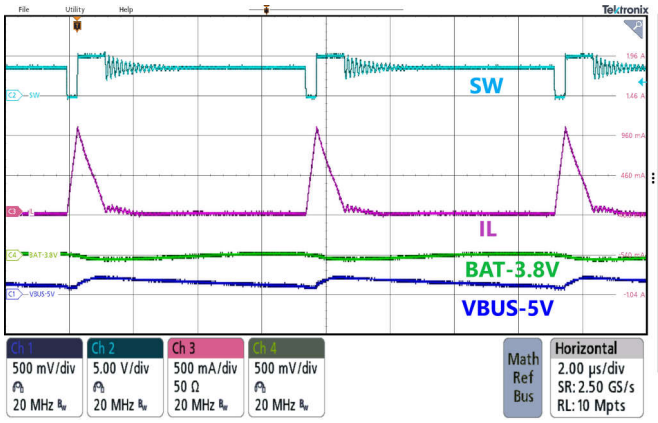
V_{OTG} = 5.12 V V_{VBAT} = 3.8 V
I_{BUS} = 100 mA

図 8-8. Boost Mode Power Up



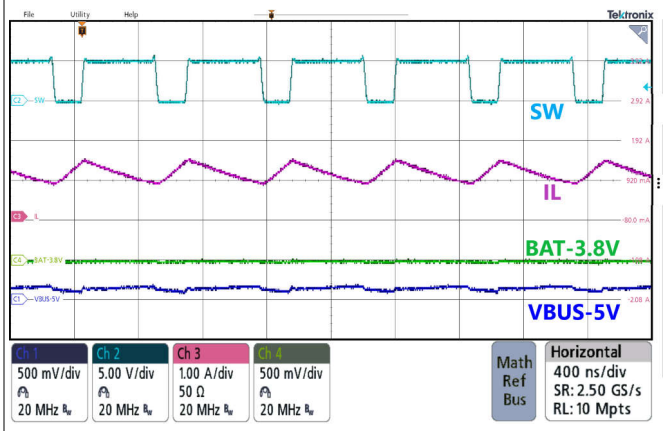
V_{OTG} = 5.12 V V_{VBAT} = 3.8 V
I_{BUS} = 100 mA

図 8-9. Boost Mode Power Down



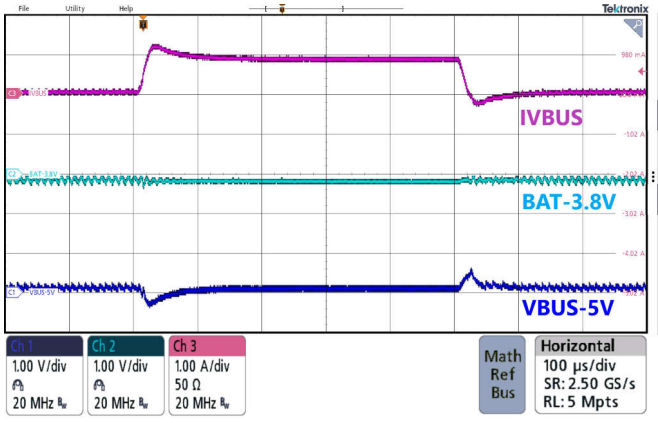
V_{OTG} = 5.12 V V_{VBAT} = 3.8 V
I_{BUS} = 50 mA

図 8-10. PFM Switching in Boost Mode



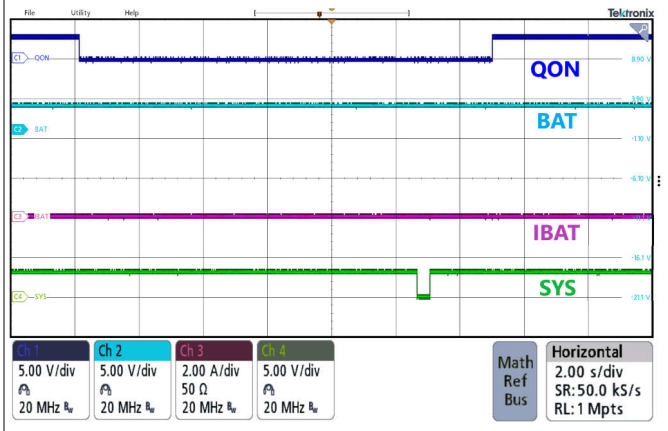
V_{OTG} = 5.12 V V_{VBAT} = 3.8 V
I_{BUS} = 1 A

図 8-11. PWM Switching in Boost Mode



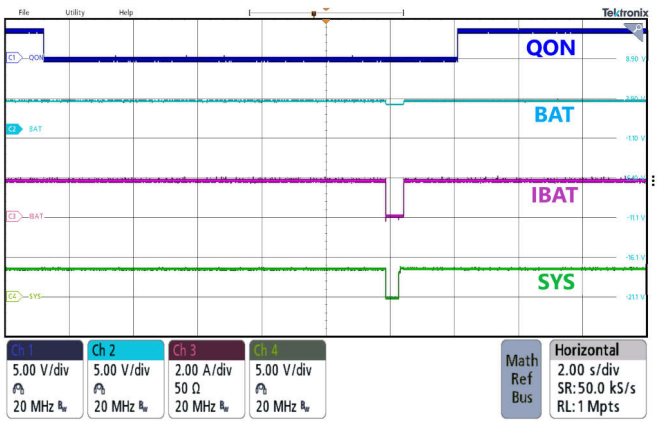
V_{OTG} = 5.12 V V_{VBAT} = 3.8 V
I_{BUS}= 0 A to 1 A

図 8-12. Boost Mode Transient Response



V_{VBAT} = 3.2 V

図 8-13. System Reset by QON without VBUS Present



V_{VBUS} = 5 V V_{VBAT} = 3.2 V

図 8-14. System Reset by QON with VBUS Present

9 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 18V input with at least 100-mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT.

10 Layout

10.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see 図 10-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
5. Ensure that the number and sizes of vias allow enough copper for a given current path.

10.2 Layout Example

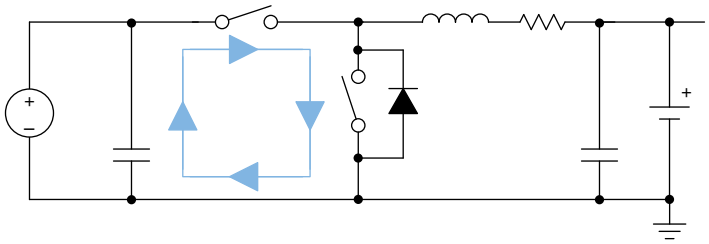


図 10-1. High Frequency Current Path

11 Device and Documentation Support

11.1 Device Support

11.1.1 サード・パーティ製品に関する免責事項

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *BQ25601 and BQ25601D (PWR877) Evaluation Module User's Guide*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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11.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2023) to Revision A (December 2023)	Page
• 「事前情報」から「量産データ」に変更	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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