TEXAS INSTRUMENTS
AMC1333M10
JAJSOP1 – MAY 2022

AMC1333M10 高精度、±1V 入力、10MHz 内部クロック搭載、強化絶縁型デルタ-シグマ変調器

1 特長

- リニア入力電圧範囲：±1V
- 高い入力インピーダンス：2.4GΩ (標準値)
- 小さな DC 誤差：
  - オフセット誤差：±0.5mV (最大値)
  - オフセット・ドリフト：±4µV/℃ (最大値)
  - ゲイン誤差：±0.2% (最大値)
  - ゲイン・ドリフト：±40ppm/℃ (最大値)
- 高 CMTI：100kV/µs (最小値)
- 10MHz クロック・ジェネレータを内蔵
- ハイサイド電源喪失の検出
- 低 EMI：CISPR-11 および CISPR-25 規格に準拠
- 安全関連の認定：
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧：8000V_{PEAK}
  - UL 1577 に準拠した絶縁耐圧：5700V_{RMS} (1 分間)
- 拡張産業用温度範囲にわたって仕様を完全に規定–40℃～+125℃

2 アプリケーション

- モーター・ドライブ
- 周波数インバータ
- 保護リレー
- 電源

3 概要

AMC1333M10 は高精度のデルタ・シグマ (ΔΣ) 変調器で、磁気干渉に対して高い耐性のある絶縁バリアにより、入力と出力の回路が分離されています。このバリアは、DIN EN IEC 60747-17 (VDE 0884-17) および UL1577 規格に従って最大 8000V_{PEAK} の強化絶縁を達成していることが認証され、最大 1.5kV_{RMS} の使用電圧に対応しています。この絶縁バリアは、異なる同相電圧レベルで動作するシステム領域を分離し、電気的損傷を生じさせる可能性がある電圧またはオペレータに害を及ぼす可能性がある電圧から低電圧側を保護します。

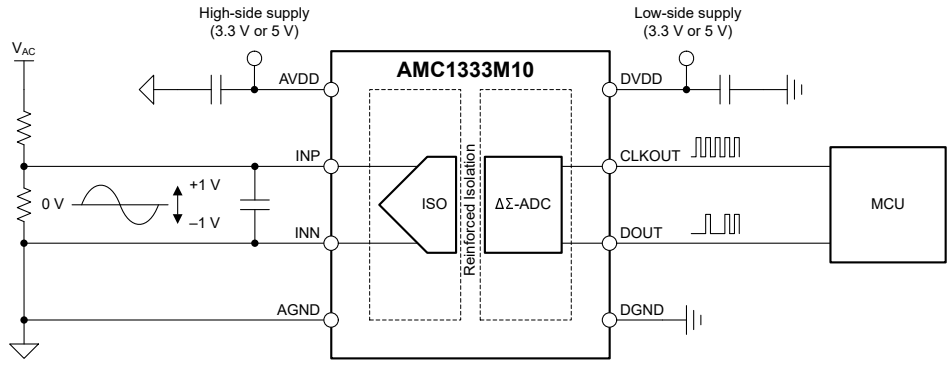
±1V の広いバイポーラ入力電圧範囲と高い入力抵抗を特長とする AMC1333M10 は、高電圧アプリケーションでデバイスを分圧抵抗に直接接続できます。AMC1333M10 の出力ビットストリームは、内部で生成されるクロックと同期します。内蔵デジタル・フィルタ (TMS320F2807x や TMS320F2837x マイクロコントローラ・ファミリで使用されているものなど) を使用してビットストリームを間引くと、39kSPS のデータ速度、87dB のダイナミック・レンジで、16 ビットの分解能が得られます。

AMC1333M10 は 8 ピンのワイド・ボディ SOIC パッケージで提供され、–40℃～+125℃の拡張産業用温度範囲で完全に動作が規定されています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
AMC1333M10	SOIC (8)	5.85mm × 7.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
May 2022	*	Initial release.

5 Pin Configuration and Functions

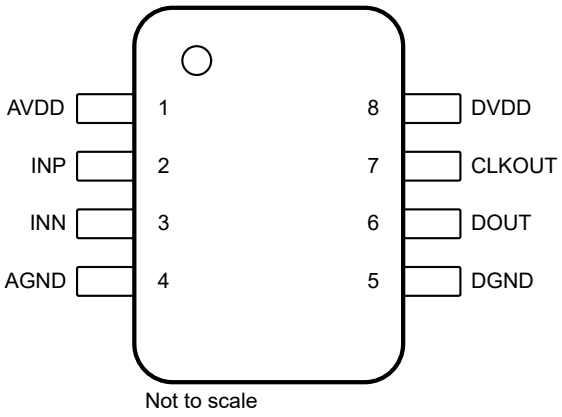


図 5-1. DWV Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	High-side power	Analog (high-side) power supply(1)
2	INP	Analog input	Noninverting analog input
3	INN	Analog input	Inverting analog input
4	AGND	High-side ground	Analog (high-side) ground reference
5	DGND	Low-side ground	Digital (low-side) ground reference
6	DOUT	Digital output	Modulator data output
7	CLKOUT	Digital output	Modulator clock output
8	DVDD	Low-side power	Digital (low-side) power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	6.5	V
	DVDD to DGND	–0.3	6.5	
Analog input voltage	On the INP and INN pins	AGND – 5	AVDD + 0.5	V
Digital input voltage	On the CLKIN pin	DGND – 0.5	DVDD + 0.5	V
Digital output voltage	On the DOUT pin	DGND – 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions* . If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	High-side supply voltage	AVDD to AGND	3.0	5.0	5.5	V
DVDD	Low-side supply voltage	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±1.25		V
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{AINP} – V_{AINN}$	–1		1	V
	Absolute common-mode input voltage(1)	$(V_{INP} + V_{INN}) / 2$ to AGND	–2		AVDD	V
V_{CM}	Operating common-mode input voltage(2)	$(V_{INP} + V_{INN}) / 2$ to AGND, 3.0 V ≤ AVDD < 4.5 V, $\lvert V_{INP} – V_{INN} \rvert \le 1.25$ V	–0.8		AVDD – 2.4	V
		$(V_{INP} + V_{INN}) / 2$ to AGND, 4.5 V ≤ AVDD ≤ 5.5 V, $\lvert V_{INP} – V_{INN} \rvert \le 1.25$ V	–0.8		2.1	
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40	25	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.
(2) See the *Analog Input* section for more details.

6.4 Thermal Information

THERMAL METRIC(1)		DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5 V	78	mW
P_{D1}	Maximum power dissipation (high-side supply)	AVDD = 3.6 V	27	mW
		AVDD = 5.5 V	46	
P_{D2}	Maximum power dissipation (low-side supply)	DVDD = 3.6 V	18	mW
		DVDD = 5.5 V	32	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	8000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	9600	
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 V_{PP} at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5700 V_{RMS}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6840 V_{RMS}, t = 1 s (100% production test)	5700	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition program
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 94°C/W, T_J = 150°C, T_A = 25°C, AVDD = DVDD = 5.5 V			242	mA
		$R_{\theta JA}$ = 94°C/W, T_J = 150°C, T_A = 25°C, AVDD = DVDD = 3.6 V			369	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 94°C/W, T_J = 150°C, T_A = 25°C			1330	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$, where $AVDD_{max}$ is the maximum high-side voltage and $DVDD_{max}$ is the maximum controller-side supply voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, INP = –1 V to +1 V, and INN = AGND = 0 V; typical specifications are at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Single-ended input resistance	INN = AGND	0.1	2.4		GΩ
R_{IND}	Differential input resistance		0.1	3		GΩ
I_{IB}	Input bias current	INP = INN = AGND, $I_{IB} = (I_{INP} + I_{INN}) / 2$	–10	±3	10	nA
TCI_{IB}	Input bias current temperature drift			–7		pA/°C
I_{IO}	Input offset current	$I_{IO} = I_{INP} – I_{INN}$	–5	±1	5	nA
C_{IN}	Single-ended input capacitance	INN = AGND		2		pF
C_{IND}	Differential input capacitance			2		pF
CMTI	Common-mode transient immunity	|AGND – DGND| = 1 kV	100	150		kV/µs
CMRR	Common-mode rejection ratio	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–104		dB
		INP = INN, f_{IN} = 10 kHz, –0.5 V ≤ V_{IN} ≤ 0.5 V		–89		
PSRR	Power-supply rejection ratio	PSRR vs AVDD, at DC		–86		dB
		PSRR vs AVDD, 100-mV and 10-kHz ripple		–86		
DC ACCURACY						
E_O	Offset error(1) (2)	INP = INN = AGND, T_A = 25°C	–0.5	±0.04	0.5	mV
TCE_O	Offset error temperature drift(4)		–4	±0.6	4	µV/°C
E_G	Gain error(2)	T_A = 25°C	–0.2%	±0.03%	0.2%	
TCE_G	Gain error temperature drift(5)		–40	±20	40	ppm/°C
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(3)	Resolution: 16 bits	–5	±1.6	5	LSB
AC ACCURACY						
THD	Total harmonic distortion(6)	V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz, single-ended input (AINN = AGND)		–91	–82	dB
DIGITAL OUTPUT (CMOS)						
C_{LOAD}	Output load capacitance			15		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 m	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 m			0.4	

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, INP = –1 V to +1 V, and INN = AGND = 0 V; typical specifications are at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$AVDD_{UV}$	AVDD undervoltage detection threshold	AVDD rising	2.1		2.65	V
		AVDD falling	1.95		2.5	
$DVDD_{UV}$	DVDD undervoltage detection threshold	DVDD rising	2.2	2.45	2.65	V
		DVDD falling	1.8		2.2	V
I_{AVDD}	High-side supply current	3 V ≤ AVDD ≤ 3.6 V		5.8	7.6	mA
		4.5 V ≤ AVDD ≤ 5.5 V		6.4	8.4	
I_{DVDD}	Low-side supply current	2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		4	5.1	mA
		4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		4.4	5.8	

(1) This parameter is input referred.
(2) The typical value includes one sigma statistical variation.
(3) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCE_O = (E_{O,MAX} – E_{O,MIN}) / TempRange$ where $E_{O,MAX}$ and $E_{O,MIN}$ refer to the maximum and minimum E_O values measured within the temperature range (–40 to 125°C).
(5) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125°C).
(6) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Internal clock frequency		9.5	10	10.5	MHz
	Internal clock duty cycle		45%	50%	55%	
t_H	DOUT hold time after rising edge of CLKOUT	C_{LOAD} = 15 pF	3.5			ns
t_D	DOUT hold time after rising edge of CLKOUT	C_{LOAD} = 15 pF			15	ns
t_r	DOUT and CLKOUT rise time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	6	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.2	6	
t_f	DOUT and CLKOUT fall time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.2	6	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		2.9	6	
t_{ASTART}	Device start-up time	AVDD step from 0 to 3.0 V with DVDD ≥ 2.7 V to bitstream valid, 0.1% settling		0.25		ms

6.11 Timing Diagrams

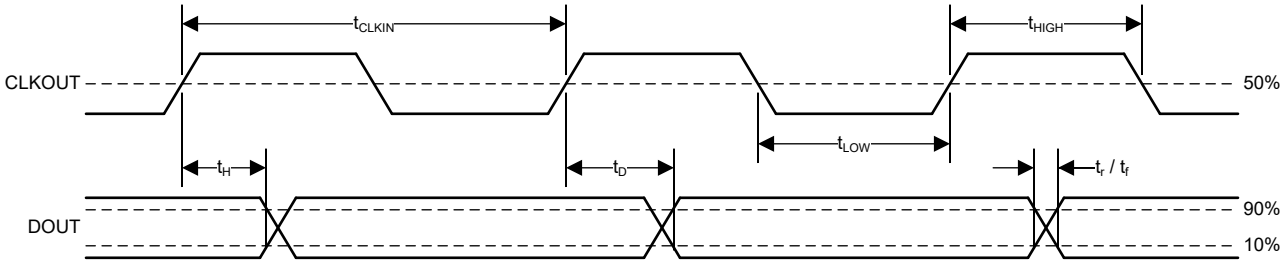


図 6-1. Digital Interface Timing

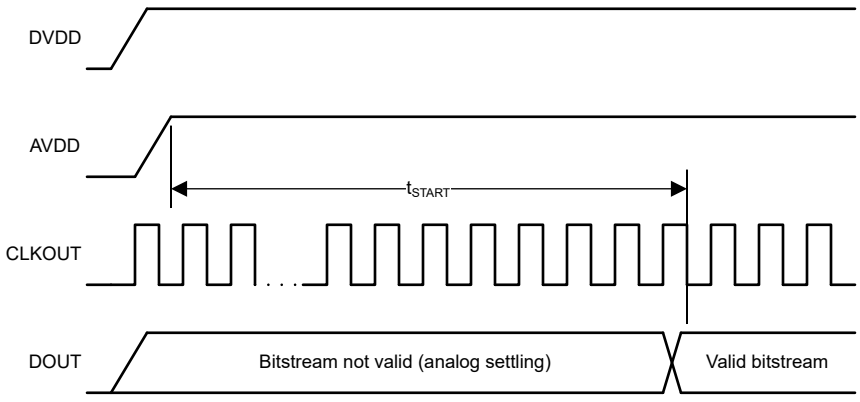


図 6-2. Device Start-Up Timing

6.12 Insulation Characteristics Curves

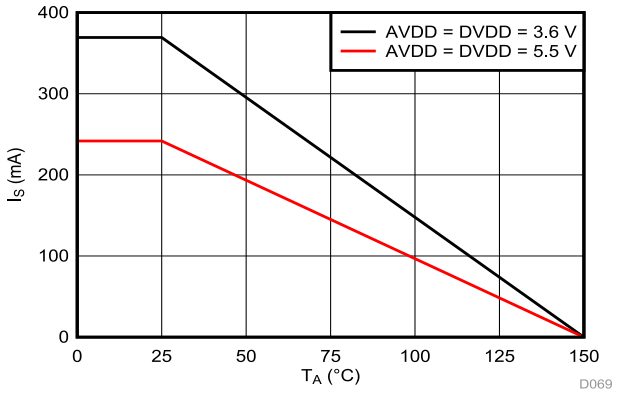


図 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE

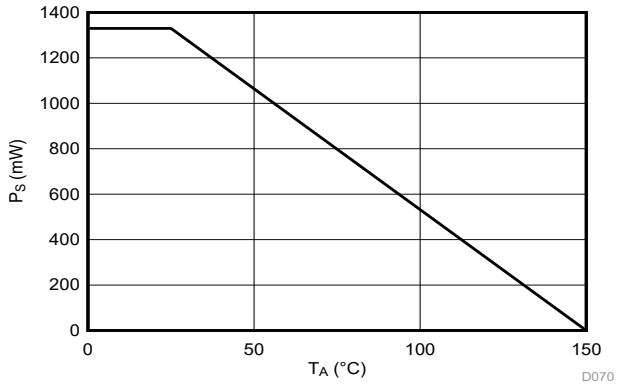
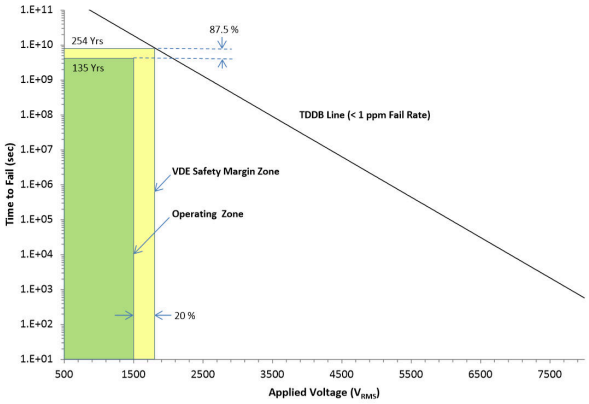


図 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE

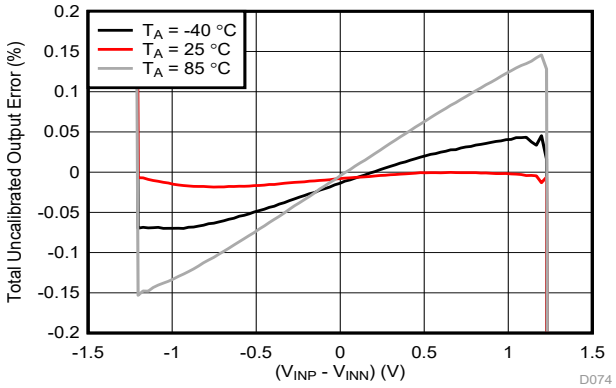


T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

図 6-5. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

at AVDD = 5 V, DVDD = 3.3 V, INP = –1 V to 1 V, INN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)



Total uncalibrated output error (in %) is defined as:
(Output Code / 2^{16}) – (V_{IN} + 1.25 V) / 2.5 V) × 100,
where V_{IN} = (V_{INP} – V_{INN})

図 6-6. Total Uncalibrated Output Error vs Input Voltage

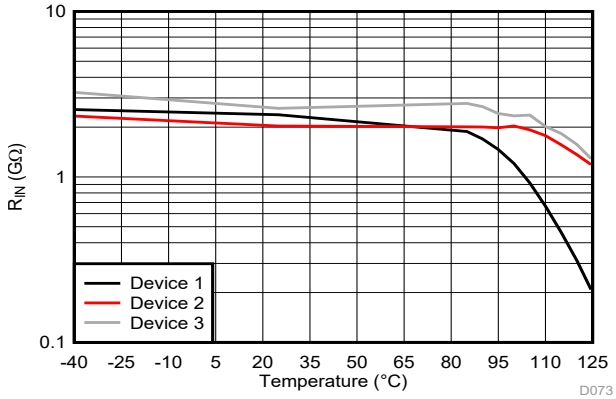


図 6-7. Single-Ended Input Resistance vs Temperature

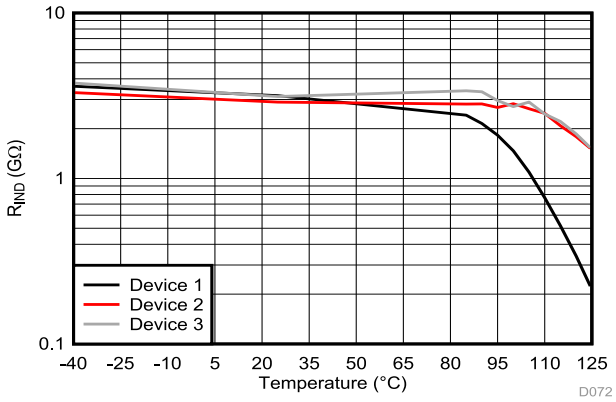


図 6-8. Differential Input Resistance vs Temperature

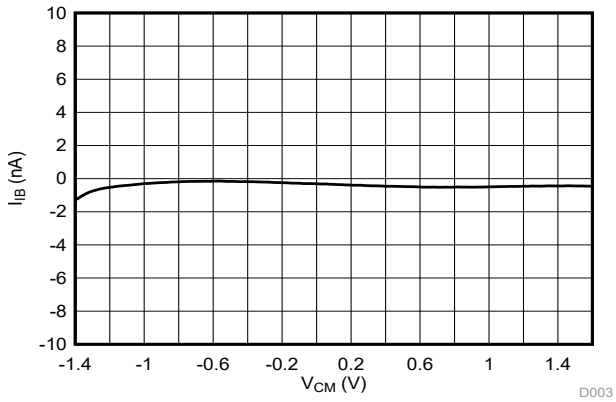


図 6-9. Input Bias Current vs Common-Mode Input Voltage

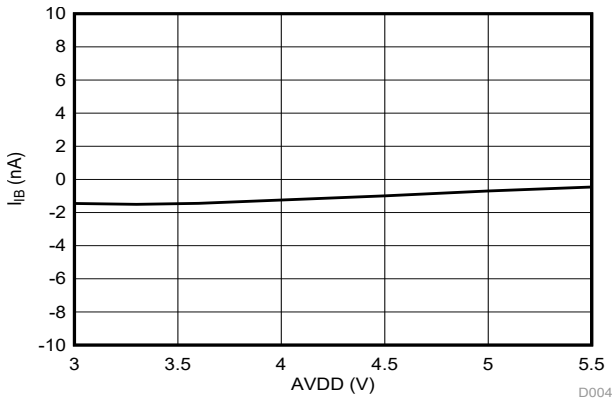


図 6-10. Input Bias Current vs High-Side Supply Voltage

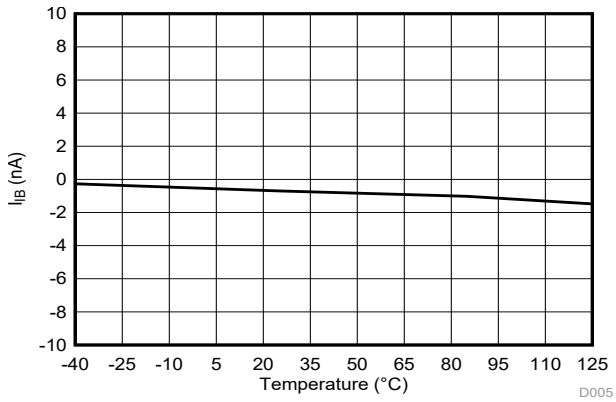


図 6-11. Input Bias Current vs Temperature

6.13 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = –1 V to 1 V, INN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)

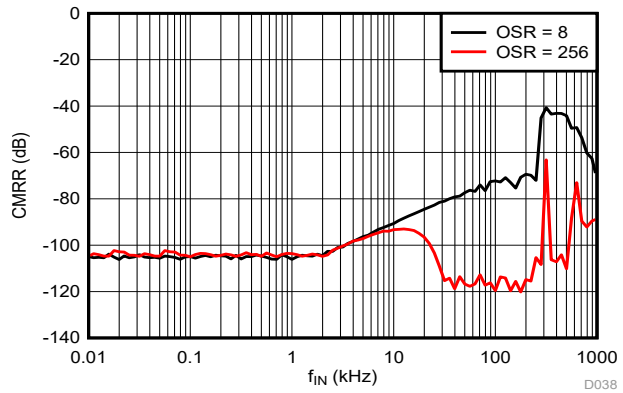


図 6-12. Common-Mode Rejection Ratio vs Ripple Frequency

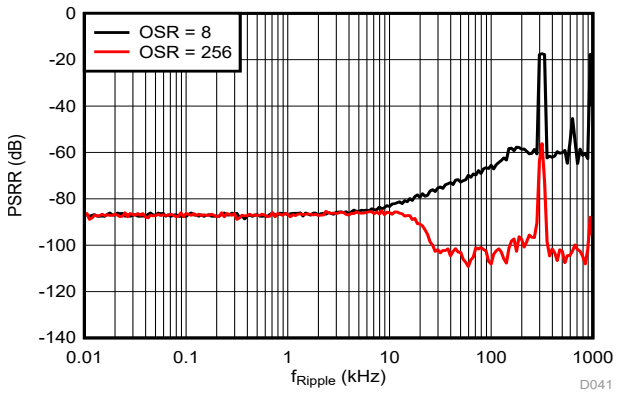


図 6-13. Power-Supply Rejection Ratio vs Ripple Frequency

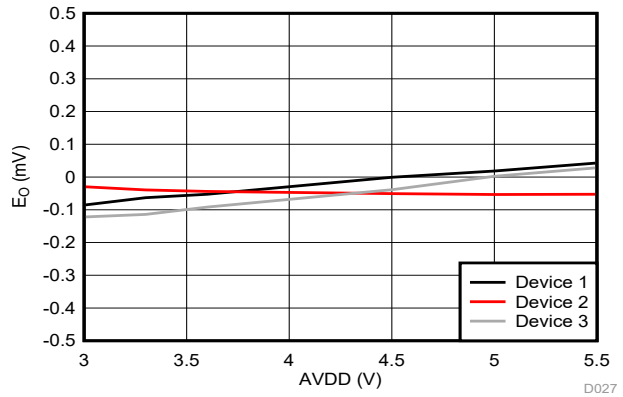


図 6-14. Offset Error vs High-Side Supply Voltage

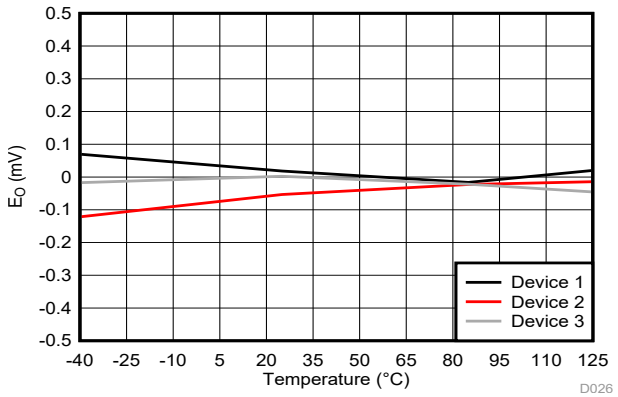


図 6-15. Offset Error vs Temperature

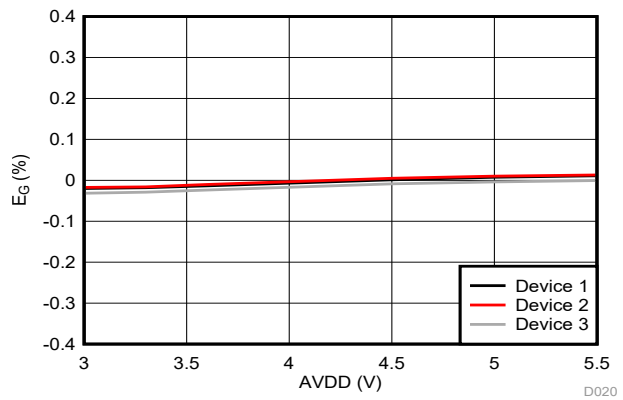


図 6-16. Gain Error vs High-Side Supply Voltage

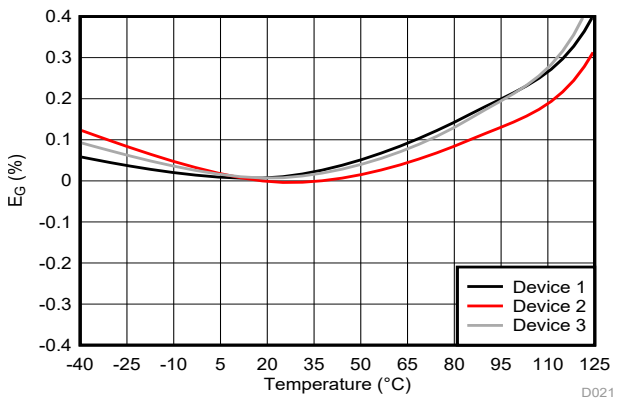


図 6-17. Gain Error vs Temperature

6.13 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = –1 V to 1 V, INN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)

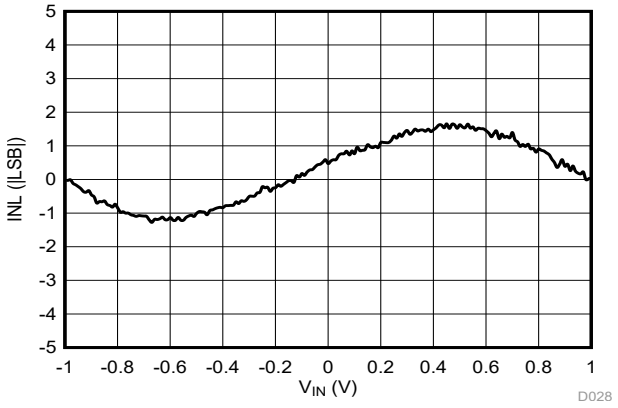


図 6-18. Integral Nonlinearity vs Input Voltage

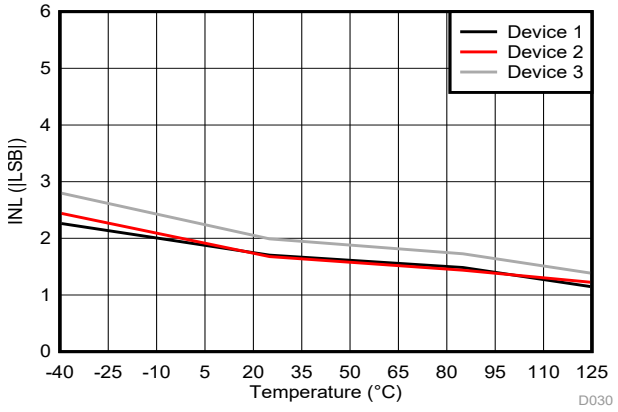


図 6-19. Integral Nonlinearity vs Temperature

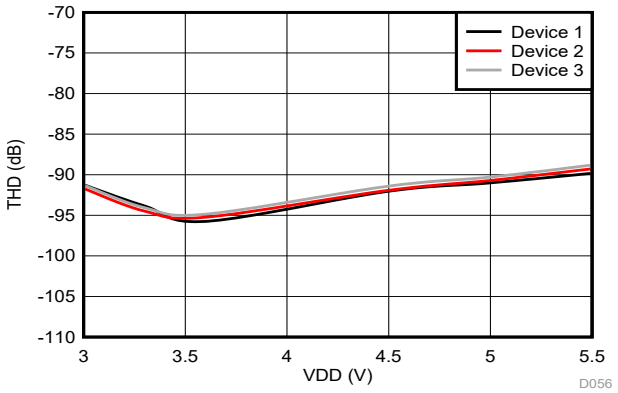


図 6-20. Total Harmonic Distortion vs High-Side Supply Voltage

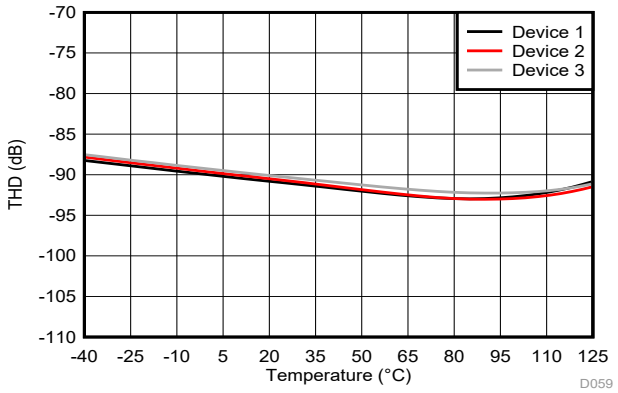


図 6-21. Total Harmonic Distortion vs Temperature

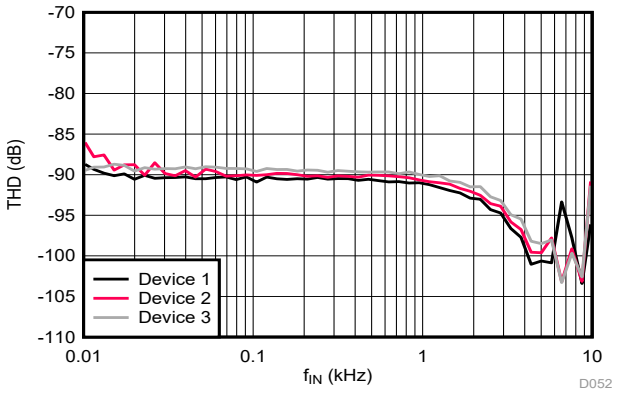


図 6-22. Total Harmonic Distortion vs Input Signal Frequency

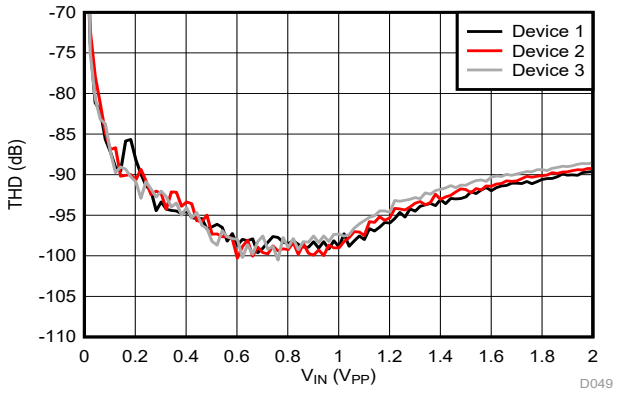
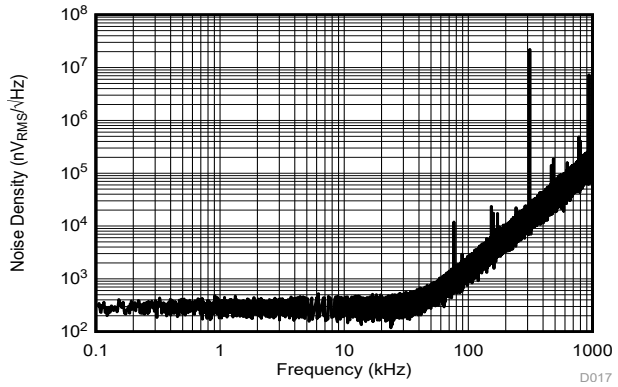


図 6-23. Total Harmonic Distortion vs Input Signal Amplitude

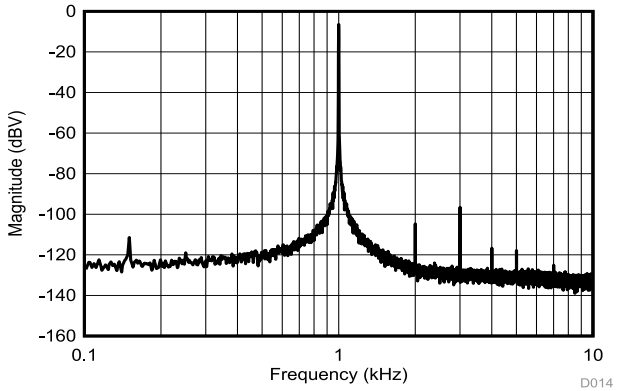
6.13 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, INP = –1 V to 1 V, INN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)



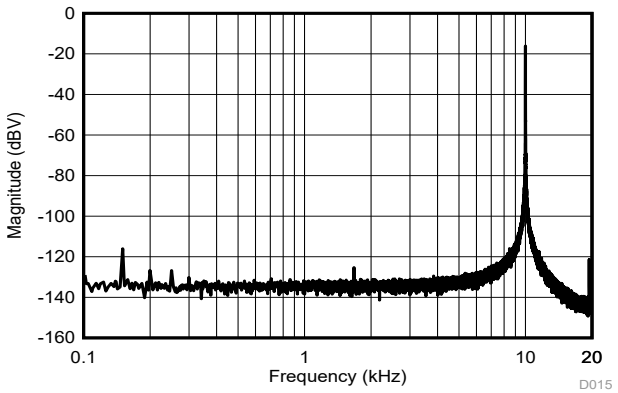
sinc^3, OSR = 1, frequency bin width = 1 Hz

図 6-24. Noise Density With Both Inputs Shorted to HGND



sinc^3, OSR = 256, V_{IN} = 2 V_{PP}

図 6-25. Frequency Spectrum With 1-kHz Input Signal



sinc^3, OSR = 256, V_{IN} = 2 V_{PP}

図 6-26. Frequency Spectrum With 10-kHz Input Signal

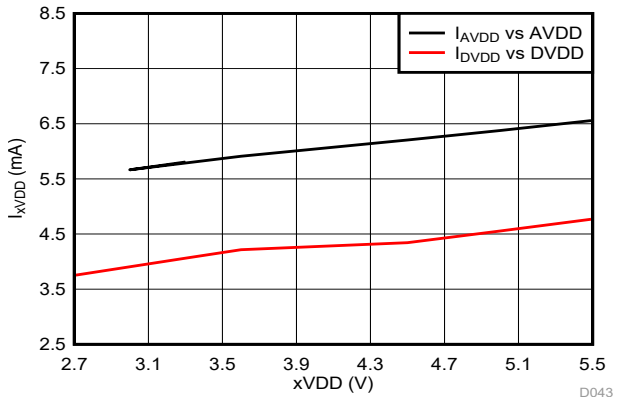


図 6-27. Supply Current vs Supply Voltage

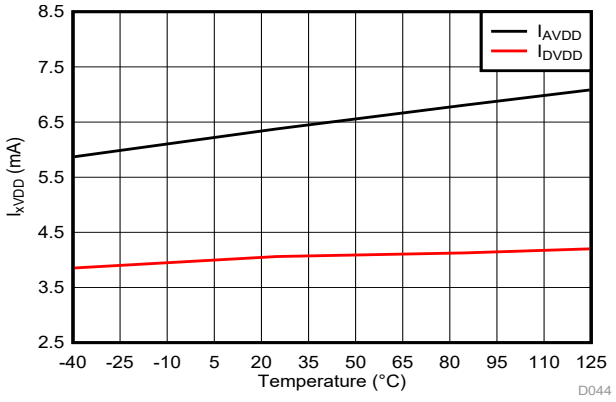


図 6-28. Supply Current vs Temperature

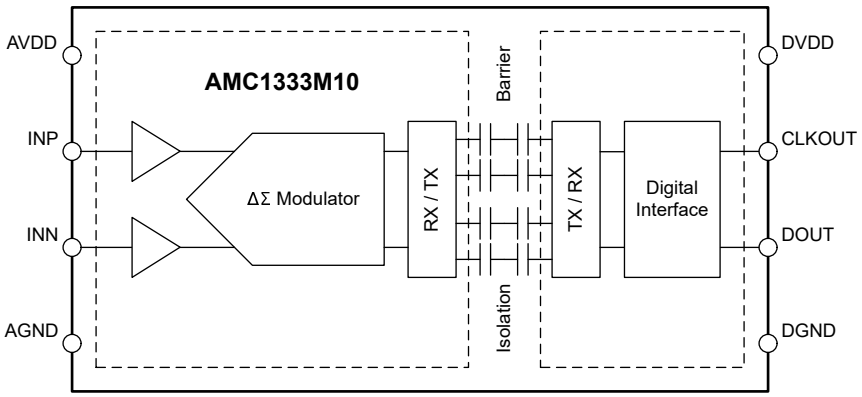
7 Detailed Description

7.1 Overview

The input stage of the AMC1333M10 consists of a fully differential amplifier that feeds the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. The isolated data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the internally generated clock source at the CLKOUT pin. The time average of this serial bitstream output is proportional to the analog input voltage.

The silicon-dioxide (SiO_2) based capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1333M10 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram

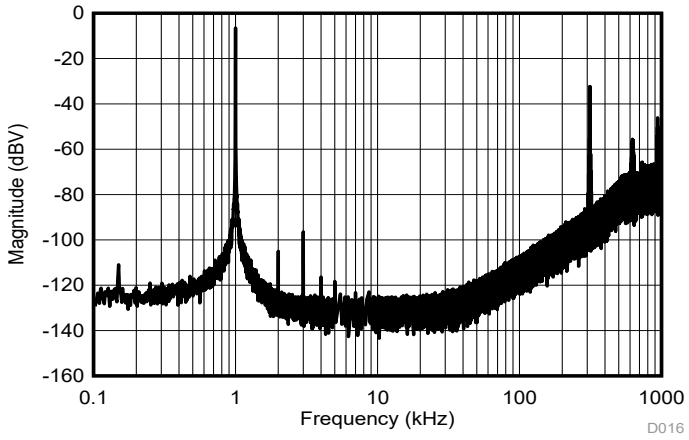


7.3 Feature Description

7.3.1 Analog Input

The high-impedance input stage of the AMC1333M10 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section. The high-impedance and low bias-current input makes the AMC1333M10 suitable for isolated, high-voltage-sensing applications that typically employ high-impedance resistor dividers.

For reduced offset and offset drift, the input buffer is chopper-stabilized with the chopping frequency set at f_{CLK} / 32. 図 7-1 shows the spur at 312.5 kHz that is generated by the chopping frequency for a modulator clock of 10 MHz.



sinc^3 filter, OSR = 1, f_{IN} = 1 kHz

図 7-1. Quantization Noise Shaping

There are two restrictions on the analog input signals (INP and INN). First, if the input voltage exceeds the input range specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. Second, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range V_{FSR} and within the specified input common-mode voltage range V_{CM}, as shown in 図 7-2 and as specified in the *Recommended Operating Conditions* table.

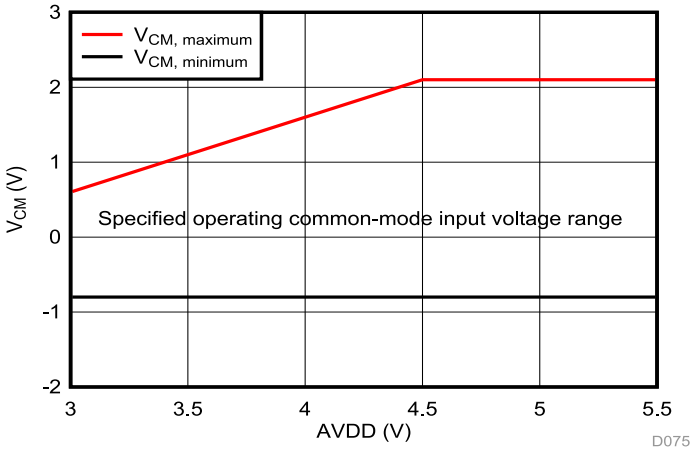


図 7-2. Common-Mode Input Voltage Range With a Differential Input Signal of ±1.25 V

7.3.2 Modulator

図 7-3 conceptualizes the second-order, switched-capacitor, feed-forward ΔΣ modulator implemented in the AMC1333M10. The output V_5 of the 1-bit, digital-to-analog converter (DAC) is subtracted from the input voltage $V_{IN} = (V_{INN} – V_{INP})$, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in an output voltage V_3 that is summed with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

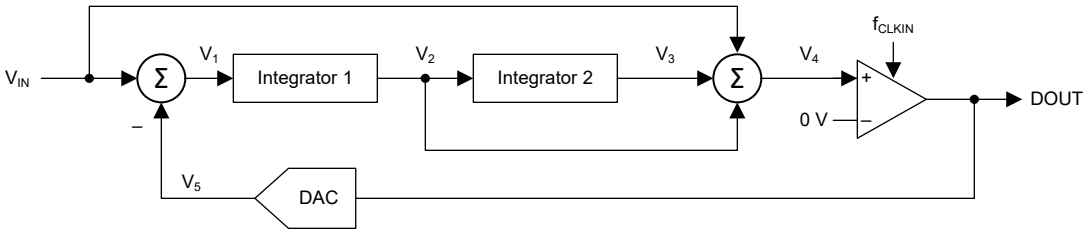


図 7-3. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as depicted in 図 7-1. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's C2000™ and Sitara™ microcontroller families offer a suitable programmable, hardwired filter structure, termed a *sigma-delta filter module* (SDFM), optimized for usage with the AMC1333M10. Alternatively, a field-programmable gate array (FPGA) or complex programmable logic device (CPLD) can be used to implement the filter.

7.3.3 Isolation Channel Signal Transmission

The AMC1333M10 uses an on-off keying (OOK) modulation scheme, as shown in 図 7-4, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) illustrated in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1333M10 is 480 MHz.

図 7-4 shows the concept of the on-off keying scheme.

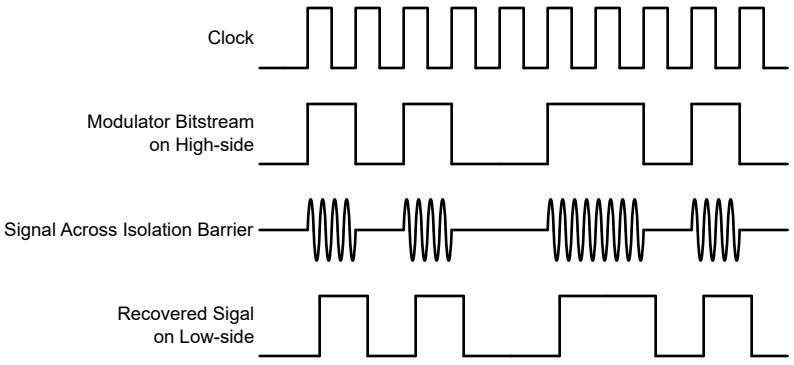


図 7-4. OOK-Based Modulation Scheme

7.3.4 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 1 V produces a stream of ones and zeros that are high 90% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982. A differential input of –1 V produces a stream of ones and zeros that are high 10% of the time and ideally results in code 6553 with 16-bit resolution. These input voltages are also the specified linear range of the AMC1333M10. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior as the quantization noise increases. The output of the modulator clips with a constant stream of zeros with an input less than or equal to –1.25 V, or with a constant stream of ones with an input greater than or equal to 1.25 V. In this case, however, the AMC1333M10 generates a single 1 (if the input is at negative full-scale) or 0 (if the input is at positive full-scale) every 128 clock cycles to indicate proper device function (see the *Output Behavior in Case of a Full-Scale Input* section for more details). 図 7-5 shows the input voltage versus the output modulator signal.

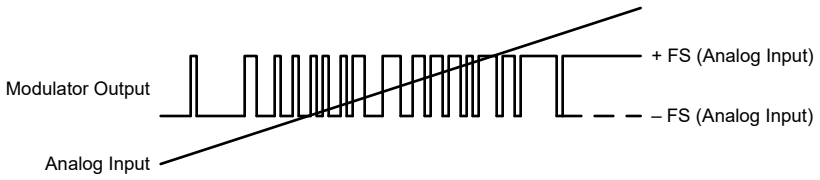


図 7-5. Modulator Output vs Analog Input

The density of ones in the output bitstream can be calculated using 式 1 for any input voltage ($V_{IN} = V_{INP} – V_{INN}$) value with the exception of a full-scale input signal, as described in *Output Behavior in Case of a Full-Scale Input*:

$$\rho = \frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

7.3.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1333M10 (that is, $|V_{IN}| \geq |V_{Clipping}|$), the device generates a single one or zero every 128 bits at DOUT, as shown in 図 7-6, depending on the actual polarity of the signal being sensed. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.

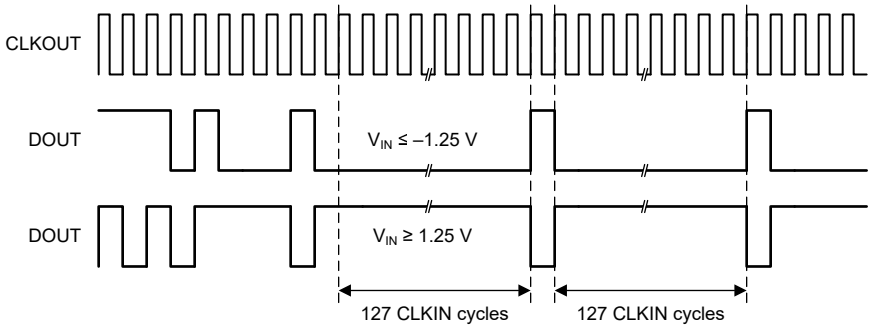


図 7-6. Full-Scale Output of the AMC1333M10

7.3.4.2 Output Behavior in Case of a Missing High-Side Supply

If the high-side supply is missing, the device provides a constant bitstream of logic 0's at the output, as shown in 図 7-7; that is, DOUT is permanently low. A one is not generated every 128 clock pulses, which differentiates this condition from a valid negative full-scale input. This feature is useful to identify high-side power-supply problems on the board.

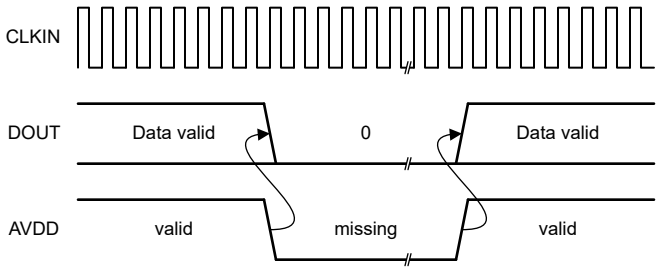


図 7-7. Output of the AMC1333M10 in Case of a Missing High-Side Supply

7.4 Device Functional Modes

The AMC1333M10 is operational when the power supplies AVDD and DVDD are applied as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The high input impedance, low input bias current, bipolar input voltage range, excellent accuracy, and low temperature drift make the AMC1333M10 a high-performance solution for industrial applications where isolated AC or DC voltage sensing is required.

8.2 Typical Application

Isolated modulators are widely used for voltage measurements in high-voltage applications that must be isolated from a low-voltage domain. Typical applications are AC line voltage measurements, either line-to-neutral or line-to-line in grid-connected equipment.

図 8-1 illustrates a simplified schematic of an AC motor drive application that uses three AMC1333M10 devices to measure the AC line voltage on each phase of a three-phase system. The AC line voltage is divided down to an approximate ±1-V level across the bottom resistor (RSNS) of a high-impedance resistive divider that is sensed by the AMC1333M10. The digital output of the AMC1333M10 is galvanically isolated from the input and processed by a digital sigma-delta filter module (SDFM) inside the TMS320F28x7x microcontroller on the low-voltage side of the system. A common high-side power supply (AVDD) for all three AMC1333M10 devices is generated from the low-side supply (DVDD) of the system by an isolated DC/DC converter circuit. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The high-impedance input, high input voltage range, and the high common-mode transient immunity (CMTI) of the AMC1333M10 ensure reliable and accurate operation even in high-noise environments.

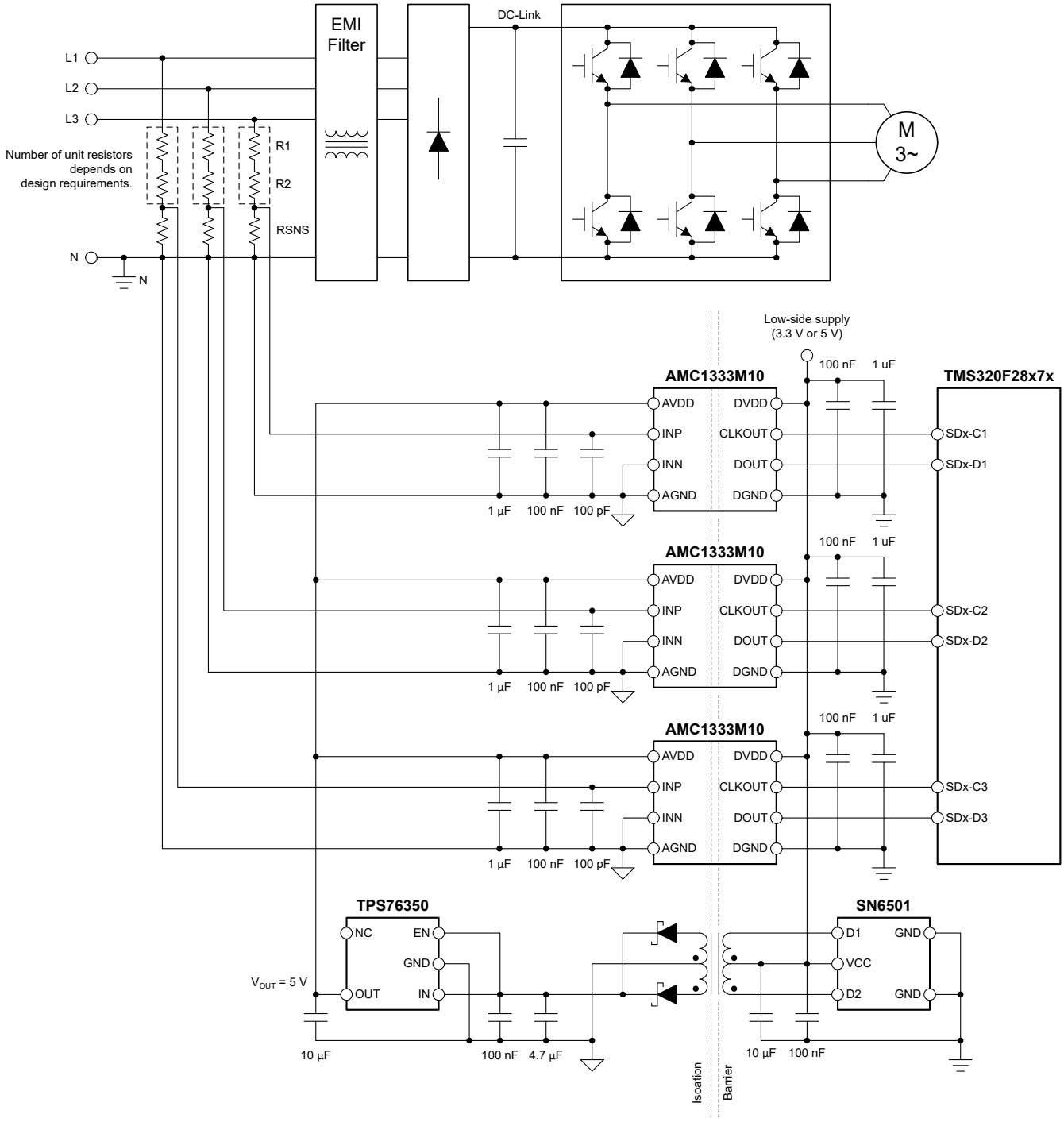


図 8-1. Using the AMC1333M10 for AC Line-Voltage Sensing in an AC Motor Drive Application

8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	120-V_{RMS} LINE VOLTAGE	230-V_{RMS} LINE VOLTAGE
System input voltage	120 V ±10%, 60 Hz	230 V ±10%, 50 Hz
High-side supply voltage	3.3 V or 5 V	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V	3.3 V or 5 V
Maximum resistor operating voltage	75 V	75 V
Voltage drop across the sense resistor (RSNS) for a linear response	±1 V (maximum)	±1 V (maximum)
Current through the resistive divider, I_{CROSS}	100 µA	100 µA

8.2.2 Detailed Design Procedure

This discussion covers the 230-V_{RMS} example. The procedure for calculating the resistive divider for the 120-V_{RMS} use case is identical.

The 100-µA, cross-current requirement at peak input voltage (360 V) determines that the total impedance of the resistive divider is 3.6 MΩ. The impedance of the resistive divider is dominated by the top resistors (shown exemplary as R1 and R2 in 図 8-1) and the voltage drop across RSNS can be neglected for a short time. The maximum allowed voltage drop per unit resistor is specified as 75 V; therefore, the total minimum number of unit resistors in the top portion of the resistive divider is 360 V / 75 V = 5. The calculated unit value is 3.6 MΩ / 5 = 720 kΩ, and the next closest value from the E96 series is 715 kΩ.

The sense resistor value RSNS is sized such that the voltage drop across the impedance at maximum input voltage (360 V) equals the linear full-scale input voltage (V_{FSR}) of the AMC1333M10 (that is, +1 V). RSNS is calculated as RSNS = V_{FSR} / (V_{Peak} – V_{FSR}) × R_{TOP}, where R_{TOP} is the total value of the top resistor string (5 × 715 kΩ = 3575 kΩ). The resulting value for RSNS is 10.04 kΩ, and the next closest value from the E96 series is 10.0 kΩ.

表 8-2 summarizes the design of the resistive divider.

表 8-2. Resistor Value Examples

PARAMETER	120-V_{RMS} LINE VOLTAGE	230-V_{RMS} LINE VOLTAGE
Peak voltage	190 V	360 V
Unit resistor value, R_{TOP}	634 kΩ	715 kΩ
Number of unit resistors in R_{TOP}	3	5
Sense resistor value, RSNS	10.2kΩ	10.0 kΩ
Total resistance value (R_{TOP} + RSNS)	1912.2 kΩ	3885.0 kΩ
Resulting current through resistive divider, I_{CROSS}	99.4 µA	100.4 µA
Resulting full-scale voltage drop across sense resistor RSNS	1.013 V	1.004 V
Peak power dissipated in R_{TOP} unit resistor	6.3 mW	7.2 mW
Total peak power dissipated in resistive divider	18.9 mW	36.2 mW

8.2.2.1 Input Filter Design

Placing an RC filter in front of the isolated modulator improves signal-to-noise performance of the signal path. In practice, however, the impedance of the resistor divider is high and only a small value filter capacitor can be used not to limit the signal bandwidth to an unacceptable low value. Design the input filter such that the cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (10 MHz) of the internal ΔΣ modulator.

Most voltage-sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In this case, an additional resistor is not required and a single capacitor (as shown in 図 8-2) is sufficient to filter the input signal.

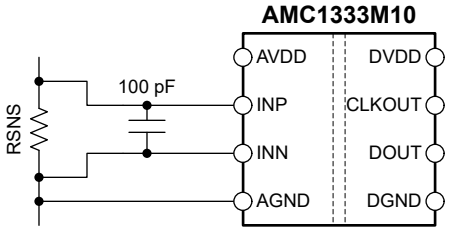


図 8-2. Input Filter

8.2.2.2 Bitstream Filtering

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). 式 2 shows a $sinc^3$-type filter, which is a very simple filter that is built with minimal effort and hardware.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is also done with a $sinc^3$ filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

An example code for implementing a $sinc^3$ filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

For modulator output bitstream filtering, a device from TI's C2000 or Sitara microcontroller families is recommended. These families support multichannel dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one path provides high-accuracy results for the control loop and the other provides a fast-response path for overcurrent detection.

A *delta sigma modulator filter calculator* is available for download at www.ti.com that aids in the filter design and selecting the right OSR and filter order to achieve the desired output resolution and filter response time.

8.2.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. 図 8-3 shows the ENOB of the AMC1333M10 with different oversampling ratios.

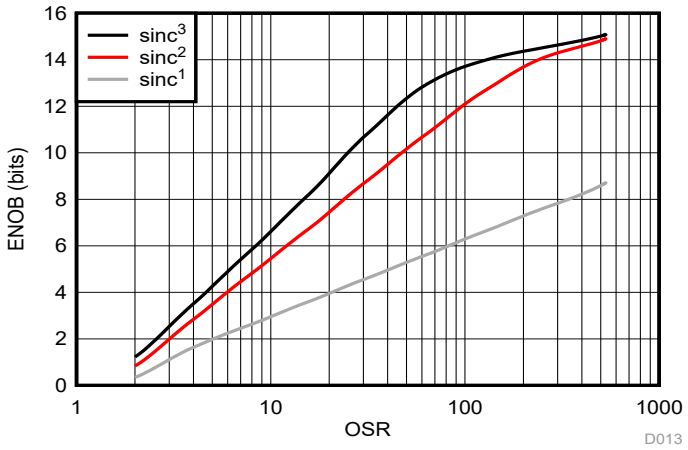


図 8-3. Measured Effective Number of Bits vs Oversampling Ratio

8.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1333M10 unconnected (floating) when the device is powered up. If either modulator input is left floating, the input bias current can drive this input beyond the specified common-mode input voltage range. If both inputs are beyond that range, the gain of the front-end diminishes and the output bitstream is not valid.

Connect the high-side ground (AGND) to INN, either by a hard short or through a resistive path. A DC current path between INN and AGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range, as specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the sense resistor rather than shorting AGND to INN directly at the input to the device. See the *Layout* section for more details.

Do not connect protection diodes to the inputs (INP or INN) of the AMC1333M10. Diode leakage current can introduce significant measurement error especially at high temperatures. The input pin is protected against high voltages by its ESD protection circuit and the high impedance of the external restive divider.

9 Power Supply Recommendations

In a typical application, the high-side power supply (AVDD) for the AMC1333M10 is generated from the low-side supply (DVDD) by an isolated DC/DC converter. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC1333M10 does not require any specific power-up sequencing. The high-side power supply (AVDD) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-µF capacitor (C2). The low-side power supply (DVDD) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. 図 9-1 shows a decoupling diagram for the AMC1333M10.

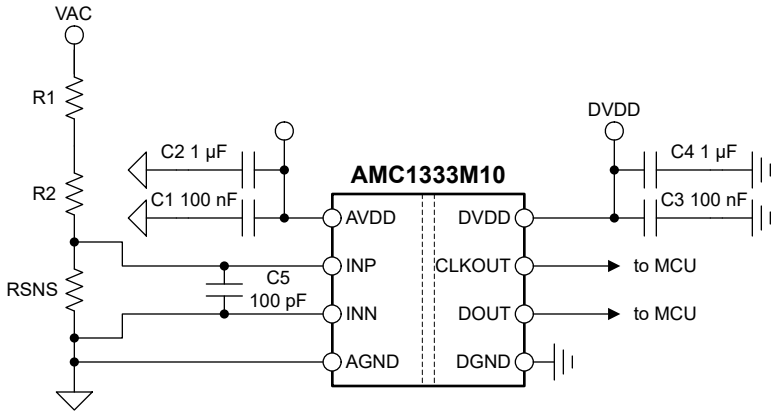


図 9-1. Decoupling of the AMC1333M10

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

10 Layout

10.1 Layout Guidelines

図 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1333M10 supply pins) and placement of the other components required by the device. For best performance, place the sense resistor close to the device input pins (INN and INP).

10.2 Layout Example

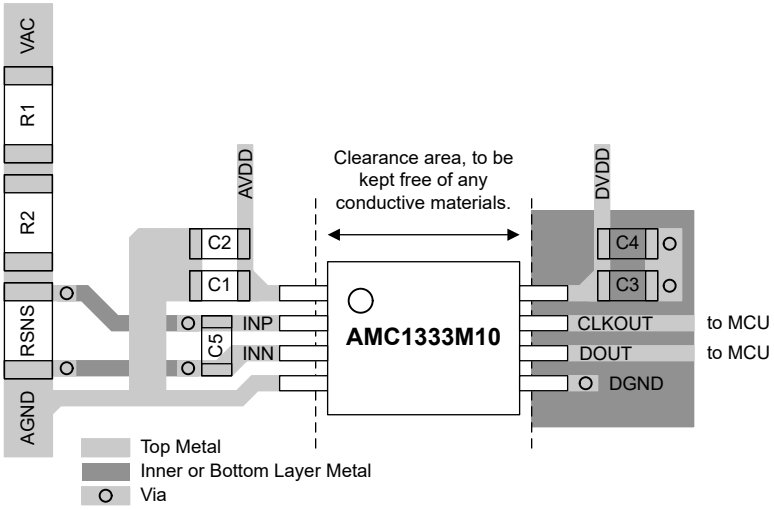


図 10-1. Recommended Layout of the AMC1333M10

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *TMS320F28004x Piccolo™ Microcontrollers* data sheet
- Texas Instruments, *TMS320F2807x Piccolo™ Microcontrollers* data sheet
- Texas Instruments, *TMS320F2837xD Dual-Core Delfino™ Microcontrollers* data sheet
- Texas Instruments, *TPS763 Low-Power, 150-mA, Low-Dropout Linear Regulator* data sheet
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity*
- Texas Instruments, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application report
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *Delta Sigma Modulator Filter Calculator* design tool

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1333M10DWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1333M10	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

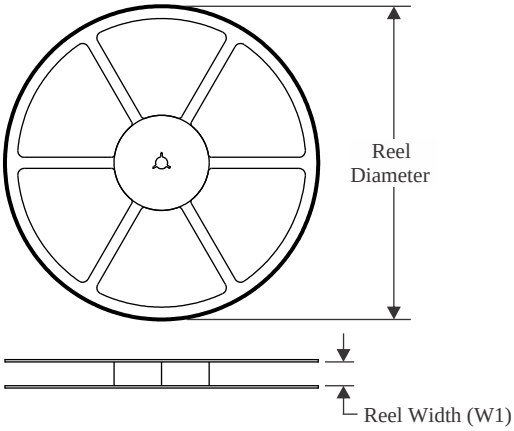
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

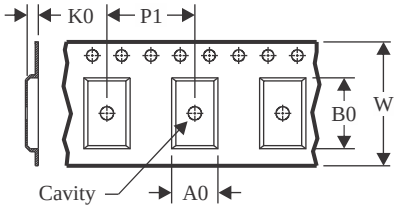
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

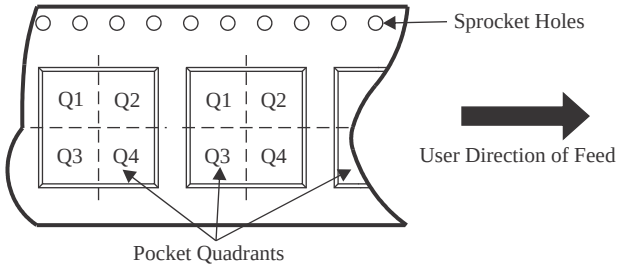


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

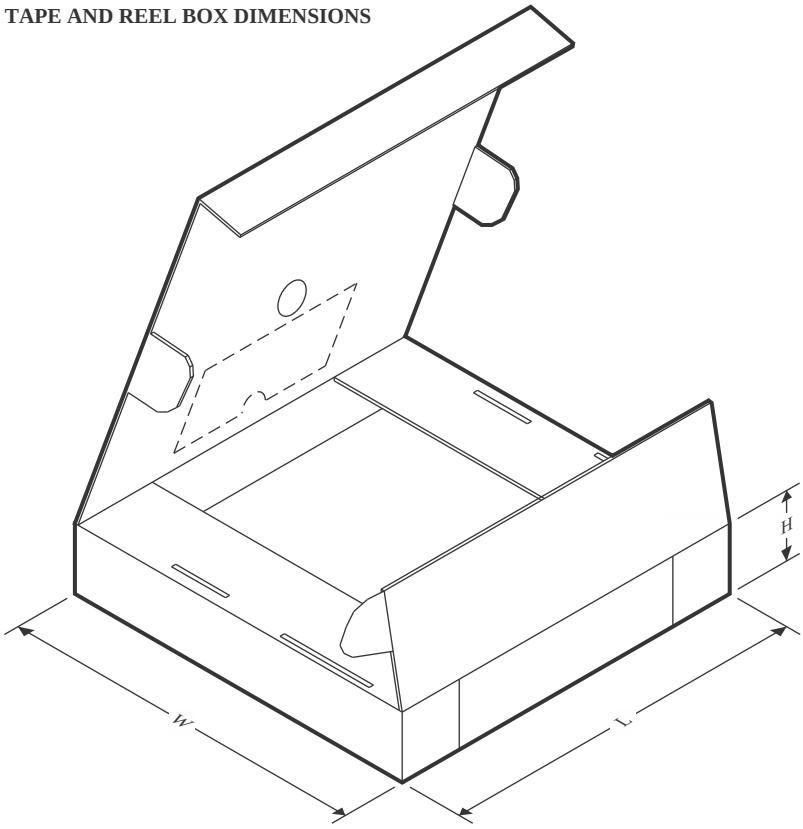
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

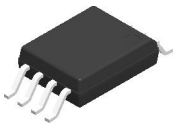
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1333M10DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

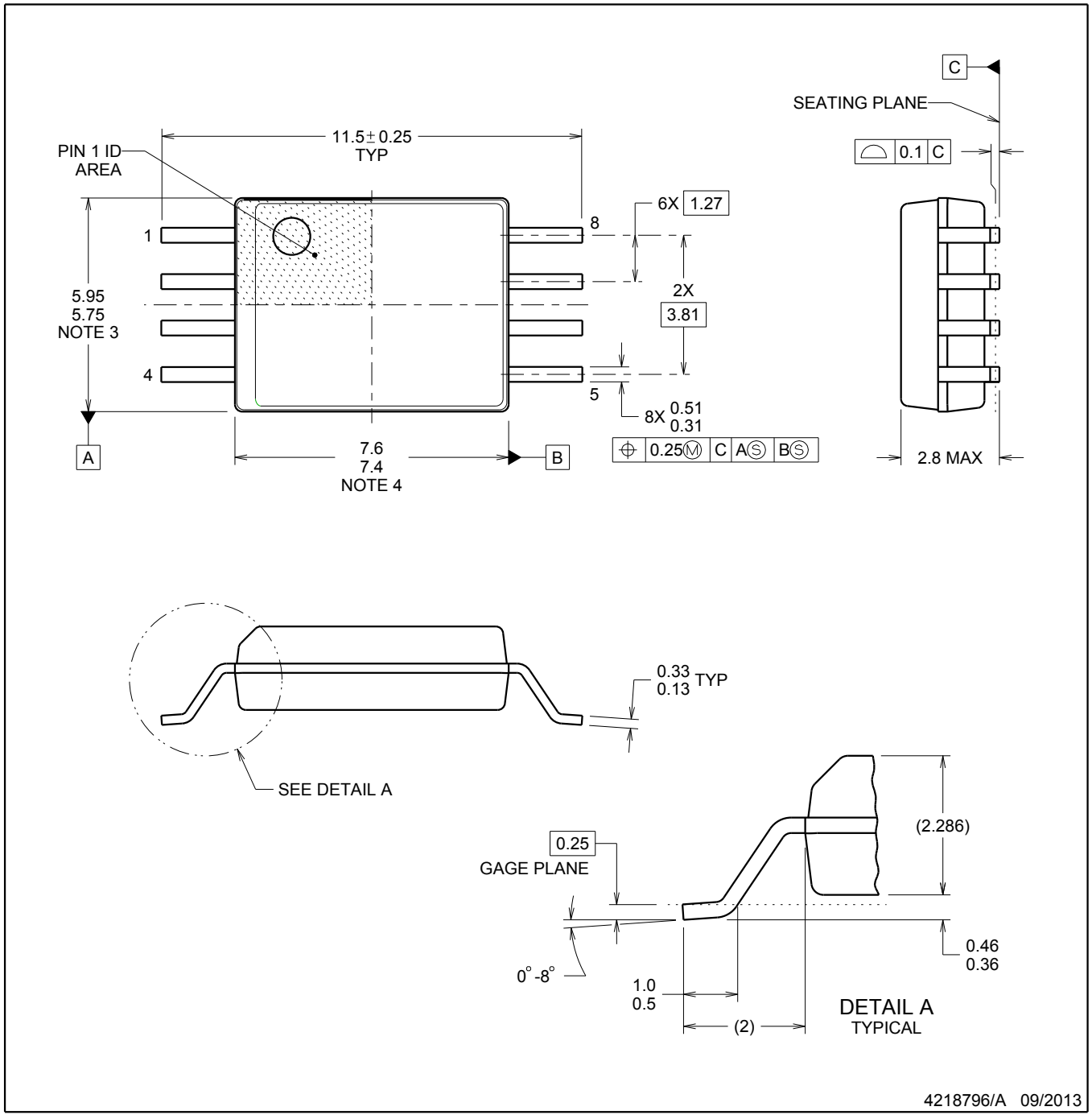
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1333M10DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0



DWV0008A

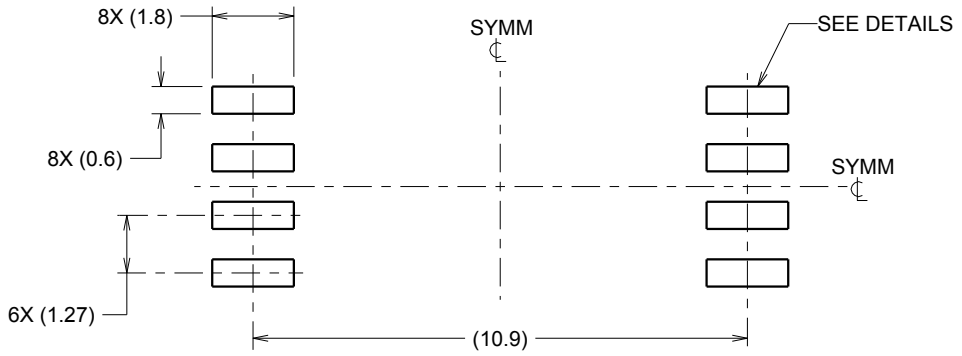
SOIC - 2.8 mm max height

SOIC

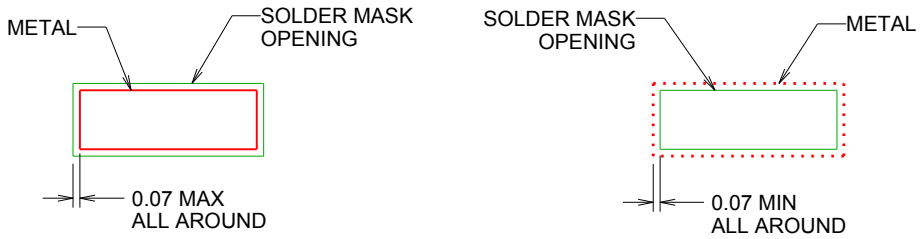


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

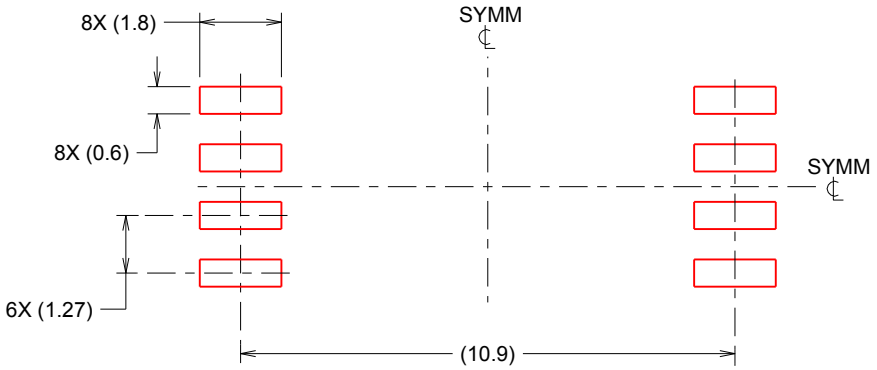
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265