AMC0386-Q1 車載用、高精度、高電圧入力、強化絶縁型の、外部クロックによるデルタ シグマ変調器

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～125℃、T_A
- 外付け抵抗なしで AC または DC 電圧を直接検出できる内蔵高電圧抵抗分圧器
- システムレベルのキャリブレーションなしで、温度範囲と寿命全体にわたって 1% 未満の高精度
- 電源電圧範囲:
  - ハイサイド (AVDD):3.0V～5.5V
  - ローサイド (DVDD):2.7V～5.5V
- 小さい DC 誤差:
  - オフセット誤差:±0.9mV (最大値)
  - オフセット ドリフト:±7µV/°C (最大値)
  - 減衰誤差:±0.25% (最大値)
  - 減衰ドリフト:±40ppm/°C (最大値)
- 「高 CMTI:100V/ns (最小値)
- ハイサイド電源喪失の検出
- 低 EMI:CISPR-11 および CISPR-25 規制に準拠
- 利用可能な入力オプション:
  - AMC0386M04-Q1:400V、8MΩ
  - AMC0386M06-Q1: 600V、10MΩ
  - AMC0386M10-Q1: 1000V、12.5MΩ
- 低 EMI:CISPR-11 および CISPR-25 規格に準拠
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧:7000V_{PK}
  - UL 1577 に準拠した絶縁耐圧:5000V_{RMS} (1 分間)

2 アプリケーション

- トラクション インバータ
- オンボード チャージャ
- DC/DC コンバータ
- バッテリ ジャンクション ボックス

3 概要

AMC0386-Q1 は、高電圧、高インピーダンス入力、外部クロックのガルバニック絶縁された高精度のデルタ シグマ (ΔΣ) 変調器です。入力は、高電圧信号源に直接接続できる設計を採用しています。

この絶縁バリアは、異なる同相電圧レベルで動作するシステム領域を分離します。絶縁バリアは、磁気干渉に対して高い耐性があり、最大 5kV_{RMS} (60s) の強化絶縁を実現することが認証されています。

AMC0386-Q1 の出力ビットストリームは、外部クロックと同期します。このデバイスは、sinc3 や OSR 256 フィルタと組み合わせることにより、16 ビットの分解能、84dB のダイナミック レンジ、39kSPS のデータ レートを実現します。

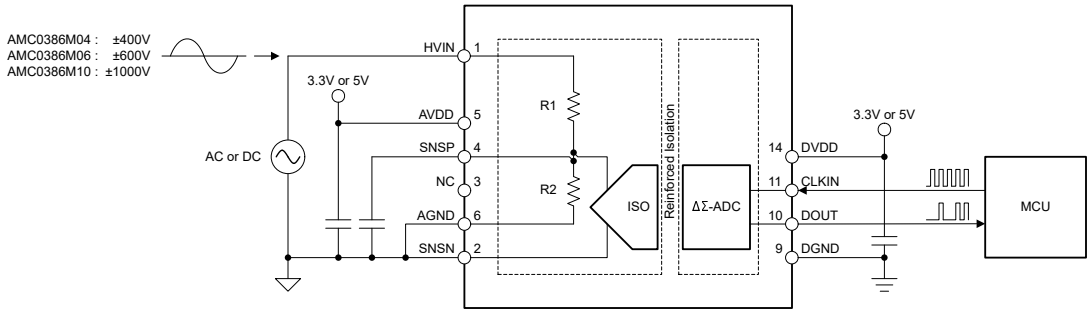
AMC0386-Q1 は、その内蔵抵抗分圧器、非常に高い DC 精度、低い温度ドリフト、高い安定性により、システムレベルのキャリブレーションなしに、寿命および温度範囲全にわたって 1% 未満の高精度を実現します。

AMC0386-Q1 は 15 ピン、0.65mm ピッチの SSOP パッケージで供給され、-40℃～+125℃ の温度範囲で完全に動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
AMC0386-Q1	DFX (SSOP、15)	12.8mm × 10.3mm

(1) 詳細については、付録「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

Device Comparison Table

表 4-1. Device Comparison

DEVICE	R1	R2	DIVIDER RATIO	LINEAR INPUT RANGE	CLIPPING VOLTAGE	ABS MAX INPUT VOLTAGE
AMC0386M04-Q1 (1)	8MΩ	20kΩ	401:1	400V	513V	600V
AMC0386M06-Q1 (1)	10MΩ	16.6kΩ	601:1	600V	769V	900V
AMC0386M10-Q1	12.5MΩ	12.5kΩ	1001:1	1000V	1281V	1500V

(1) PODUCT PREVIEW

ADVANCE INFORMATION

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4 Pin Configuration and Functions

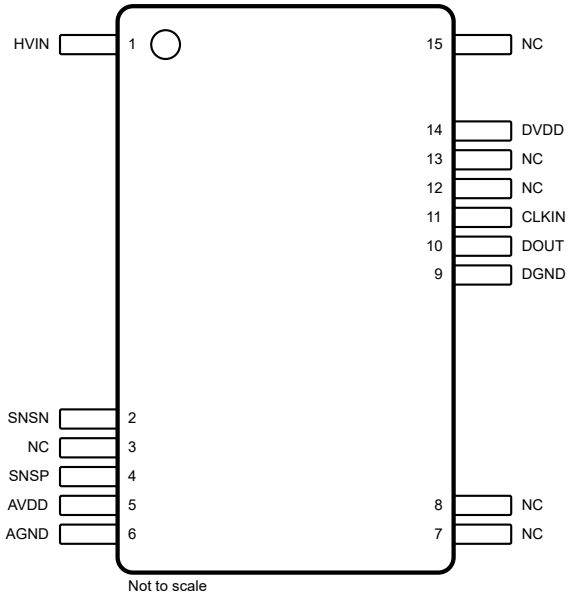


図 4-1. DWV および D パッケージ, 15 ピン SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	HVIN	Analog input	High-voltage input
2	SNSN	Analog input	Ground sense pin and inverting analog input to the modulator. Connect to AGND.
3, 7, 8, 12, 13, 15	NC	N/A	No internal connection. Pin can be connected to any potential or left floating.
4	SNSP	Analog I/O	Sense voltage pin and noninverting analog input to the modulator. Connect to an external filter capacitor or leave floating.
5	AVDD	High-side power	Analog (high-side) power supply(1)
6	AGND	High-side ground	Analog (high-side) ground
9	DGND	Low-side ground	Digital (low-side) ground
10	DOUT	Digital output	Modulator data output
11	CLKIN	Digital input	Modulator clock input with internal, 1.5MΩ pulldown resistor
14	DVDD	Low-side power	Digital (low-side) power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

5 Specifications

5.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side, AVDD to AGND	–0.3	6.5	V
	Low-side, DVDD to DGND	–0.3	6.5	
Analog input voltage	HVIN to AGND, AMC0386M04-Q1	–600	600	V
	HVIN to AGND, AMC0386M06-Q1	–900	900	
	HVIN to AGND, AMC0386M10-Q1	–1500	1500	
	SNSP, SNSN	AGND – 1.5	AVDD + 0.5	
Digital input voltage	CLKIN	DGND – 0.5	DVDD + 0.5	V
Digital output voltage	DOUT	DGND – 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply and HVIN pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ADVANCE INFORMATION

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Hgh-side power supply	AVDD to AGND	3	5.0	5.5	V
DVDD	Low-side power supply	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Nominal input voltage before clipping output	Referred to SNSP	–1.28		1.28	V
		Referred to HVIN, AMC0386M04-Q1	–513		513	
		Referred to HVIN, AMC0386M06-Q1	–769		769	
		Referred to HVIN, AMC0386M10-Q1	–1281		1281	
V_{FSR}	Specified linear input voltage	Referred to SNSP	–1		1	V
		Referred to HVIN, AMC0386M04-Q1	–400		400	
		Referred to HVIN, AMC0386M06-Q1	–600		600	
		Referred to HVIN, AMC0386M10-Q1	–1000		1000	
V_{IO}	Digital input/output voltage		0		DVDD	V
f_{CLKIN}	Input clock frequency		5	10	11	MHz
t_{HIGH}	Input clock high time		22.5	50	177.5	ns
t_{LOW}	Input clock low time		21.5	50	177.5	ns
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

ADVANCE INFORMATION

5.4 Thermal Information

THERMAL METRIC(1)		DFX (SSOP)	UNIT
		15 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5V, $V_{HVIN} = V_{Clipping}$ AMC0386M04-Q1	129	
		AVDD = DVDD = 5.5V, $V_{HVIN} = V_{Clipping}$ AMC0386M06-Q1	154	
		AVDD = DVDD = 5.5V, $V_{HVIN} = V_{Clipping}$ AMC0386M10-Q1	222	mW
P_{D1}	Maximum power dissipation (high-side)	AVDD = 5.5V, $V_{HVIN} = V_{Clipping}$ AMC0386M04-Q1	101	mW
		AVDD = 5.5V, $V_{HVIN} = V_{Clipping}$ AMC0386M06-Q1	126	
		AVDD = 5.5V, $V_{HVIN} = V_{Clipping}$ AMC0386M10-Q1	194	
P_{D2}	Maximum power dissipation (low-side)	DVDD = 5.5V	28	mW

ADVANCE INFORMATION

5.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 9.2	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I-III	
		Rated mains voltage ≤ 1000V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1410	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1000	V_{RMS}
		At DC voltage	1410	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification test), V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)}$ = V_{IOTM}, t_{ini} = 60s, $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)}$ = V_{IOTM}, t_{ini} = 60s, $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)}$ = 1.2 x V_{IOTM}, t_{ini} = 1s, $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)}$ = $V_{pd(m)}$ = 1.2 × V_{IOTM}, t_{ini} = t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 V_{PP} at 1MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification test), V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

ADVANCE INFORMATION

5.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 107°C/W, AVDD = DVDD = 5.5V, V_{HVIN} = $V_{Clipping}$, T_J = 150°C, T_A = 25°C AMC0386M04-Q1			200	mA
		$R_{\theta JA}$ = 107°C/W, AVDD = DVDD = 5.5V, V_{HVIN} = $V_{Clipping}$, T_J = 150°C, T_A = 25°C AMC0386M06-Q1			200	
		$R_{\theta JA}$ = 107°C/W, AVDD = DVDD = 5.5V, V_{HVIN} = $V_{Clipping}$, T_J = 150°C, T_A = 25°C AMC0386M10-Q1			190	
P_S	Safety input, output, or total power				1170	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

ADVANCE INFORMATION

5.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, V_{SNSP} = –1 V to +1 V, and V_{SNSN} = 0V; typical specifications are at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and f_{CLKIN} = 10 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Input resistance	AMC0386M04-Q1	TBD	8	TBD	MΩ
		AMC0386M06-Q1	TBD	10	TBD	
		AMC0386M10-Q1	TBD	12.5	TBD	
	Nominal resistive divider ratio	V_{HVIN} / V_{SNSP}, AMC0386M04-Q1		401		
		V_{HVIN} / V_{SNSP}, AMC0386M06-Q1		601		
		V_{HVIN} / V_{SNSP}, AMC0386M10-Q1		1001		
CMTI	Common-mode transient immunity		100			V/ns
DC ACCURACY						
E_O	Input offset error	Referred to SNSP, T_A = 25°C, HVIN = AGND	–0.9	±0.08	0.9	mV
		Referred to HVIN, T_A = 25°C, HVIN = AGND AMC0386M04-Q1	–360	±30	200	
		Referred to HVIN, T_A = 25°C, HVIN = AGND AMC0386M06-Q1	–540	±50	300	
		Referred to HVIN, T_A = 25°C, HVIN = AGND AMC0386M10-Q1	–900	±80	900	
TCE_O	Offset error temperature drift(3)	Referred to SNSP, T_A = 25°C, HVIN = AGND	–0.004	±0.0006	0.004	mV/°C
		Referred to HVIN, HVIN = AGND AMC0386M04-Q1	–2.8	±1.4	2.8	
		Referred to HVIN, HVIN = AGND AMC0386M06-Q1	–4.2	±2.1	4.2	
		Referred to HVIN, HVIN = AGND AMC0386M10-Q1	–7	±3.5	7	
E_G	Gain error(1)	T_A = 25°C	–0.25	±0.02	0.25	%
TCE_G	Gain error temperature drift(4)		–40	±20	40	ppm/°C
INL	Integral nonlinearity(2)	Resolution: 16 bits	–4	±1.6	4	LSB
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
PSRR	Power-supply rejection ratio(5)	AVDD DC PSRR, HVIN = AGND, AVDD from 3.0V to 5.5V		83		dB
		AVDD AC PSRR, HVIN = AGND, AVDD with 10kHz / 100mV ripple		83		
AC ACCURACY						
SNR	Signal-to-noise ratio	V_{SNSP} = $2V_{PP}$, SNSN = AGND, f_{IN} = 1kHz	86	89		dB
SINAD	Signal-to-noise + distortion	V_{SNSP} = $2V_{PP}$, SNSN = AGND, f_{IN} = 1kHz	76	86		dB
THD	Total harmonic distortion	V_{SNSP} = $2V_{PP}$, SNSN = AGND, f_{IN} = 1kHz		–88	–77	dB
DIGITAL INPUT (CMOS Logic With Schmitt-Trigger)						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD			7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 x DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 x DVDD	V
DIGITAL OUTPUT (CMOS)						
C_{LOAD}	Output load capacitance	f_{CLKIN} = 10MHz		15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –4mA	DVDD – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA			0.4	V
POWER SUPPLY						
I_{AVDD}	High-side supply current			5.3	7.5	mA
I_{DVDD}	Low-side supply current	C_{LOAD} = 15pF		3.6	5.1	mA
$AVDD_{UV}$	High-side undervoltage detection threshold	AVDD rising	2.5	2.6	2.7	V
		AVDD falling	1.9	2.0	2.1	

ADVANCE INFORMATION

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, V_{SNSP} = –1 V to +1 V, and V_{SNSN} = 0V; typical specifications are at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and f_{CLKIN} = 10 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DVDD_{UV}$	Low-side undervoltage detection threshold	DVDD rising	2.5	2.6	2.7	V
		DVDD falling	1.9	2.0	2.1	

(1) The typical value includes one sigma statistical variation.
(2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(3) Offset error drift is calculated using the box method, as described by the following equation:
$TCE_O = (value_{MAX} - value_{MIN}) / TempRange$
(4) Gain error drift is calculated using the box method, as described by the following equation:
TCE_G (ppm) = $((value_{MAX} - value_{MIN}) / (value \times TempRange)) \times 10^6$
(5) This parameter is referred to SNSP.

ADVANCE INFORMATION

5.10 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_H	DOUT hold time after rising edge of CLKIN	C_{LOAD} = 15pF	10			ns
t_D	Rising edge of CLKIN to DOUT valid delay	C_{LOAD} = 15pF			35	ns
t_r	DOUT rise time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		2.5	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		3.2	6	
t_f	DOUT fall time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		2.2	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		2.9	6	
t_{START}	Device start-up time	AVDD step from 0 to 3.0V with AVDD ≥ 2.7V to bitstream valid, 0.1% settling		100		µs

5.11 Timing Diagrams

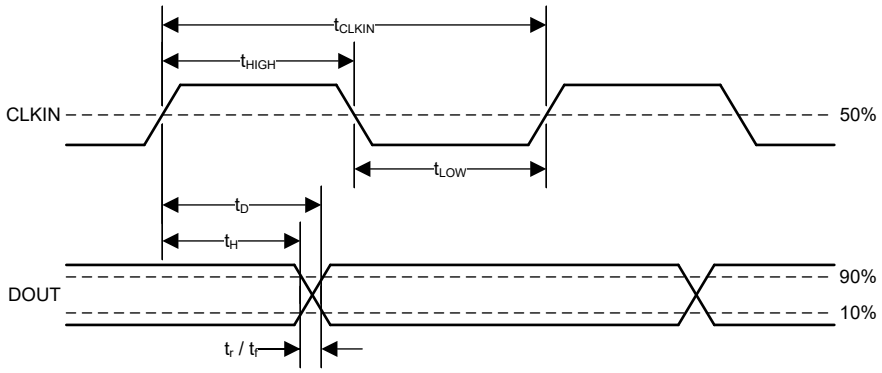


図 5-1. Digital Interface Timing

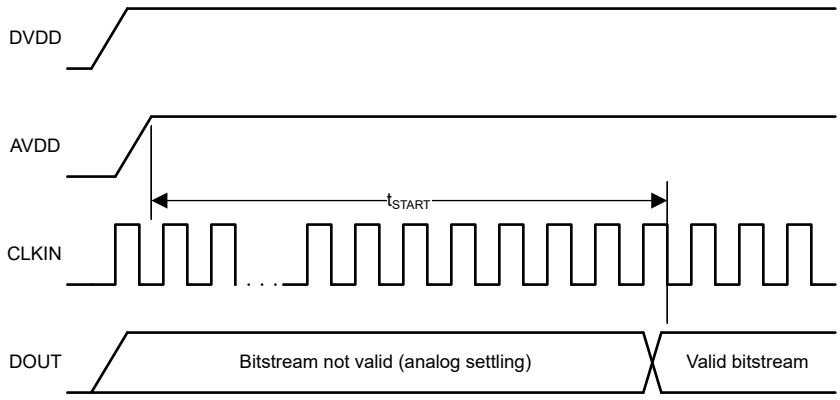


図 5-2. Device Start-Up Timing

ADVANCE INFORMATION

6 Detailed Description

6.1 Overview

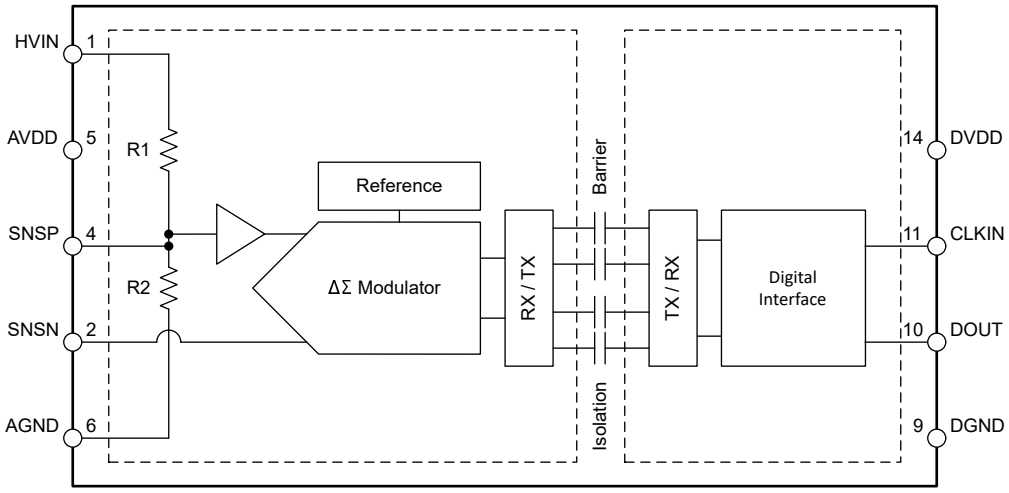
The AMC0386-Q1 is a single-channel, second-order, CMOS, delta-sigma (ΔΣ) modulator with 高電圧、高インピーダンス入力、外部クロック. The analog input of the AMC0386-Q1 is implemented with a switched-capacitor circuit. The isolated output of the converter (DOUT) provides a stream of digital ones and zeros synchronous to the external clock applied to the CLKIN pin. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies; therefore, use a digital low-pass digital filter, such as a Sinc filter at the device output to increase overall performance. This filter also converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). Use a microcontroller (μC) or field-programmable gate array (FPGA) to implement the filter.

The overall performance (speed and resolution) depends on the selection of an appropriate oversampling ratio (OSR) and filter type. A higher OSR results in higher resolution while operating at a lower refresh rate. A lower OSR results in lower resolution, but provides data at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of analog-to-digital conversion results with a dynamic range exceeding 84dB with OSR = 256.

The silicon-dioxide (SiO_2) based capacitive isolation barrier supports a high level of magnetic field immunity; see the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The AMC0386-Q1 uses an on-off keying (OOK) modulation scheme to transmit data across the isolation barrier. This modulation and the isolation barrier characteristics, result in high reliability in noisy environments and high common-mode transient immunity.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Input

The resistive divider at the input of the AMC0386-Q1 scales down the voltage applied to the HVIN pin to a ±1V linear fullscale level. This signal is available on the SNSP pin, which is also the input of the analog signal chain.

The input stage of the AMC0386-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

ADVANCE INFORMATION

6.3.2 Modulator

図 6-1 conceptualizes the second-order, switched-capacitor, feed-forward ΔΣ modulator implemented in the AMC0386-Q1. The output V_5 of the 1-bit, digital-to-analog converter (DAC) is subtracted from the input voltage $V_{IN} = (V_{SNSP} - V_{SNSN})$. This subtraction provides an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage. The result or the second integration is an output voltage V_3 that is summed with the input signal V_{IN} and the output of the first integrator V_2. Depending on the value of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5. Thus, causing the integrators to progress in the opposite direction and forcing the integrator output value to track the average value of the input.

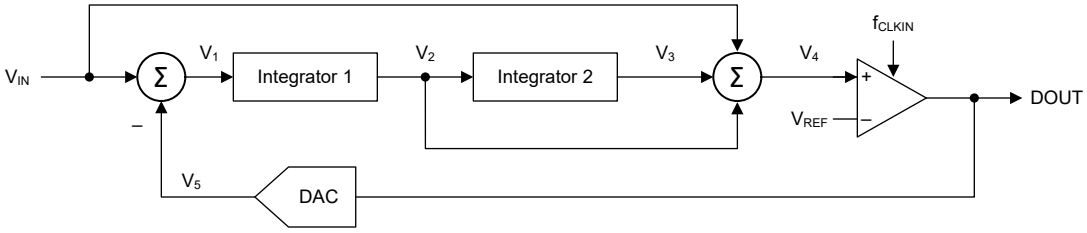


図 6-1. Block Diagram of a Second-Order Modulator

6.3.3 Isolation Channel Signal Transmission

The AMC0386-Q1 uses an on-off keying (OOK) modulation scheme, as shown in 図 6-2, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) as illustrated in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0386-Q1 is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC0386-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

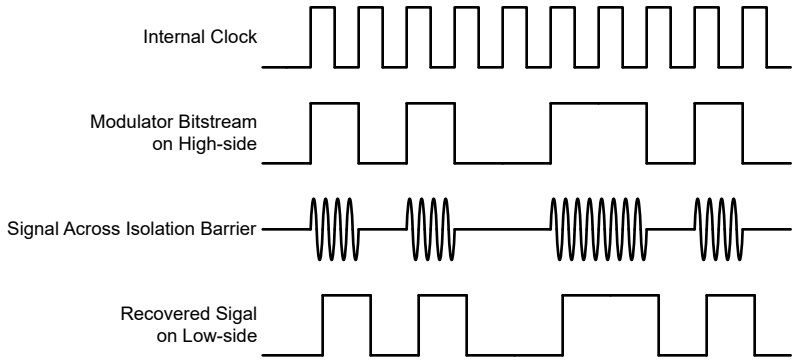


図 6-2. OOK-Based Modulation Scheme

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6.3.4 Digital Output

A differential input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 1V produces a stream of ones and zeros that are high 89.06% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58368. A differential input of -1V produces a stream of ones and zeros that are high 10.94% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 7168. These input voltages are also the specified linear range of the AMC0386-Q1. If the input voltage value exceeds this range, the output of the modulator shows increasing nonlinear behavior as the quantization noise increases. The modulator output clips with a constant stream of zeros at an input ≤-1.28V or with a constant stream of ones at an input ≥1.28V. In this case, however, the AMC0386-Q1 generates a single 1 or 0 every 128 clock cycles to indicate proper device function. A single 1 is generated if the input is at negative fullscale and a 0 is generated if the input is at positive fullscale. See the *Output Behavior in Case of a Fullscale Input* section for more details. 図 6-3 shows the input voltage versus the output modulator signal.

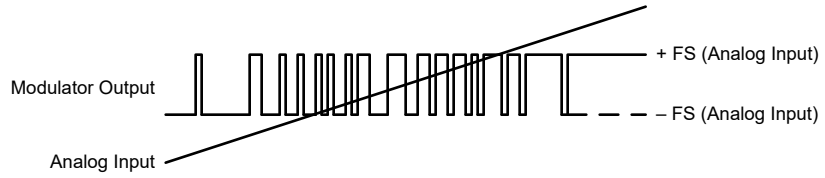

図 6-3. Modulator Output vs Analog Input

Calculate the density of ones in the output bitstream with 式 1 for any input voltage V_{IN} = (V_{SNSP} – V_{SNSN}) value. The only exception is a fullscale input signal. See the *Output Behavior in Case of a Fullscale Input* section.

$$\rho = (|V_{Clipping}| + V_{IN}) / (2 \times V_{Clipping}) \quad (1)$$

6.3.4.1 Output Behavior in Case of a Fullscale Input

If a fullscale input signal is applied to the AMC0386-Q1, the device generates a single one or zero every 128 bits at DOUT. 図 6-4 shows a timing diagram of this process. A single 1 or 0 is generated depending on the actual polarity of the signal being sensed. A fullscale signal is defined as $|V_{SNSP} - V_{SNSN}| \geq |V_{Clipping}|$. In this way, differentiating between a missing AVDD and a fullscale input signal is possible on the system level.

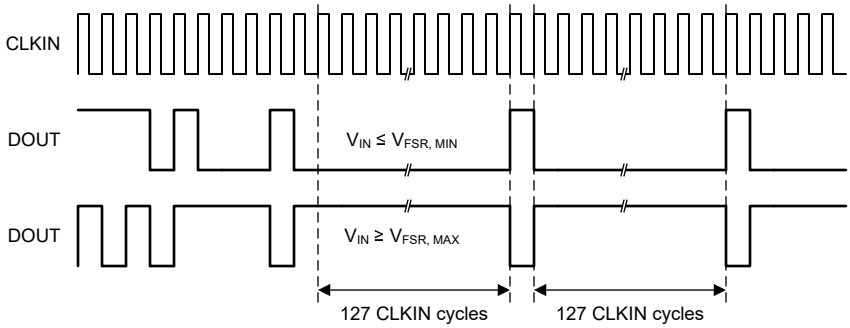

図 6-4. Fullscale Output of the AMC0386-Q1

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6.3.4.2 Output Behavior in Case of a Missing High-Side Supply

As shown in 図 6-5, the device provides a constant bitstream of logic 0's at the output if the high-side supply is missing. DOUT is permanently low when the high-side supply is missing. A one is not generated every 128 clock pulses, which differentiates this condition from a valid negative fullscale input. This feature helps identify high-side power-supply problems on the board.

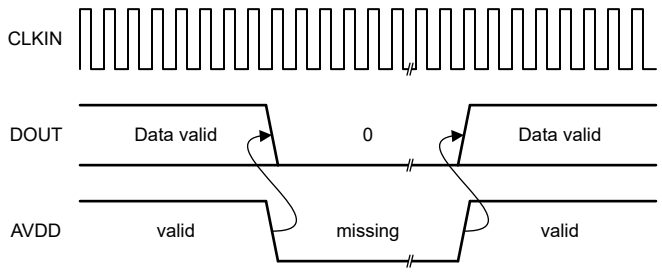

図 6-5. Output of the AMC0386-Q1 in Case of a Missing High-Side Supply

6.4 Device Functional Modes

The AMC0386-Q1 operates in one of the following states:

- OFF-state: The low-side of the device (AVDD) is below the $AVDD_{UV}$ threshold. The device is not responsive. OUT はハイ インピーダンス状態。内部的に、OUT および CLKIN は、ESD 保護ダイオードにより DVDD および DGND にクランプされます。
- Missing high-side supply: The low-side of the device (DVDD) is supplied and within *Recommended Operating Conditions* . The high-side supply (AVDD) is below the $AVDD_{UV}$ threshold. このデバイスは、セクションで説明されているように、ロジック 0 の一定のビットストリームを出力します。
- Analog input overrange (positive fullscale input): AVDD and DVDD are within recommended operating conditions but the analog input voltage $V_{IN} = (V_{SNSP} – V_{SNSN})$ is above the maximum clipping voltage ($V_{Clipping, MAX}$). Output Behavior in Case of a Fullscale Input セクションで説明しているように、このデバイスは 128 クロックサイクルごとにロジック 0 を出力します。
- Analog input underrange (negative fullscale input): AVDD and DVDD are within recommended operating conditions but the analog input voltage $V_{IN} = (V_{SNSP} – V_{SNSN})$ is below the minimum clipping voltage ($V_{Clipping, MIN}$). Output Behavior in Case of a Fullscale Input セクションで説明しているように、このデバイスは 128 クロックサイクルごとにロジック 1 を出力します。
- Normal operation: V_{AVDD}, V_{DVDD}, and V_{IN} are within the recommended operating conditions. The device outputs a digital bitstream, as explained in the *Digital Output* section.

表 6-1 lists the operational modes.

表 6-1. Device Operational Modes

OPERATINAL MODE	AVDD	DVDD	V_{IN}	DEVICE RESPONSE
OFF	Don't care	$V_{DVDD} < DVDD_{UV}$	Don't care	OUT はハイ インピーダンス状態。内部的に、OUT および CLKIN は、ESD 保護ダイオードにより DVDD および DGND にクランプされます。
Missing high-side supply	$V_{AVDD} < AVDD_{UV}$	Valid(1)	Don't care	このデバイスは、セクションで説明されているように、ロジック 0 の一定のビットストリームを出力します。
Input overrange	Valid(1)	Valid(1)	$V_{IN} > V_{Clipping, MAX}$	Output Behavior in Case of a Fullscale Input セクションで説明しているように、このデバイスは 128 クロックサイクルごとにロジック 0 を出力します。

表 6-1. Device Operational Modes (続き)

OPERATINAL MODE	AVDD	DVDD	V_{IN}	DEVICE RESPONSE
Input underrange	Valid(1)	Valid(1)	$V_{IN} < V_{Clipping, MIN}$	Output Behavior in Case of a Fullscale Input セクションで説明しているように、このデバイスは 128 クロックサイクルごとにロジック 1 を出力します。
Normal operation	Valid(1)	Valid(1)	Valid(1)	Normal operation

(1) "Valid" denotes within the recommended operating conditions.

ADVANCE INFORMATION

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Best Design Practices

Avoid any kind of leakage current betweet the HVIN and SNSP pin. Leakage current potentially introduces significant measurement error. See the *Layout Example* for layout recommendations.

7.2 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0386-Q1 is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501-Q1 and a transformer that supports the desired isolation voltage ratings.

The AMC0386-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. 図 7-1 shows a decoupling diagram for the AMC0386-Q1.

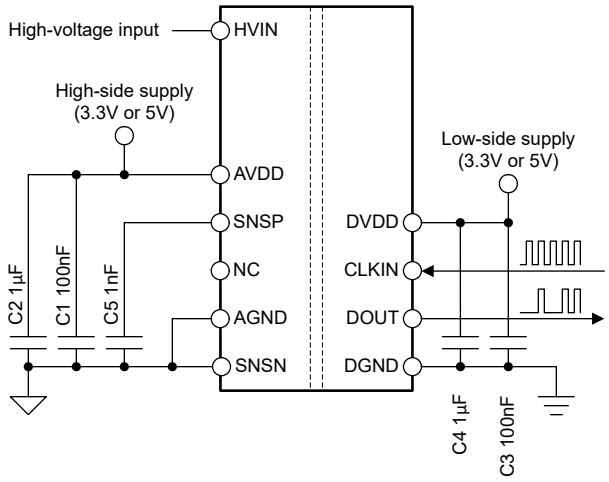

図 7-1. Decoupling of the AMC0386-Q1

Capacitors provide adequate effective capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

ADVANCE INFORMATION

7.3 Layout

7.3.1 Layout Guidelines

図 7-2 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0386-Q1 supply pins). This section also depicts the placement of other components required by the device.

TI recommends placing a guard ring around the SNSP pin and to connect the guard ring to AGND. The guard ring prevents leakage currents from forming a parallel current path between HVIN and SNSP. The guard ring is partially routed underneath the device, reducing the clearance distance between the high-voltage and low-voltage side. Place a keep-out zone around pins 7 and 8 (both pins have no internal connection) to recover the full clearance distance of >8mm.

To maximize the creepage distance between the high-voltage and low-voltage side, TI recommends placing another keep-out zone around pin 15 as shown in 図 7-2.

7.3.2 Layout Example

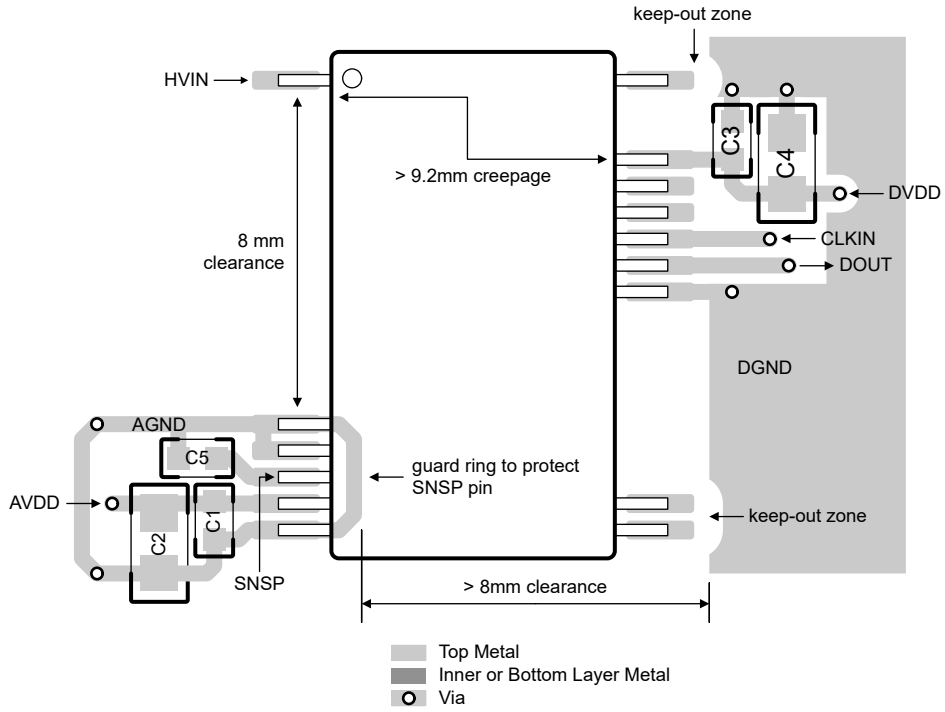

図 7-2. Recommended Layout of the AMC0386-Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity*
- Texas Instruments, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application report
- Texas Instruments, *Delta Sigma Modulator Filter Calculator* design tool

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

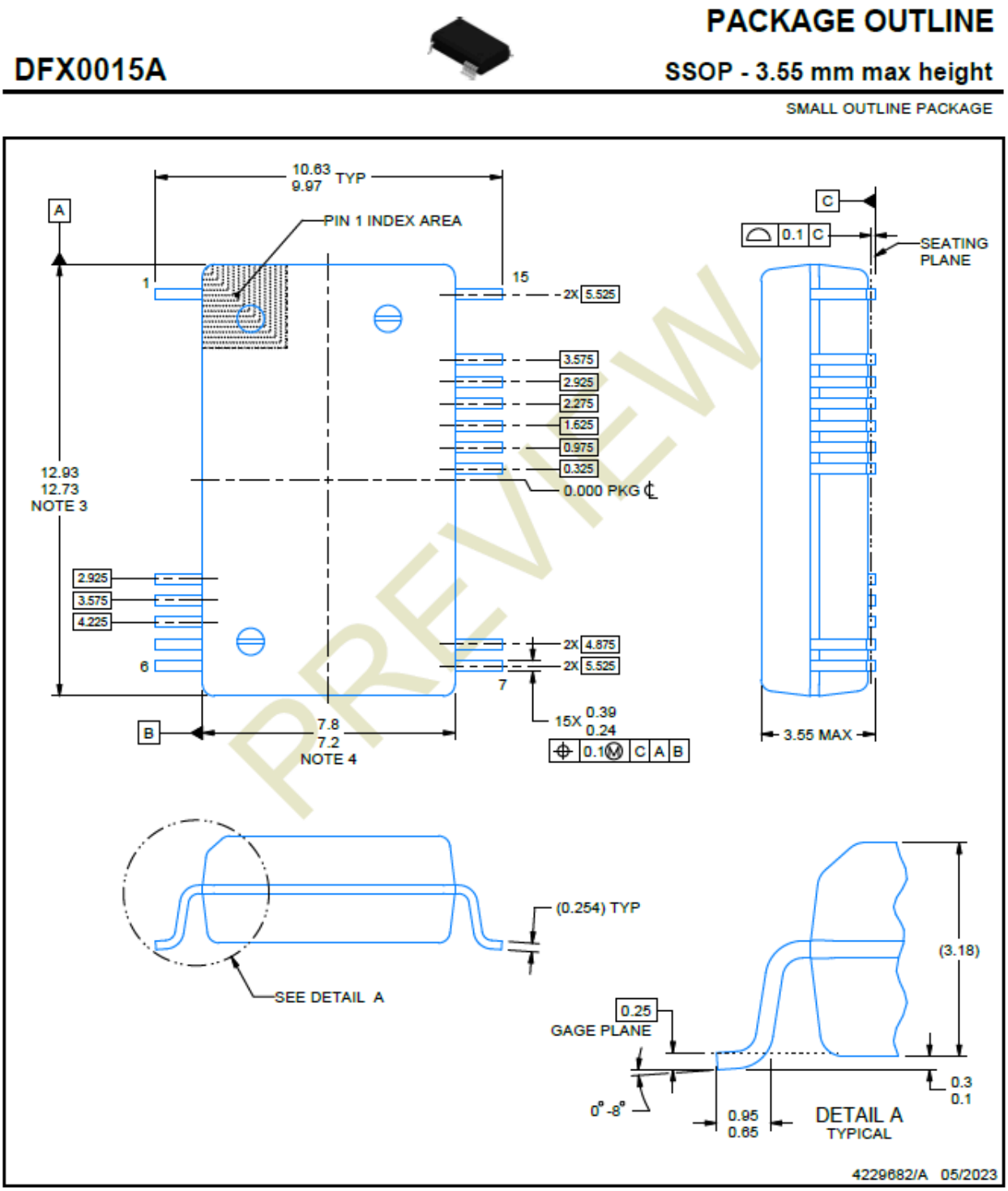
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

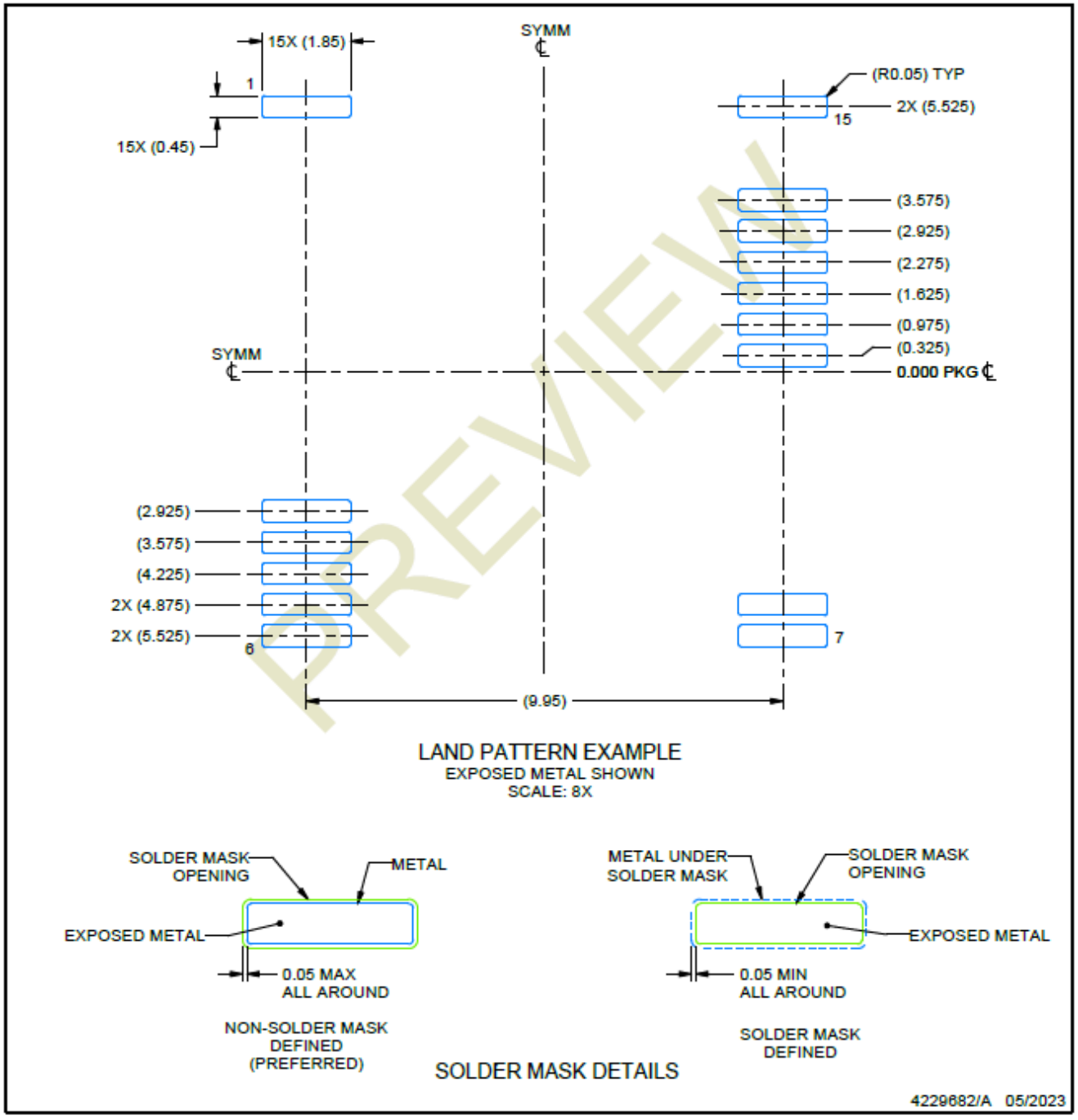
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DFX0015A

SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

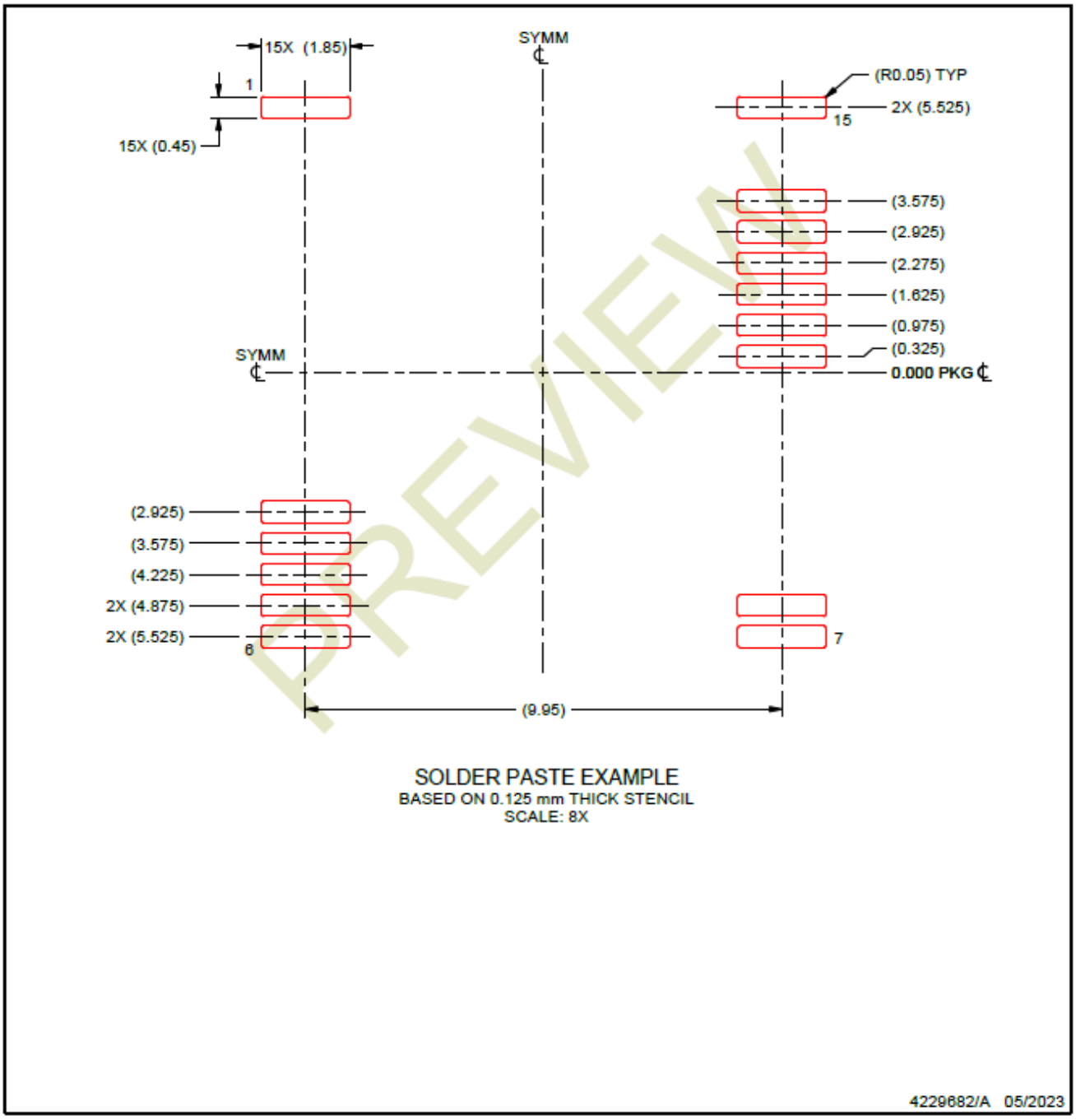
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFX0015A

SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PAMC0386M10QDFXRQ1	ACTIVE	SSOP	DFX	15	750	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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