AMC0x30S-Q1 車載対応、固定ゲイン シングルエンド出力付き、高精度、±1V 入力、基本および強化絶縁型アンプ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- リニア入力電圧範囲:±1V
- 高い入力インピーダンス:1GΩ (標準値)
- 電源電圧範囲:
  - ハイサイド (VDD1):3.0V～5.5V
  - ローサイド (VDD2):3.0V～5.5V
- 固定ゲイン:1V/V
- シングルエンド出力
- 小さい DC 誤差:
  - オフセット誤差:±1.5mV (最大値)
  - オフセットドリフト:±20µV/°C (最大値)
  - ゲイン誤差:±0.25% (最大値)
  - ゲインドリフト:±40ppm/°C (最大値)
  - 非線形性:0.05% (最大値)
- 「高 CMTI:50V/ns (最小値)
- 低 EMI:CISPR-11 および CISPR-25 規格に準拠
- 絶縁定格:
  - AMC0230S-Q1:基本絶縁型
  - AMC0330S-Q1:強化絶縁型
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL1577

2 アプリケーション

- トラクション インバータ
- オンボード チャージャ
- DC/DC コンバータ

3 概要

AMC0x30S-Q1 は±1V、高インピーダンス入力、固定ゲイン、シングルエンド出力備えた高精度、電気的絶縁型アンプです。高インピーダンス入力は、高インピーダンスの抵抗分圧器や出力抵抗の高い他の電圧信号源と接続するよう最適化されています。

この絶縁バリアは、異なる同相電圧レベルで動作するシステム領域を分離します。絶縁バリアは磁気干渉に対して非常に耐性があります。この絶縁バリアは、最大 $5kV_{RMS}$ (DWV パッケージ) の強化絶縁と、最大 $3kV_{RMS}$ (D パッケージ) (60s) の基本絶縁を実現することが認定されています。

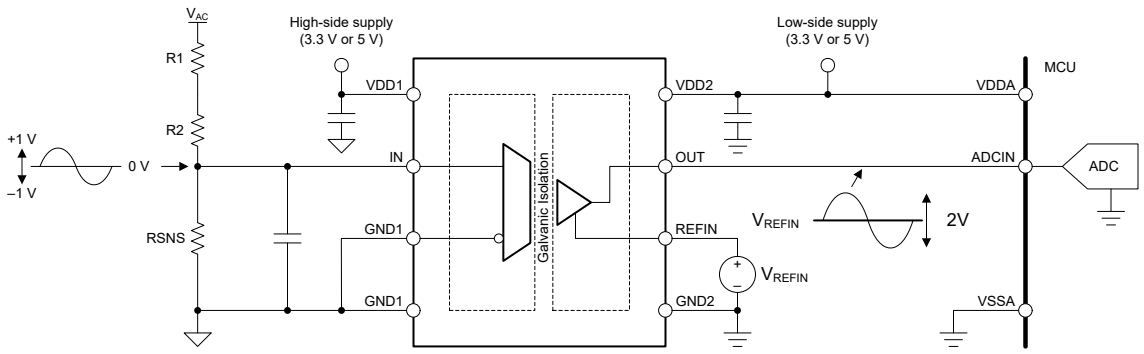
AMC0x30S-Q1 は、1V/V の固定ゲインで入力電圧に比例するシングルエンド信号を出力します。出力は、ADC の入力に直接接続できるように設計されています。REFIN ピンに印加される電圧によって、0V 入力の出力電圧が設定されます。

AMC0x30S-Q1 デバイスは、8 ピンのワイド ボディおよびナロー ボディ SOIC パッケージで供給され、–40°C から 125°C までの温度範囲で完全に動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
AMC0230S-Q1 (3)	D (SOIC 8)	4.9mm × 6.0mm
AMC0330S-Q1	DWV (SOIC 8)	5.85mm × 11.5mm

(1) 詳細については、付録「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 製品プレビュー



代表的なアプリケーション

ADVANCE INFORMATION

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4 Device Comparison Table

PARAMETER	AMC0230S-Q1 (1)	AMC0330S-Q1
Isolation rating per VDE 0884-17	Basic	Reinforced
Package	Narrow-body SOIC (D)	Wide-body SOIC (DWV)

(1) PRODUCT PREVIEW

ADVANCE INFORMATION

5 Pin Configuration and Functions

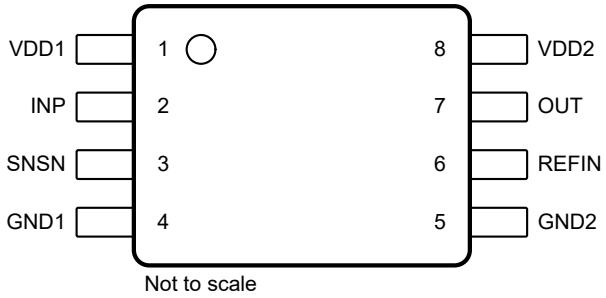


図 5-1. DWV および D パッケージ, 8 ピン SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply(1)
2	INP	Analog input	Analog input
3	SNSN	Analog input	GND1 sense pin and inverting analog input to the modulator. Connect to GND1.
4	GND1	High-side ground	High-side analog ground
5	GND2	Low-side ground	Low-side analog ground
6	REFIN	Analog input	このピンに印加される電圧は、本デバイスの出力電圧に対するオフセットとして追加されます。内部では、90kΩ 抵抗が REFIN と GND2 の間に接続されています。
7	OUT	Analog output	Analog output
8	VDD2	Low-side power	Low-side power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	INP, SNSN to GND1	GND1 – 3	VDD1 + 0.5	V
Reference input voltage	REFIN to GND2	GND2 – 0.5	VDD2 + 0.5	V
Analog output voltage	OUT to GND2	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD1	High-side power supply	VDD1 to GND1	3	5.0	5.5	V
VDD2	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Nominal input voltage before clipping output	INP to SNSN	–1.28		1.28	V
V_{FSR}	Specified linear input voltage	INP to SNSN	–1		1	V
V_{REFIN}	Reference input voltage	REFIN to GND2	2.7		VDD2 – $V_{Clipping}$ – 0.25	V
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	OUT to GND2			500	pF
R_{LOAD}	Resistive load	OUT to GND2		10	1	kΩ
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

ADVANCE INFORMATION

6.4 Thermal Information (D Package)

THERMAL METRIC(1)		D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

ADVANCE INFORMATION

6.5 Thermal Information (DWV Package)

THERMAL METRIC[1]		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.6 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5V	TBD	mW
P_{D1}	Maximum power dissipation (high-side)	AVDD = 3.6V	TBD	mW
		AVDD = 5.5V	TBD	
P_{D2}	Maximum power dissipation (low-side)	DVDD = 3.6V	TBD	mW
		DVDD = 5.5V	TBD	

ADVANCE INFORMATION

6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 4	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 4	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1130	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	800	V_{RMS}
		At DC voltage	1130	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	4250	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7), $V_{pd(ini)} = V_{IOTM} = V_{pd(m)}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 V_{PP} at 1MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 6000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1410	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1000	V_{RMS}
		At DC voltage	1410	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 V_{PP} at 1MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

ADVANCE INFORMATION

6.9 Safety-Related Certifications (Basic Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ; 6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Basic insulation	Single protection
Certificate number: Pending	File number: Pending

ADVANCE INFORMATION

6.10 Safety-Related Certifications (Reinforced Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending

ADVANCE INFORMATION

6.11 Safety Limiting Values (D Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = TBD°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			TBD	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = TBD°C/W, VDDx = 3.6V, T_J = 150°C, T_A = 25°C			TBD	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = TBD°C/W, T_J = 150°C, T_A = 25°C			TBD	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

ADVANCE INFORMATION

6.12 Safety Limiting Values (DWV Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = TBD°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			TBD	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = TBD°C/W, VDDx = 3.6V, T_J = 150°C, T_A = 25°C			TBD	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = TBD°C/W, T_J = 150°C, T_A = 25°C			TBD	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

ADVANCE INFORMATION

6.13 Electrical Characteristics

typical specifications are at T_A = 25°C, VDD1 = 5V, and VDD2 = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
C_{IN}	Input capacitance			TBD		pF
R_{INP}	Input impedance	INP pin, T_A = 25°C		1		GΩ
I_{IB}	Input bias current	INP = GND1, T_A = 25°C	–15	3.5	15	nA
CMTI	Common-mode transient immunity		50			V/ns
ANALOG OUTPUT						
	Nominal gain			1		V/V
R_{OUT}	Output resistance	OUTP or OUTN		<0.2		Ω
	Output short-circuit current	sourcing or sinking, INP = GND1, output shorted to either GND or VDD2		11		mA
DC ACCURACY						
V_{OS}	Input offset voltage(1) (2)	INP = GND1, VDD2 = 3.3V, V_{REFIN} = 1.65V, T_A = 25°C	–1.5	±0.2	1.5	mV
TCV_{OS}	Input offset thermal drift(1) (2) (4)		–20	±3	20	µV/°C
E_G	Gain error(1)	T_A = 25°C	–0.25%	±0.05%	0.25%	
TCE_G	Gain error drift(1) (5)		–40	±5	40	ppm/°C
	Nonlineartity(1)		–0.05%	±0.01%	0.05%	
	Output noise	INP = GND1, BW = 50kHz		TBD		µVrms
PSRR	Power-supply rejection ratio(2)	VDD1 DC PSRR, INP = GND1, VDD1 from 3V to 5.5V		–80		dB
		VDD1 AC PSRR, INP = GND1, VDD1 with 10kHz / 100mV ripple		–65		
		VDD2 DC PSRR, INP = GND1, VDD2 from 3V to 5.5V		–85		
		VDD2 AC PSRR, INP = GND1, VDD2 with 10kHz / 100mV ripple		–70		
AC ACCURACY						
BW	Output bandwidth		90	110		kHz
THD	Total harmonic distortion(3)	V_{INP} = 2V_{PP}, V_{INP} > 0V, f_{IN} = 10kHz		–92	–80	dB
SNR	Signal-to-noise ratio	V_{INP} = 2.25V_{PP}, f_{INP} = 1kHz, BW = 10kHz	72	79		dB
		V_{INP} = 2.25V_{PP}, f_{INP} = 10kHz, BW = 50kHz		72		
POWER SUPPLY						
I_{DD1}	High-side supply current			4.2	6.0	mA
I_{DD2}	Low-side supply current			6.0	9.9	mA
$VDD1_{UV}$	High-side undervoltage detection threshold	VDD1 rising	2.5	2.6	2.7	V
		VDD1 falling	1.9	2.0	2.1	
$VDD2_{UV}$	Low-side undervoltage detection threshold	VDD2 rising	2.5	2.6	2.7	V
		VDD2 falling	1.9	2.0	2.1	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G\ (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25°C)} \times TempRange) \times 10^6$

6.14 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.8		µs
t_f	Output signal fall time			1.8		µs
	V_{INP} to V_{OUT} signal delay (50% - 10%)	Unfiltered output		2.4		µs
	V_{INP} to V_{OUT} signal delay (50% - 50%)	Unfiltered output		3.0	3.2	µs
	V_{INP} to V_{OUT} signal delay (50% - 90%)	Unfiltered output		4.2		µs
t_{AS}	Analog settling time	AVDD step to 3.0V with DVDD ≥ 3.0V, to V_{OUT} valid, 0.1% settling		50	100	µs

6.15 Timing Diagram

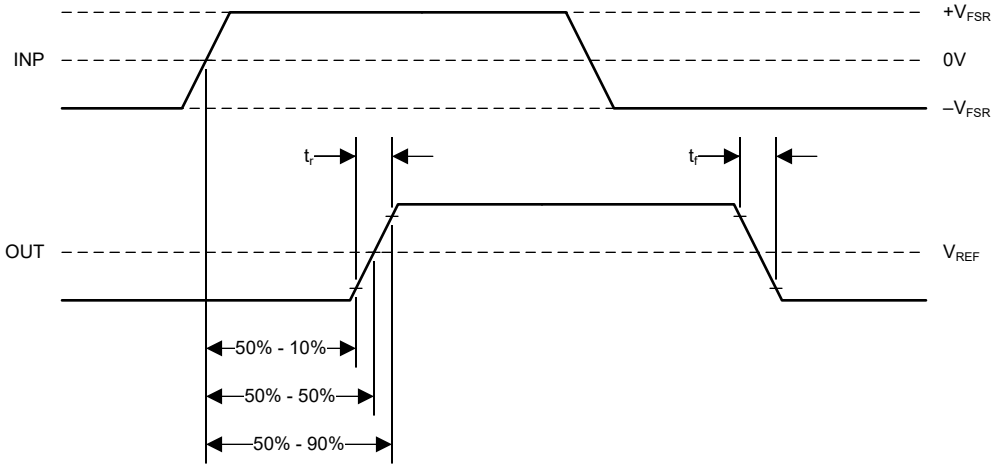


図 6-1. Rise, Fall, and Delay Time Definition

ADVANCE INFORMATION

ADVANCE INFORMATION

7 Detailed Description

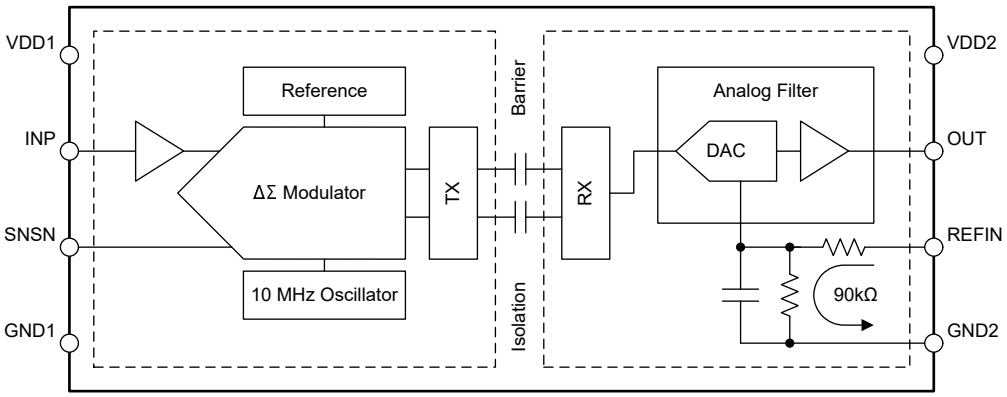
7.1 Overview

The AMC0x30S-Q1 is a precision, galvanically isolated amplifier with a ±1V、高インピーダンス入力、固定ゲイン、シングルエンド出力. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high side from the low side.

On the low-side, the received bitstream is processed by an analog filter that outputs a GND2-referenced, single-ended signal at the OUT pin. This single-ended output signal is proportional to the input signal. The output voltage at 0V input is set by the voltage applied to the REFIN pin.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The digital modulation used in the AMC0x30S-Q1 transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The input stage of the AMC0x30S-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal. First, if the input voltage exceeds the value specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10mA. This limitation is caused by the device input electrostatic discharge (ESD) diodes turning on. Second, linearity and noise performance are specified only when the input voltage is within the linear fullscale range (V_{FSR}). V_{FSR} is specified in the *Recommended Operating Conditions* table.

7.3.2 Isolation Channel Signal Transmission

The AMC0x30S-Q1 uses an on-off keying (OOK) modulation scheme, as shown in 図 7-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) as illustrated in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0x30S-Q1 is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC0x30S-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

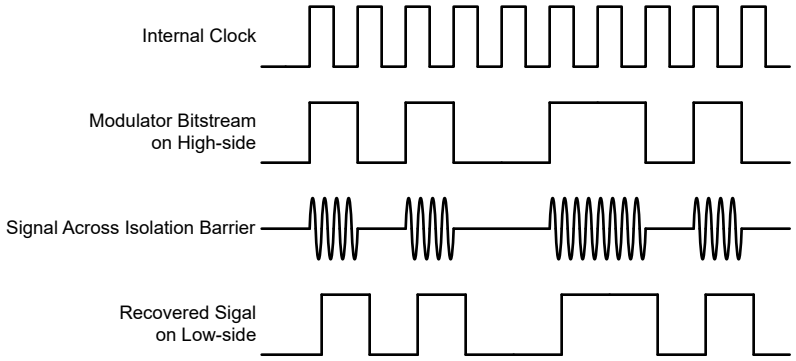


図 7-1. OOK-Based Modulation Scheme

ADVANCE INFORMATION

7.3.3 Analog Output

The AMC0x30S-Q1 provides a single-ended analog output voltage that is proportional to the input voltage. The output is referred to GND2 and is galvanically isolated from the input of the device. The output is designed to connect directly to the input of an ADC.

The mid-range output voltage is set by the REFIN pin. For any input voltage within the specified linear input range, the device outputs a voltage equal to:

$$V_{OUT} = V_{IN} + V_{REFIN} = (V_{INP} – V_{SNSN}) + V_{REFIN} \quad (1)$$

The device is linear within the specified linear fullscale range. Beyond the linear fullscale range, the output continues to follow the input, but with reduced linearity performance. The output clips when the input voltage reaches the clipping voltage. 図 7-2 shows the input-to-output transfer characteristic.

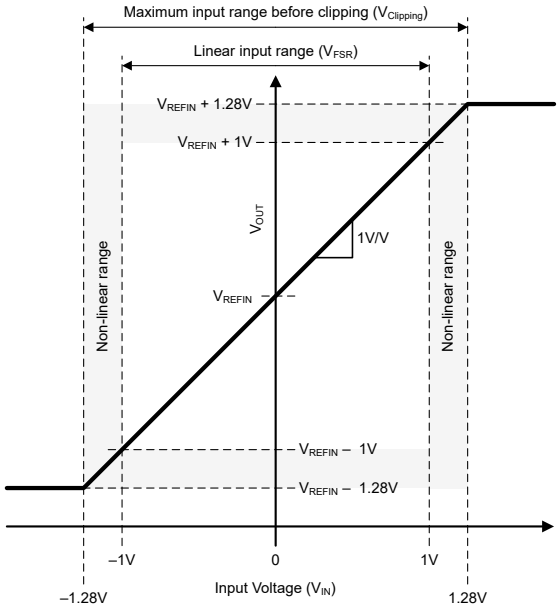


図 7-2. Input to Output Transfer Curve of the AMC0x30S-Q1

ADVANCE INFORMATION

7.4 Device Functional Modes

The AMC0x30S-Q1 operates in one of the following states:

- OFF-state: The low-side supply (VDD2) is below the $VDD2_{UV}$ threshold. The device is not responsive. OUT はハイ インピーダンス状態。内部では、OUT は ESD 保護ダイオードによって VDD2 および GND2 にクランプされます。
- Missing high-side supply: The low-side of the device (VDD2) is supplied and within the *Recommended Operating Conditions* section. The high-side supply (VDD1) is below the $VDD1_{UV}$ threshold. OUT ピンは V_{REFIN} に駆動されます。
- Analog input overrange (positive fullscale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is above the maximum clipping voltage $V_{Clipping, MAX}$. 本デバイスは OUT ピンに V_{REFIN} を出力します。
- Analog input underrange (negative fullscale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is below the minimum clipping voltage $V_{Clipping, MIN}$. OUT ピンは GND2 に駆動されます。
- Normal operation: VDD1, VDD2, and V_{IN} are within the recommended operating conditions. 本デバイスは、入力電圧に比例する電圧を出力します。

表 7-1 lists the operating modes.

表 7-1. Device Operational Modes

OPERATING CONDITION	VDD1	VDD2	V_{IN}	DEVICE RESPONSE
OFF	Don't care	VDD2 < $VDD2_{UV}$	Don't care	OUT はハイ インピーダンス状態。内部では、OUT は ESD 保護ダイオードによって VDD2 および GND2 にクランプされます。
Missing high-side supply	VDD1 < $VDD1_{UV}$	Valid(1)	Don't care	OUT ピンは V_{REFIN} に駆動されます。
Input overrange	Valid(1)	Valid(1)	V_{IN} > $V_{Clipping, MAX}$	本デバイスは OUT ピンに V_{REFIN} を出力します。
Input underrange	Valid(1)	Valid(1)	V_{IN} < $V_{Clipping, MIN}$	OUT ピンは GND2 に駆動されます。
Normal operation	Valid(1)	Valid(1)	Valid(1)	本デバイスは、入力電圧に比例する電圧を出力します。

(1) "Valid" denotes within the recommended operating conditions.

ADVANCE INFORMATION

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Best Design Practices

Do not leave the analog input (INP pin) of the AMC0x30S-Q1 unconnected (floating) when the device is powered up. If the device input is left floating, the output of the device is not valid.

Do not connect protection diodes to the input (INP pin) of the AMC0x30S-Q1. Diode leakage current potentially introduces significant measurement error especially at high temperatures. The input pin is protected against high voltages by the ESD protection circuit and the high impedance of the external restive divider.

9 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0x30S-Q1 is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501-Q1 and a transformer that supports the desired isolation voltage ratings.

The AMC0x30S-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. 図 9-1 shows a decoupling diagram for the AMC0x30S-Q1.

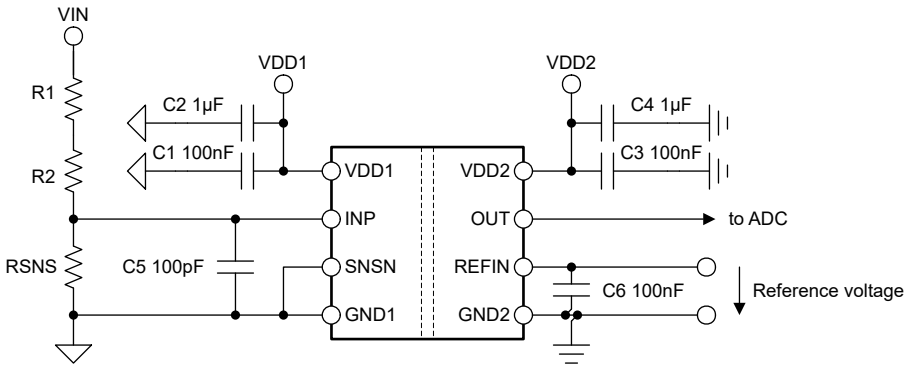


図 9-1. Decoupling of the AMC0x30S-Q1

Capacitors provide adequate effective capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

ADVANCE INFORMATION

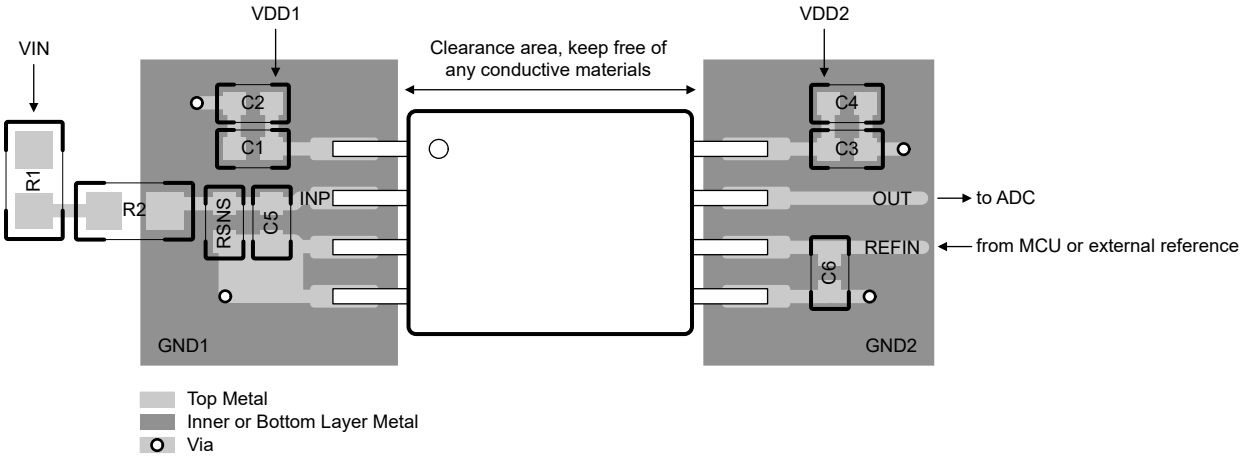
10 Layout

10.1 Layout Guidelines

The *Layout* section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0x30S-Q1 supply pins). This example also depicts the placement of other components required by the device. For best performance, place the sense resistor close to the device input pin (INP).

10.2 Layout Example

図 10-1. Recommended Layout of the AMC0x30S-Q1



11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instrument, *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2024	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

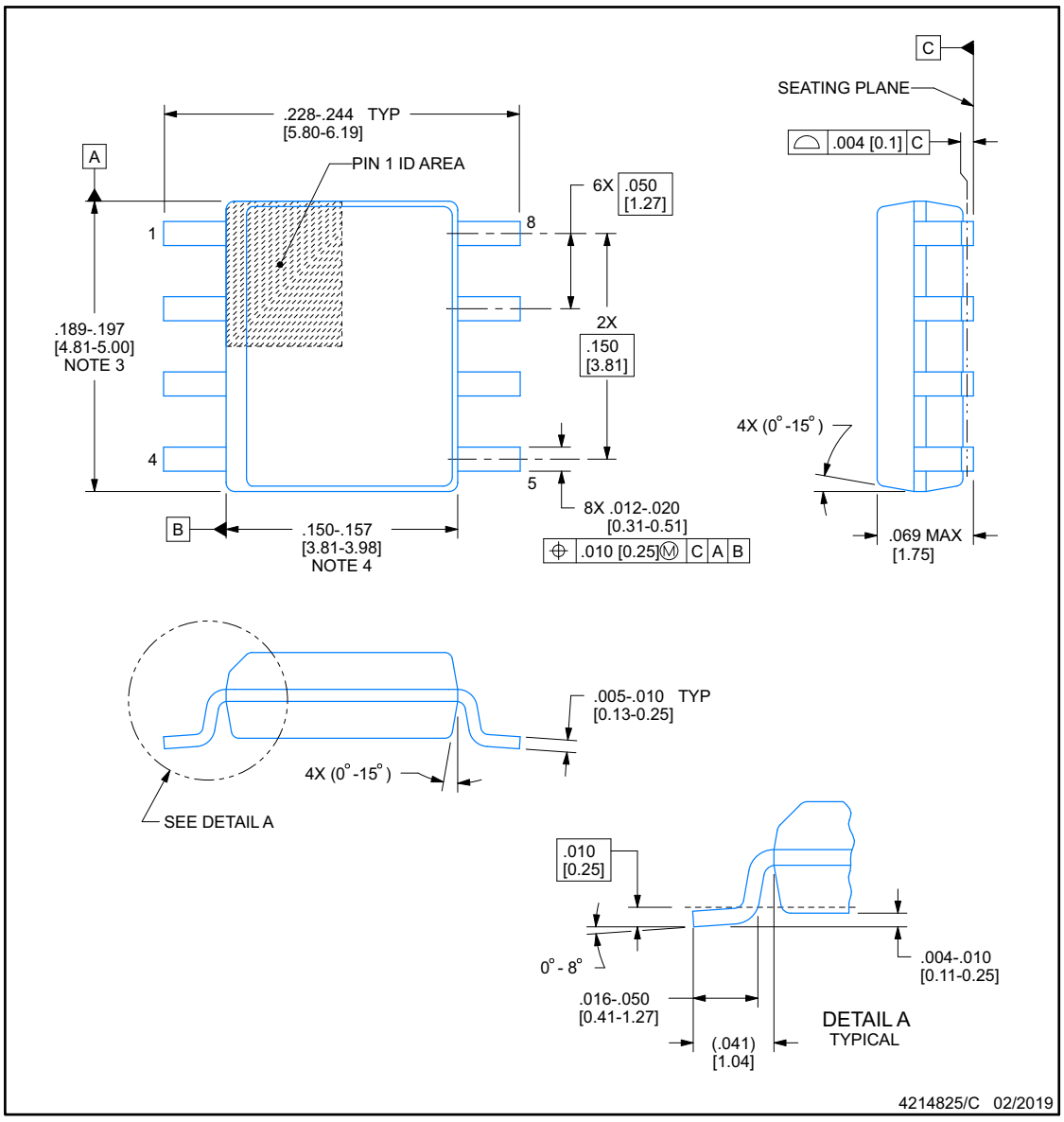
ADVANCE INFORMATION

13.1 Mechanical Data

PACKAGE OUTLINE

D0008A — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

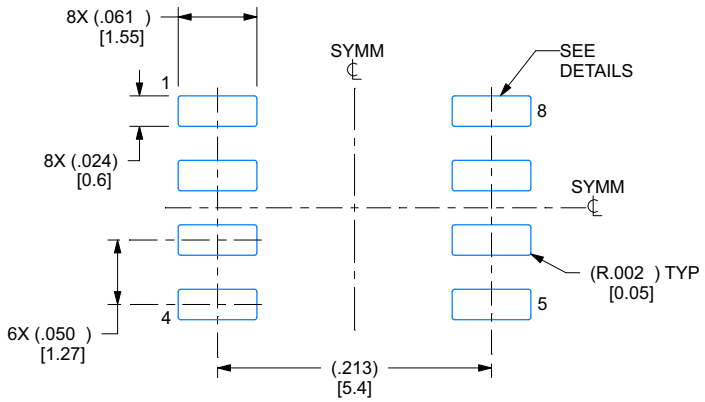
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

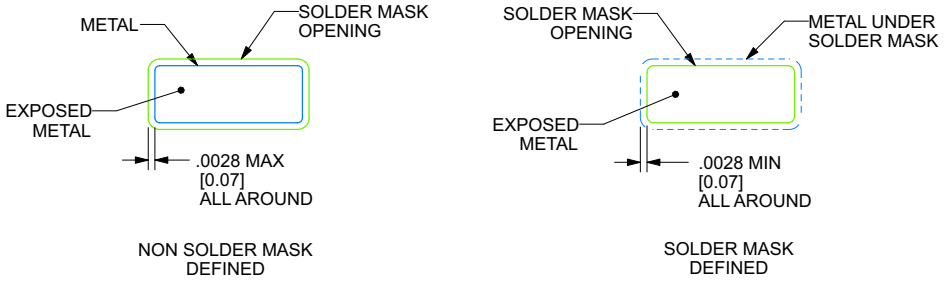
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

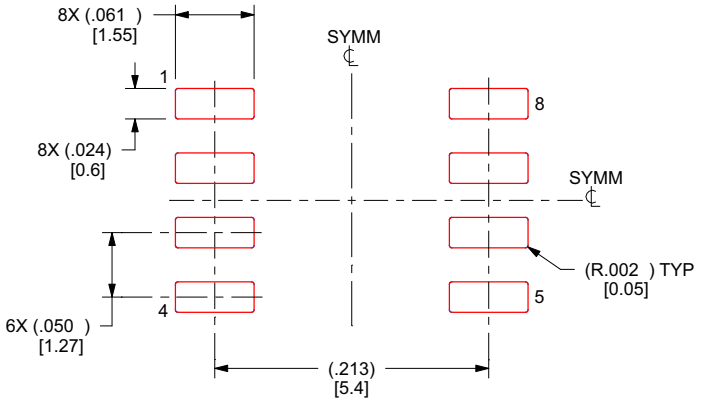
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

D0008A — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

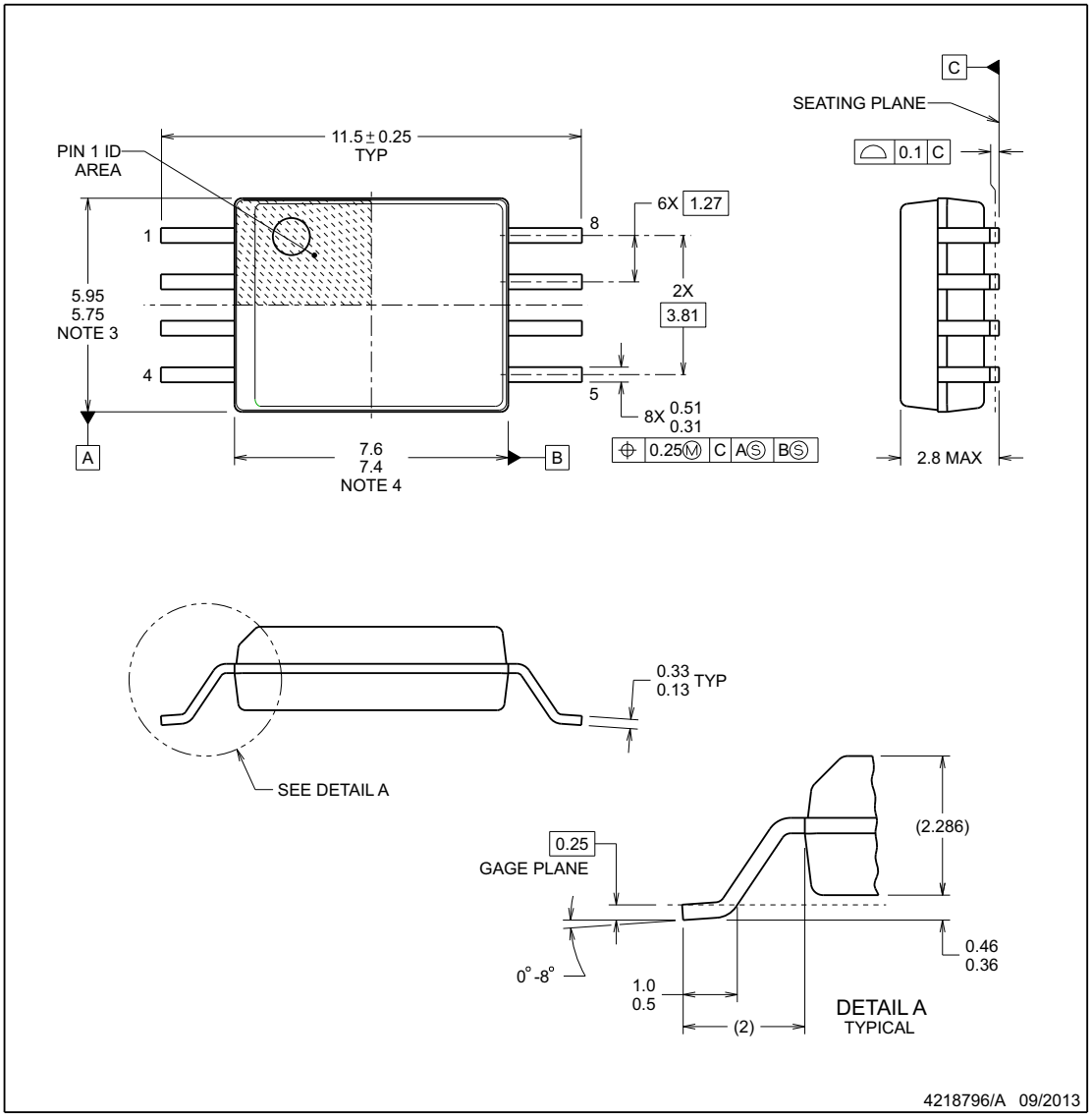
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DWV0008A

SOIC - 2.8 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

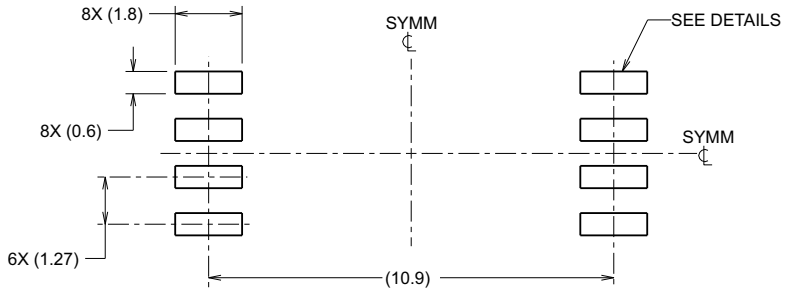
ADVANCE INFORMATION

ADVANCE INFORMATION

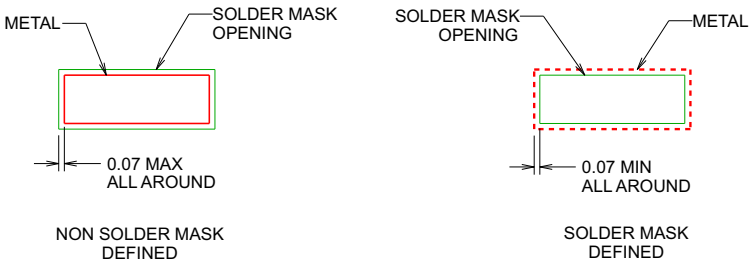
EXAMPLE BOARD LAYOUT

DWV0008A — SOIC - 2.8 mm max height

SOIC



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

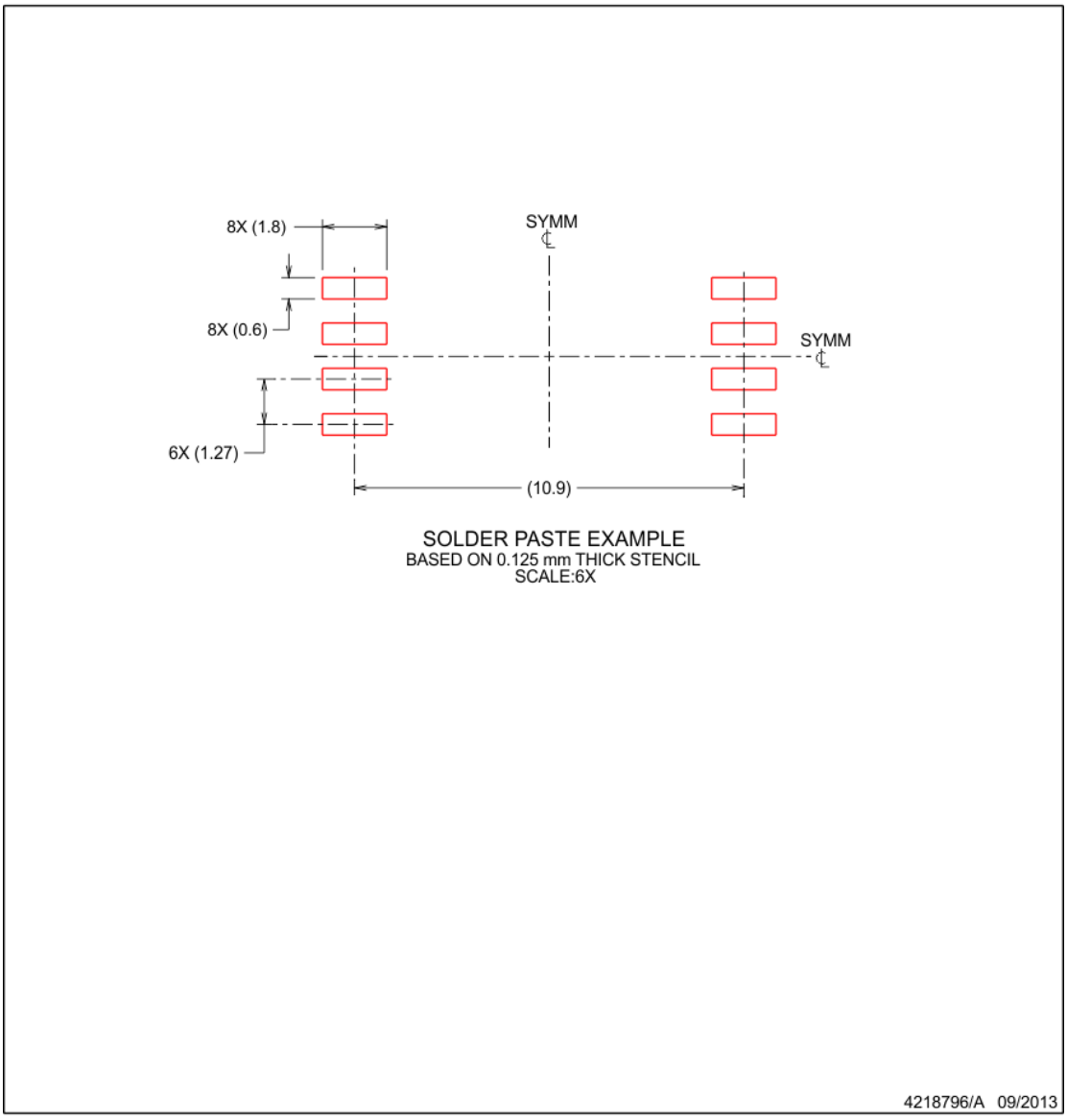
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWV0008A — SOIC - 2.8 mm max height

SOIC



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PAMC0330SQDWVRQ1	ACTIVE	SOIC	DWV	8	1000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

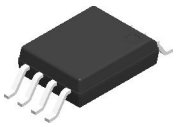
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

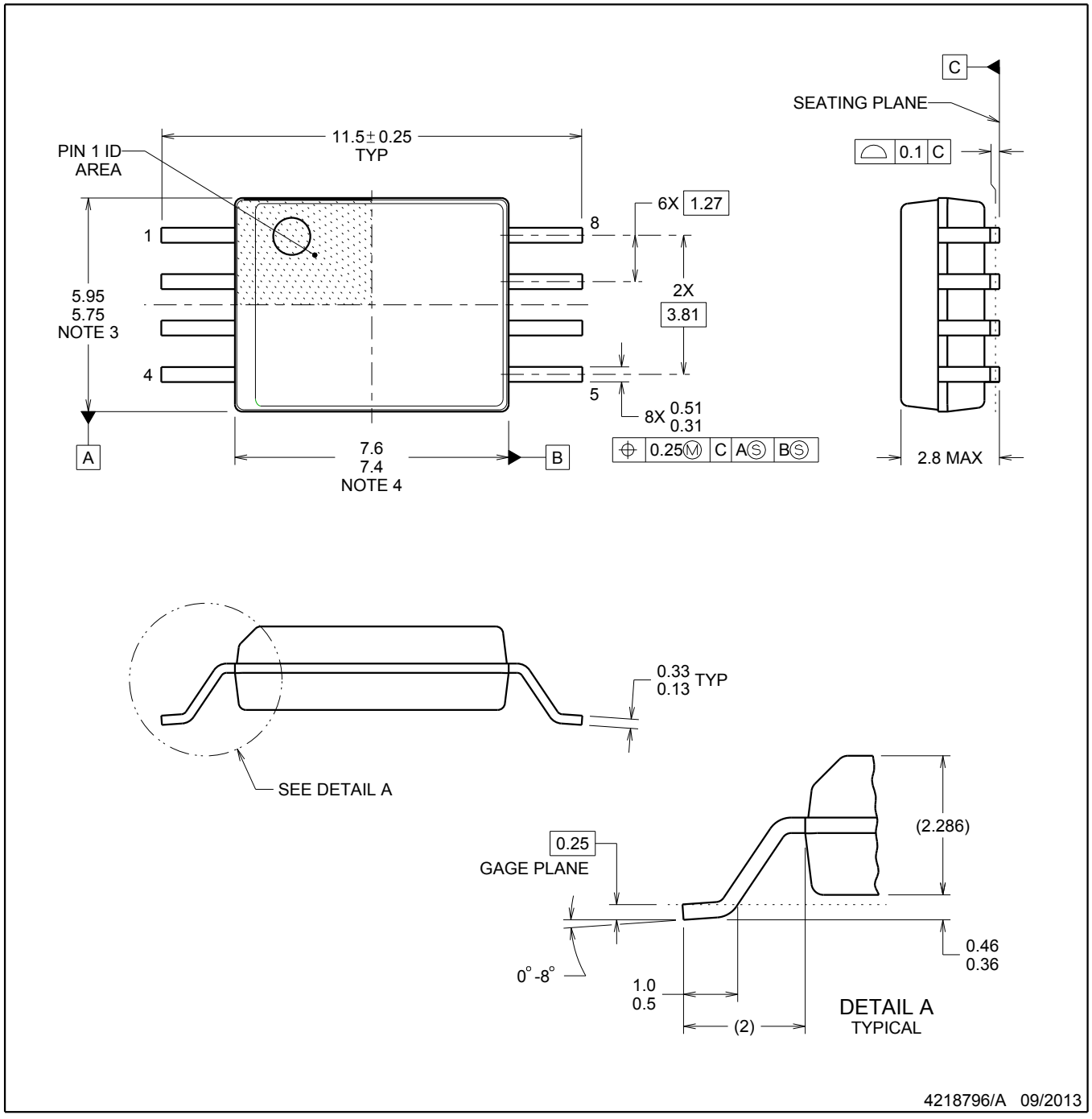
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



DWV0008A

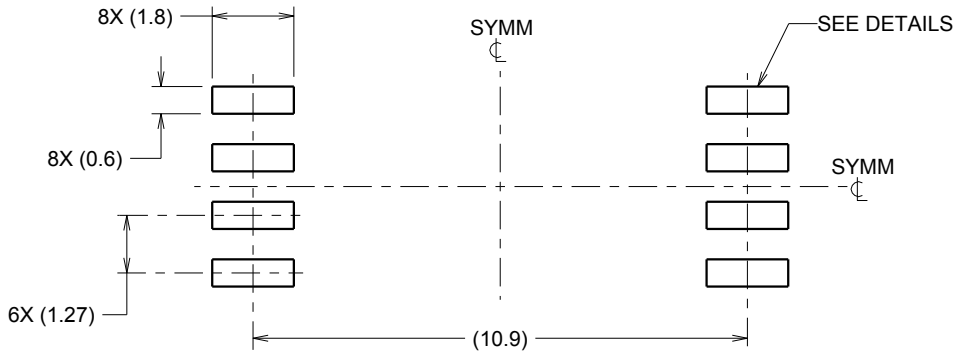
SOIC - 2.8 mm max height

SOIC

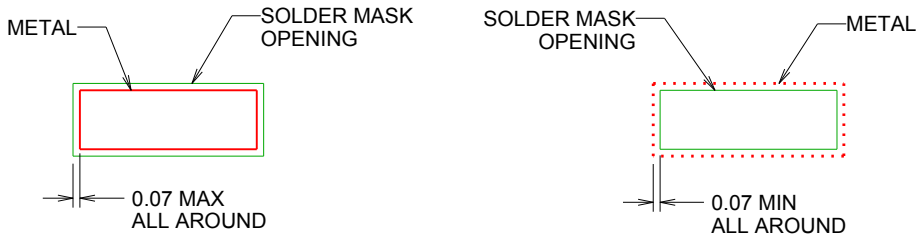


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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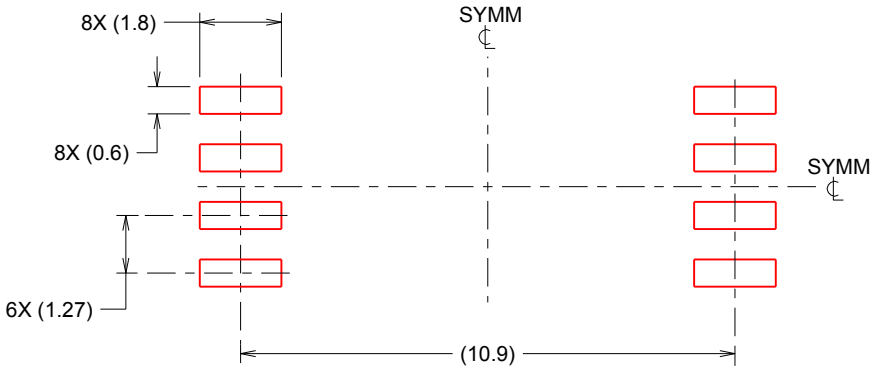
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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