AMC0x36 高精度、±1V 入力、基本および強化絶縁型の外部クロックによるデルタ シグマ変調器

1 特長

- リニア入力電圧範囲:±1V
- 高い入力インピーダンス:1GΩ (標準値)
- 電源電圧範囲:
  - ハイサイド (AVDD):3.0V～5.5V
  - ローサイド (DVDD):2.7V～5.5V
- 小さい DC 誤差:
  - オフセット誤差:±0.9mV (最大値)
  - オフセット ドリフト:±8.5µV/℃ (最大値)
  - ゲイン誤差:±0.25% (最大値)
  - ゲイン ドリフト:±35ppm/°C (最大値)
- 「高 CMTI:150V/ns (最小値)
- ハイサイド電源喪失の検出
- 低 EMI:CISPR-11 および CISPR-25 規格に準拠
- 絶縁定格:
  - AMC0236:基本絶縁型
  - AMC0336:強化絶縁型
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL1577
- 拡張産業温度範囲の全体にわたって完全に仕様を規定:-40℃～+125℃

2 アプリケーション

- モータードライブ
- 太陽光発電インバータ
- サーバー電源ユニット (PSU)
- エネルギー ストレージ システム

3 概要

AMC0x36 は、±1V、高インピーダンス入力、外部クロックのガルバニック絶縁された高精度のデルタ シグマ (ΔΣ) 変調器です。高インピーダンス入力は、高インピーダンスの抵抗分圧器や出力抵抗の高い他の電圧信号源と接続するよう最適化されています。

この絶縁バリアは、異なる同相電圧レベルで動作するシステム領域を分離します。絶縁バリアは磁気干渉に対して非常に耐性があります。この絶縁バリアは、最大 $5kV_{RMS}$ (DWV パッケージ) の強化絶縁と、最大 $3kV_{RMS}$ (D パッケージ) (60s) の基本絶縁を実現することが認定されています。

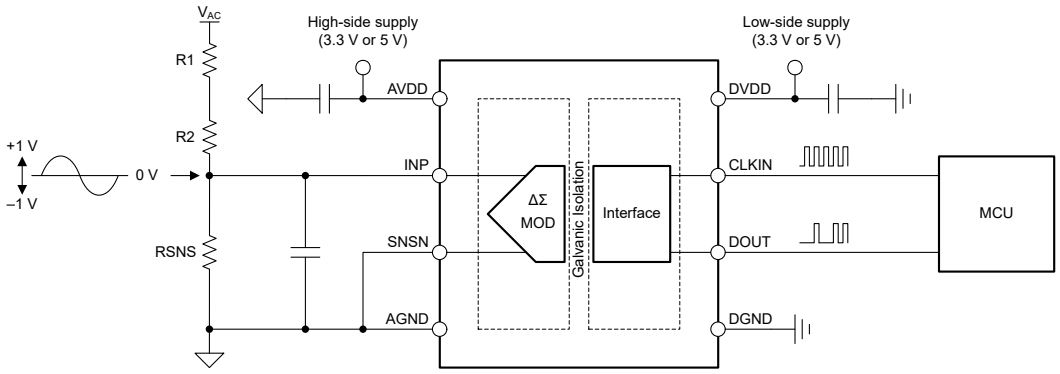
AMC0x36 の出力ビットストリームは、外部クロックと同期します。sinc3、OSR 256 フィルタと組み合わせることにより、このデバイスは 14.8 (分解能の実効ビット数)、または 89dB のダイナミック レンジ (サンプリング レート 39kSPS) を実現します。

AMC0x36 デバイスは、8 ピンのワイド ボディおよびナロー ボディ SOIC パッケージで供給され、–40°C から 125°C までの温度範囲で完全に動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
AMC0236	D (SOIC 8)	4.9mm × 6.0mm
AMC0336 (3)	DWV (SOIC 8)	5.85mm × 11.5mm

(1) 詳細については、「Mechanical, Packaging, and Orderable Information」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。
(3) 製品プレビュー



代表的なアプリケーション

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4 Device Comparison Table

PARAMETER	AMC0236	AMC0336 (1)
Isolation rating per VDE 0884-17	Basic	Reinforced
Package	Narrow-body SOIC (D)	Wide-body SOIC (DWV)

(1) PRODUCT PREVIEW

5 Pin Configuration and Functions

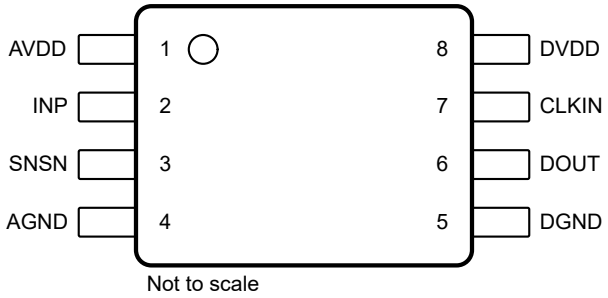


図 5-1. DWV および D パッケージ, 8 ピン SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	High-side power	Analog (high-side) power supply(1)
2	INP	Analog input	Noninverting analog input. Connect a 10nF filter capacitor from INP to SNSN.
3	SNSN	Analog input	AGND sense pin and inverting input to the modulator. Connect to AGND.
4	AGND	High-side ground	Analog (high-side) ground
5	DGND	Low-side ground	Digital (low-side) ground
6	DOUT	Digital output	Modulator data output
7	CLKIN	Digital input	Modulator clock input with internal pulldown resistor (typical value: 1.5MΩ)
8	DVDD	Low-side power	Digital (low-side) power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side AVDD to AGND	–0.3	6.5	V
	Low-side DVDD to DGND	–0.3	6.5	
Analog input voltage	INP to AGND	AGND – 3	AVDD + 0.5	V
Digital input voltage	CLKIN to DGND	DGND – 0.5	DVDD+ 0.5	V
Digital output voltage	DOUT to DGND	DGND – 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Hgh-side power supply	AVDD to AGND	3	5.0	5.5	V
DVDD	Low-side power supply	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Input voltage before clipping output	$V_{IN} = V_{INP} – V_{SNSN}$		±1.25		V
V_{FSR}	Specified linear differential input voltage	$V_{IN} = V_{INP} – V_{SNSN}$	–1		1	V
DIGITAL I/O						
V_{IO}	Digital input/output voltage		0		DVDD	V
f_{CLKIN}	Input clock frequency		5	10	11	MHz
t_{HIGH}	Input clock high time		40	50	110	ns
t_{LOW}	Input clock low time		40	50	110	ns
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

6.4 Thermal Information (D Package)

THERMAL METRIC[1]		D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Thermal Information (DWV Package)

THERMAL METRIC(1)		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5V	67	mW
P_{D1}	Maximum power dissipation (high-side)	AVDD = 5.5V	39	mW
P_{D2}	Maximum power dissipation (low-side)	DVDD = 5.5V	28	mW

6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 4	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 4	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1130	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	800	V_{RMS}
		At DC voltage	1130	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	4250	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7), $V_{pd(ini)} = V_{IOTM} = V_{pd(m)}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 6000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.9 Safety-Related Certifications (Basic Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ; 6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Basic insulation	Single protection
Certificate number: Pending	File number: Pending

6.10 Safety-Related Certifications (Reinforced Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending

6.11 Safety Limiting Values (D Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 116.5°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			195	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 116.5°C/W, T_J = 150°C, T_A = 25°C			1070	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.12 Safety Limiting Values (DWV Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 102.8°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			220	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C			1210	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.13 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0V to 5.5V, DVDD = 2.7V to 5.5V, V_{INP} = –1V to +1V, and SNSN = AGND; typical specifications are at T_A = 25°C, AVDD = 5V, DVDD = 3.3V, and f_{CLKIN} = 10MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
C_{IN}	Input capacitance	f_{CLKIN} = 10MHz		2		pF
R_{IN}	Input resistance	INP pin to AGND, SNSN = AGND	0.1	1		GΩ
I_{IB}	Input bias current(1)	INP = AGND	–10	±3	10	nA
CMTI	Common-mode transient immunity		150			V/ns
DC ACCURACY						
E_O	Offset error	T_A = 25°C, INP = AGND	–0.9	±0.08	0.9	mV
TCE_O	Offset error temperature drift(3)			3.5	8.5	µV/°C
E_G	Gain error(1)	Initial, at T_A = 25°C, V_{INP} = 1V or V_{INP} = –1V	–0.25	±0.02	0.25	%
TCE_G	Gain error temperature drift(4)		–35	±10	35	ppm/°C
INL	Integral nonlinearity(2)	Resolution: 16 bits	–6	±1	6	LSB
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
PSRR	Power-supply rejection ratio	AVDD DC PSRR, IN = AGND, AVDD from 3.0V to 5.5V		–83		dB
		AVDD AC PSRR, IN = AGND, AVDD with10kHz / 100mV ripple		–63		
AC ACCURACY						
SNR	Signal-to-noise ratio	V_{IN} = $2V_{PP}$, f_{IN} = 1kHz	86	89		dB
SINAD	Signal-to-noise + distortion	V_{IN} = $2V_{PP}$, f_{IN} = 1kHz	77	88		dB
THD	Total harmonic distortion(5)	V_{IN} = $2V_{PP}$, f_{IN} = 1kHz		–91	–80	dB
DIGITAL INPUT (CMOS Logic With Schmitt-Trigger)						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD			7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 x DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 x DVDD	V
DIGITAL OUTPUT (CMOS)						
C_{LOAD}	Output load capacitance	f_{CLKIN} = 10MHz		15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –4mA	DVDD – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA			0.4	V
POWER SUPPLY						
I_{AVDD}	High-side supply current			5.3	7	mA
I_{DVDD}	Low-side supply current	C_{LOAD} = 15pF		3.6	5	mA
$AVDD_{UV}$	High-side undervoltage detection threshold	AVDD rising	2.4	2.6	2.7	V
		AVDD falling	1.9	2.0	2.1	
$DVDD_{UV}$	Low-side undervoltage detection threshold	DVDD rising	2.3	2.5	2.7	V
		DVDD falling	1.9	2.0	2.1	

(1) The typical value includes one sigma statistical variation.
(2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(3) Offset error drift is calculated using the box method, as described by the following equation:
TCE_O = ($value_{MAX}$ - $value_{MIN}$) / TempRange
(4) Gain error drift is calculated using the box method, as described by the following equation:
TCE_G (ppm) = (($value_{MAX}$ - $value_{MIN}$) / (value x TempRange)) X 10^6
(5) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.

6.14 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_H	DOUT hold time after rising edge of CLKIN	C_{LOAD} = 15pF	10			ns
t_D	Rising edge of CLKIN to DOUT valid delay	C_{LOAD} = 15pF			35	ns
t_r	DOUT rise time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		2.5	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		3.2	6	
t_f	DOUT fall time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		2.2	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		2.9	6	
t_{START}	Device start-up time	AVDD step from 0 to 3.0V with AVDD ≥ 2.7V to bitstream valid, 0.1% settling		30		µs

6.15 Timing Diagrams

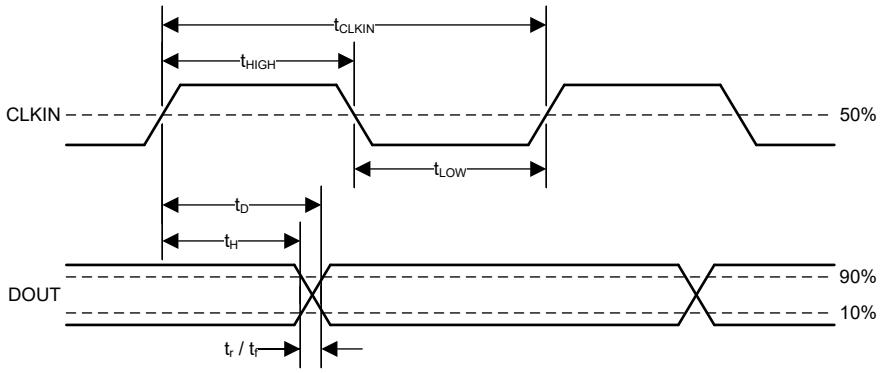


図 6-1. Digital Interface Timing

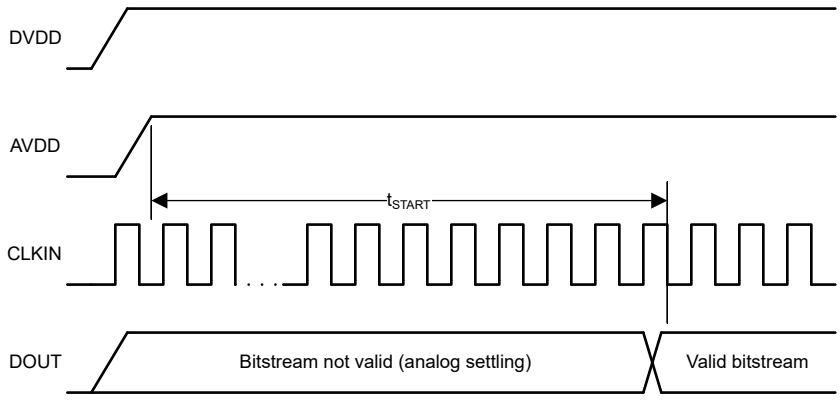


図 6-2. Device Start-Up Timing

6.16 Insulation Characteristics Curves

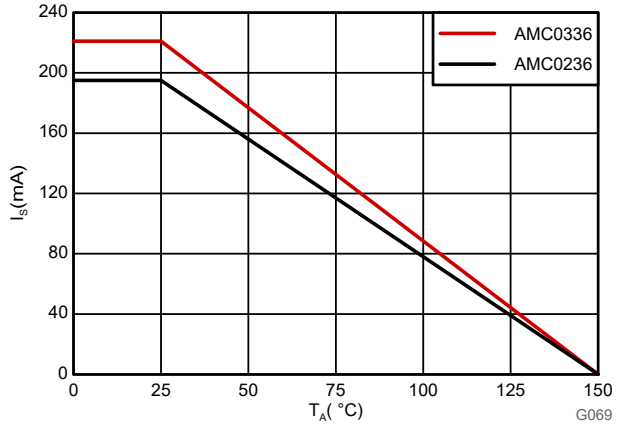


図 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE

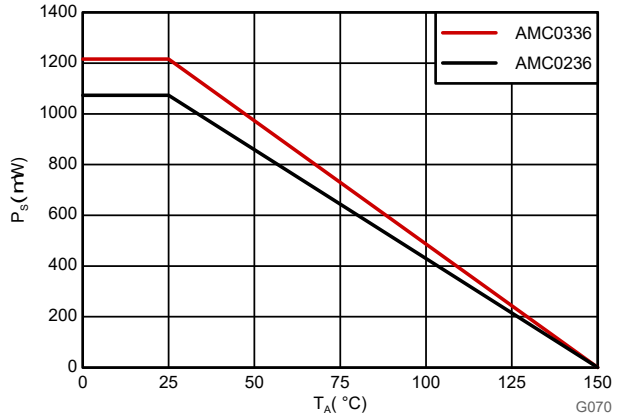
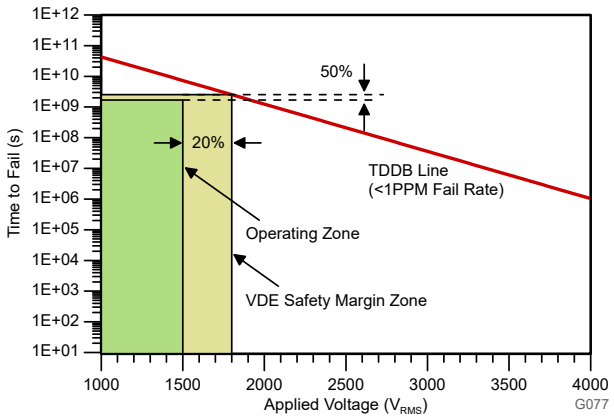


図 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V_{RMS}, projected operating lifetime ≥50 years

図 6-5. Isolation Capacitor Lifetime Projection

6.17 Typical Characteristics

at AVDD = 5 V, DVDD = 3.3 V, V_{INP} = –1 V to 1 V, SNSN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)

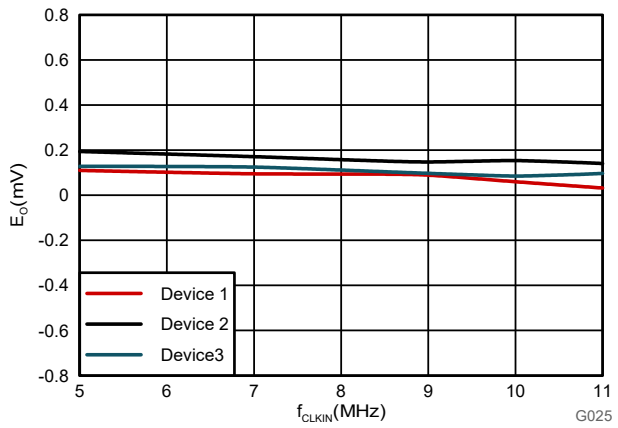


図 6-6. Offset Error vs Clock Frequency

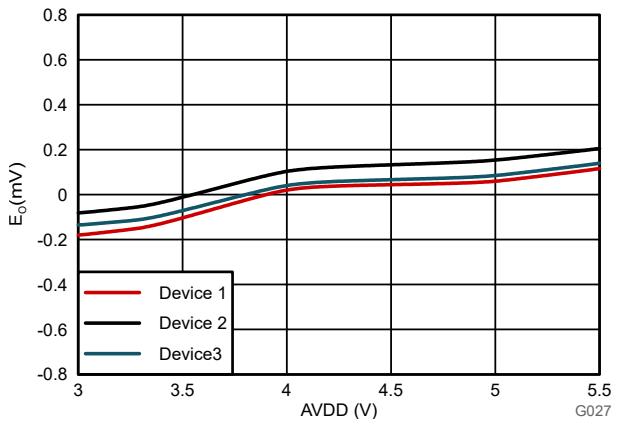


図 6-7. Offset Error vs High-Side Supply Voltage

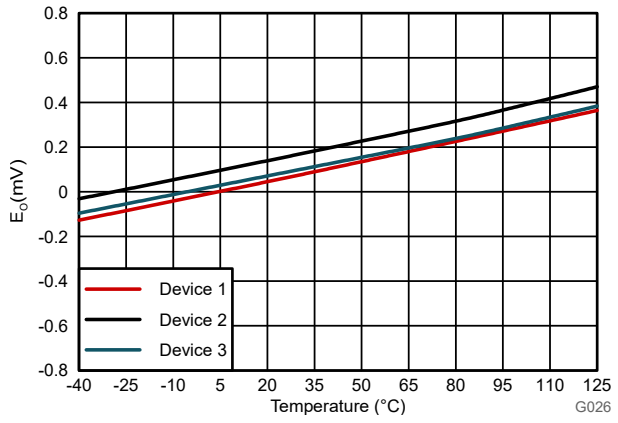


図 6-8. Offset Error vs Temperature

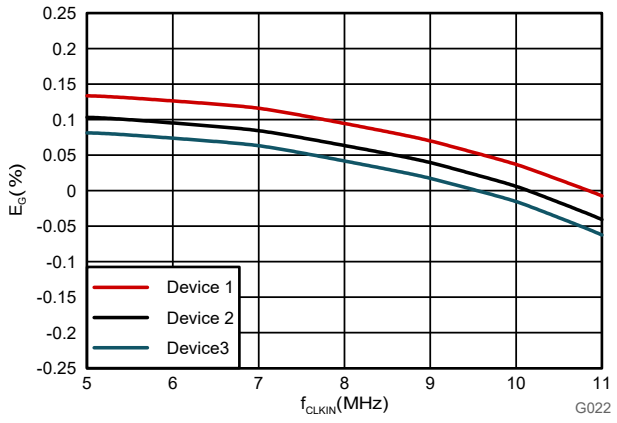


図 6-9. Gain Error vs Clock Frequency

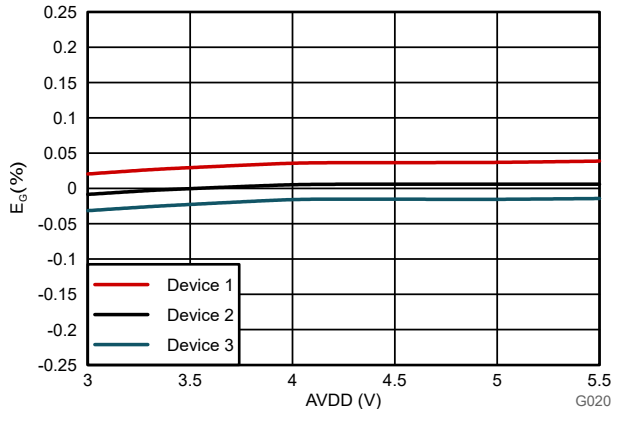


図 6-10. Gain Error vs High-Side Supply Voltage

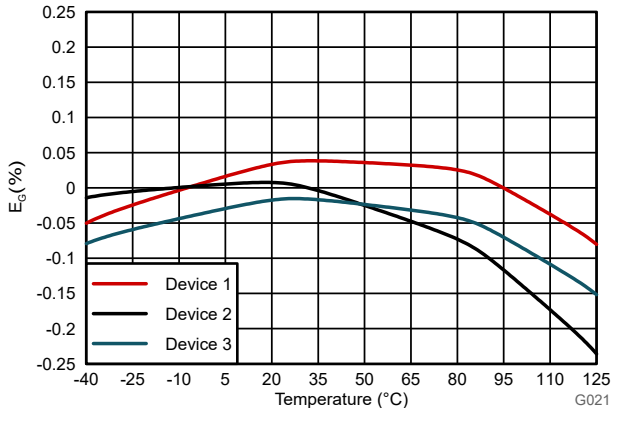
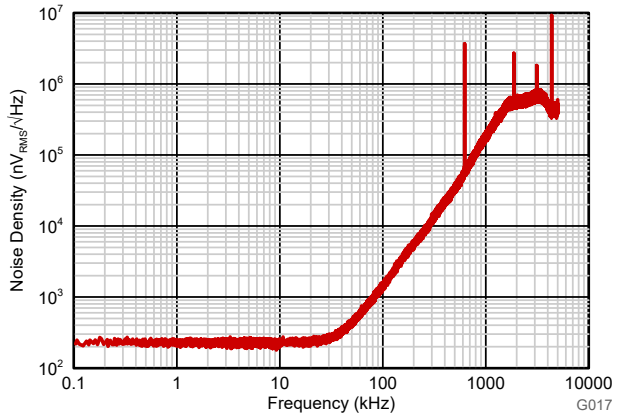


図 6-11. Gain Error vs Temperature

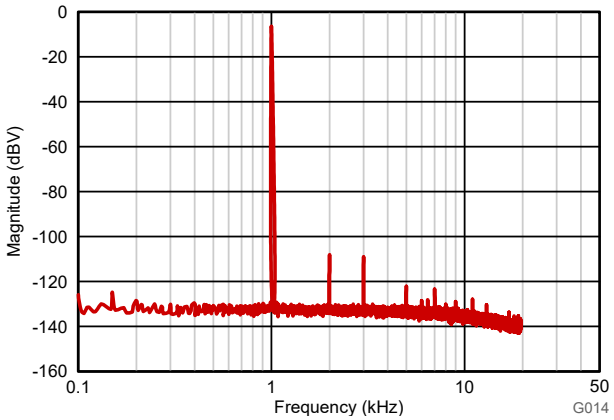
6.17 Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, V_{INP} = –1 V to 1 V, SNSN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)



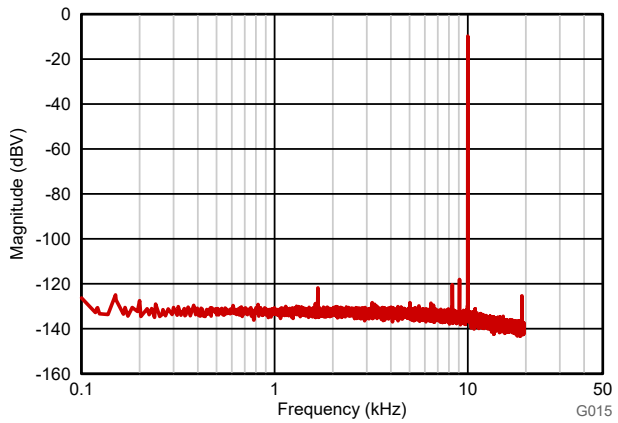
sinc^3, OSR = 1; Frequency bin-width equals 1Hz

図 6-12. Noise Density With Both Inputs Shorted to AGND



sinc^3, OSR = 256, V_{INP} = 2V_{PP}

図 6-13. Frequency Spectrum With 1-kHz Input Signal



sinc^3, OSR = 256, V_{INP} = 2V_{PP}

図 6-14. Frequency Spectrum With 10-kHz Input Signal

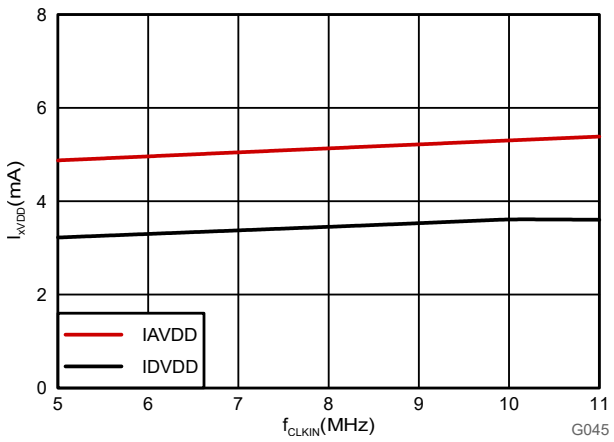


図 6-15. Supply Current vs Clock Frequency

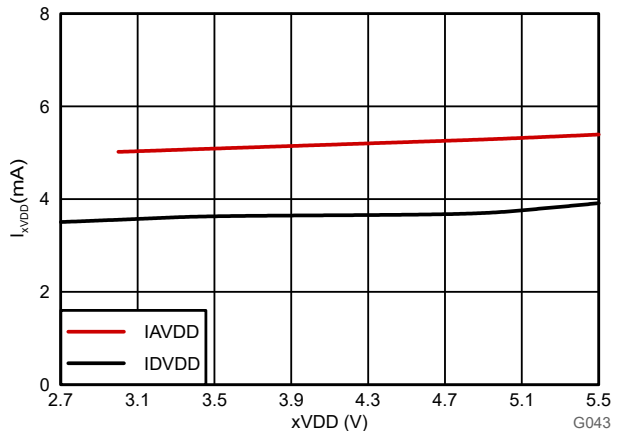


図 6-16. Supply Current vs Supply Voltage

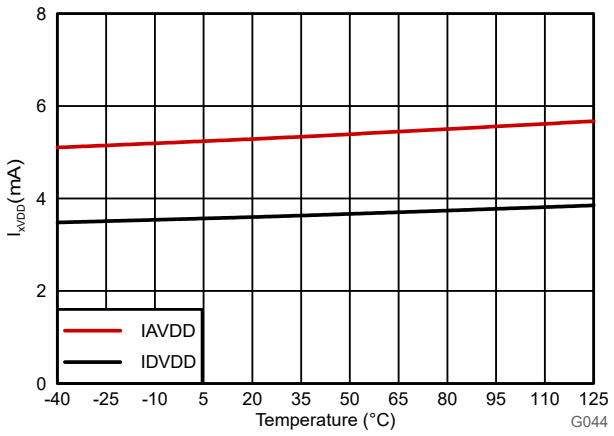


図 6-17. Supply Current vs Temperature

7 Detailed Description

7.1 Overview

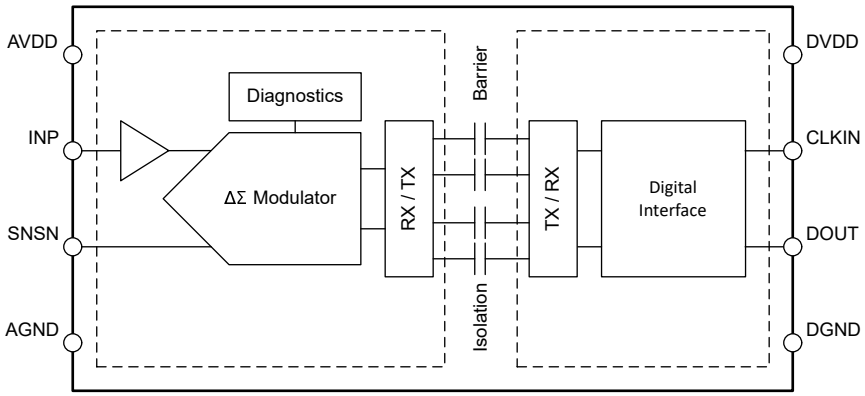
The AMC0x36 is a single-channel, second-order, CMOS, delta-sigma (ΔΣ) modulator with a high impedance input, designed for high resolution voltage measurements. The isolated output of the converter (DOUT) provides a stream of digital ones and zeros synchronous to the external clock applied to the CLKIN pin. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies; therefore, use a digital low-pass digital filter, such as a Sinc filter at the device output to increase overall performance. This filter also converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). Use a microcontroller (µC) or field-programmable gate array (FPGA) to implement the filter.

The overall performance (speed and resolution) depends on the selection of an appropriate oversampling ratio (OSR) and filter type. A higher OSR results in higher resolution while operating at a lower refresh rate. A lower OSR results in lower resolution, but provides data at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of analog-to-digital conversion results with a dynamic range exceeding 89dB with OSR = 256.

The silicon-dioxide (SiO_2) based capacitive isolation barrier supports a high level of magnetic field immunity; see the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The AMC0x36 uses an on-off keying (OOK) modulation scheme to transmit data across the isolation barrier. This modulation and the isolation barrier characteristics, result in high reliability in noisy environments and high common-mode transient immunity.

7.2 Functional Block Diagram

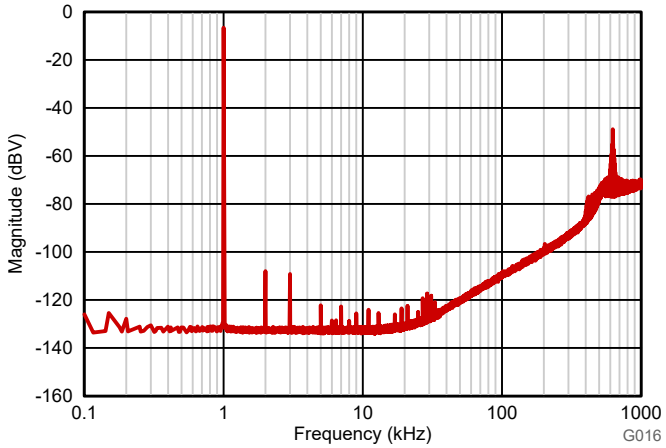


7.3 Feature Description

7.3.1 Analog Input

The high-impedance input buffer on the INP pin feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

For reduced offset and offset drift, the input buffer is chopper-stabilized with the chopping frequency set at $f_{CLKIN}/16$. 図 7-1 shows the spur at 625 kHz that is generated by the chopping frequency for a modulator clock of 10 MHz.



sinc^3 filter, OSR = 1, f_{CLKIN} = 10MHz, f_{IN} = 1kHz

図 7-1. Quantization Noise Shaping

There are two restrictions on the analog input signal. First, if the input voltage exceeds the value specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10mA. This limitation is caused by the device input electrostatic discharge (ESD) diodes turning on. Second, linearity and noise performance are specified only when the input voltage is within the linear full-scale range (V_{FSR}). V_{FSR} is specified in the *Recommended Operating Conditions* table.

7.3.2 Modulator

図 7-2 conceptualizes the second-order, switched-capacitor, feed-forward ΔΣ modulator implemented in the AMC0x36. The output V_5 of the 1-bit, digital-to-analog converter (DAC) is subtracted from the input voltage V_{IN} = (V_{INP} − V_{SNSN}). This subtraction provides an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage. The result or the second integration is an output voltage V_3 that is summed with the input signal V_{IN} and the output of the first integrator V_2. Depending on the value of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5. Thus, causing the integrators to progress in the opposite direction and forcing the integrator output value to track the average value of the input.

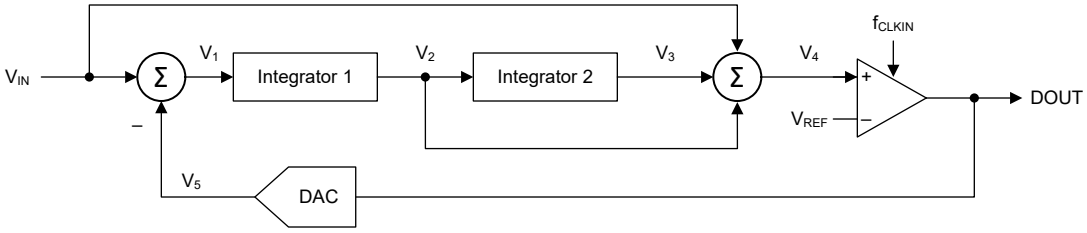


図 7-2. Block Diagram of the Second-Order Modulator

7.3.3 Isolation Channel Signal Transmission

The AMC0x36 uses an on-off keying (OOK) modulation scheme, as shown in 図 7-3, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) as illustrated in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0x36 is 480MHz.

The AMC0x36 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

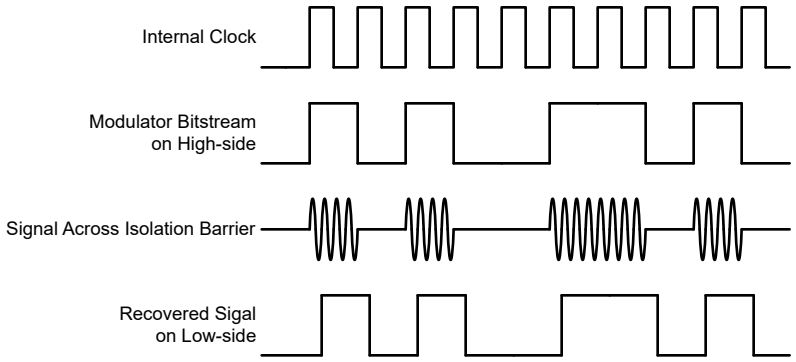


図 7-3. OOK-Based Modulation Scheme

7.3.4 Digital Output

An input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time. An input of 1V produces a stream of ones and zeros that are high 90.0% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982. An input of -1V produces a stream of ones and zeros that are high 10.0% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 6554. These input voltages are also the specified linear range of the AMC0x36. If the input voltage value exceeds this range, the output of the modulator shows increasing nonlinear behavior as the quantization noise increases. The modulator output clips with a constant stream of zeros at an input ≤-1.25V or with a constant stream of ones at an input ≥1.25V. In this case, however, the AMC0x36 generates a single 1 or 0 every 128 clock cycles to indicate proper device function. A single 1 is generated if the input is at negative fullscale and a 0 is generated if the input is at positive fullscale. See the *Output Behavior in Case of a Full-Scale Input* section for more details. 図 7-4 shows the input voltage versus the output modulator signal.

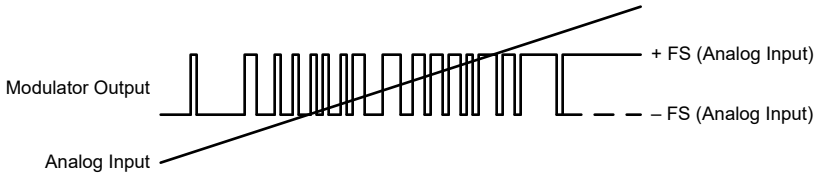


図 7-4. Modulator Output vs Analog Input

Calculate the density of ones in the output bitstream with 式 1 for any input voltage $V_{IN} = (V_{INP} – V_{SNSN})$ value. The only exception is a fullscale input signal. See the *Output Behavior in Case of a Full-Scale Input* section.

$$\rho = (|V_{Clipping}| + V_{IN}) / (2 \times V_{Clipping}) \quad (1)$$

7.3.4.1 Output Behavior in Case of a Full-Scale Input

If a fullscale input signal is applied to the AMC0x36, the device generates a single one or zero every 128 bits at DOUT. 図 7-5 shows a timing diagram of this process. A single 1 or 0 is generated depending on the actual polarity of the signal being sensed. A fullscale signal is defined as $|V_{INP} – V_{SNSN}| \geq |V_{Clipping}|$. In this way, differentiating between a missing AVDD and a fullscale input signal is possible on the system level. See the *Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB)* application note for code examples of diagnosing the digital bitstream.

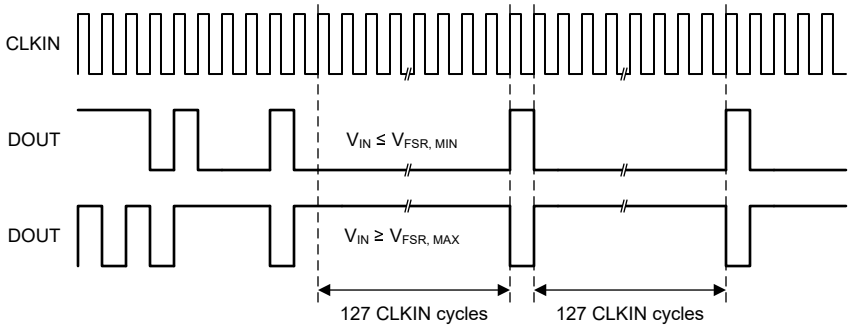


図 7-5. Fullscale Output of the AMC0x36

7.3.4.2 Output Behavior in Case of a Missing High-Side Supply

If the high-side supply (AVDD) is missing, the device provides a constant bitstream of logic 0's at the output, and DOUT is permanently low. 図 7-6 shows a timing diagram of this process. A one is not generated every 128 clock pulses, which differentiates this condition from a valid negative fullscale input. This feature helps identify high-side power-supply problems on the board. See the *Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB)* application note for code examples of diagnosing the digital bitstream.

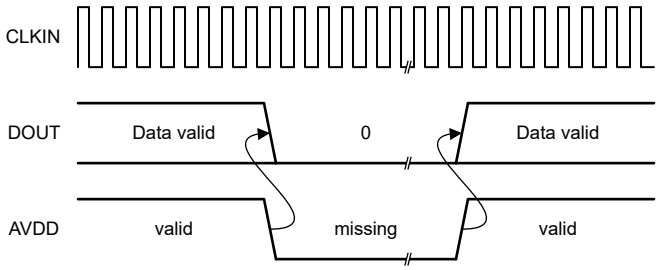


図 7-6. Output of the AMC0x36 in Case of a Missing High-Side Supply

7.4 Device Functional Modes

The AMC0x36 operates in one of the following states:

- OFF-state: The low-side of the device (DVDD) is below the $DVDD_{UV}$ threshold. The device is not responsive. DOUT はハイ インピーダンス状態。内部的に、DOUT および CLKIN は、ESD 保護ダイオードにより DVDD および DGND にクランプされます。
- Missing high-side supply: The low-side of the device (DVDD) is supplied and within *Recommended Operating Conditions* . The high-side supply (AVDD) is below the $AVDD_{UV}$ threshold. このデバイスは、Output Behavior in Case of a Missing High-Side Supply セクションで説明されているように、ロジック 0 の一定のビットストリームを出力します。
- Analog input overrange (positive fullscale input): AVDD and DVDD are within recommended operating conditions but the analog input voltage V_{IN} = (V_{INP} – V_{SNSN}) is above the maximum clipping voltage ($V_{Clipping, MAX}$). Output Behavior in Case of a Full-Scale Input セクションで説明しているように、このデバイスは 128 クロックサイクルごとにロジック 0 を出力します。
- Analog input underrange (negative fullscale input): AVDD and DVDD are within recommended operating conditions but the analog input voltage V_{IN} = (V_{INP} – V_{SNSN}) is below the minimum clipping voltage ($V_{Clipping, MIN}$). Output Behavior in Case of a Full-Scale Input セクションで説明しているように、このデバイスは 128 クロックサイクルごとにロジック 1 を出力します。
- Normal operation: AVDD, DVDD, and V_{IN} are within the recommended operating conditions. The device outputs a digital bitstream, as explained in the *Digital Output* section.

表 7-1 lists the operational modes.

表 7-1. Device Operational Modes

OPERATINAL MODE	AVDD	DVDD	V_{IN}	DEVICE RESPONSE
OFF	Don't care	V_{DVDD} < $DVDD_{UV}$	Don't care	DOUT はハイ インピーダンス状態。内部的に、DOUT および CLKIN は、ESD 保護ダイオードにより DVDD および DGND にクランプされます。
Missing high-side supply	V_{AVDD} < $AVDD_{UV}$	Valid(1)	Don't care	このデバイスは、Output Behavior in Case of a Missing High-Side Supply セクションで説明されているように、ロジック 0 の一定のビットストリームを出力します。
Input overrange	Valid(1)	Valid(1)	V_{IN} > $V_{Clipping, MAX}$	Output Behavior in Case of a Full-Scale Input セクションで説明しているように、このデバイスは 128 クロックサイクルごとにロジック 0 を出力します。
Input underrange	Valid(1)	Valid(1)	V_{IN} < $V_{Clipping, MIN}$	Output Behavior in Case of a Full-Scale Input セクションで説明しているように、このデバイスは 128 クロックサイクルごとにロジック 1 を出力します。
Normal operation	Valid(1)	Valid(1)	Valid(1)	Normal operation

(1) "Valid" denotes within the recommended operating conditions.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

AC-line powered power supplies are divided into two or more voltage domains that are galvanically isolated from each other. For example, the high-voltage domain includes the AC grid, DC-Link, and the power stage for power-factor-correction (PFC). The low-voltage domain includes the system controller and human interface. The PFC controller must measure the value of the AC line voltage while remaining galvanically isolated from the AC mains for safety reasons. With the high-impedance input and galvanically isolated output, the AMC0x36 enables this measurement.

8.2 Typical Application

図 8-1 illustrates a simplified schematic of a circuit that senses the line voltages of a three-phase AC system. All three voltages are measured against neutral. This allows the three AMC0x36 devices to share a common isolated power supply on the input side.

The AC line voltage on phase L1 is divided down to a ±1V level across the bottom resistor (RSNS) of a high-impedance resistive divider. The voltage across RSNS is sensed by the AMC0x36 (*Device 1*). On the opposite side of the isolation barrier *Device 1* outputs a serial bitstream that represents the L1-to-neutral voltage. In the same way *Device 2* and *Device 3* sense the L2 and L3 line voltages, respectively. A common AVDD supply is generated from the low-voltage side by an isolated DC/DC converter circuit. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

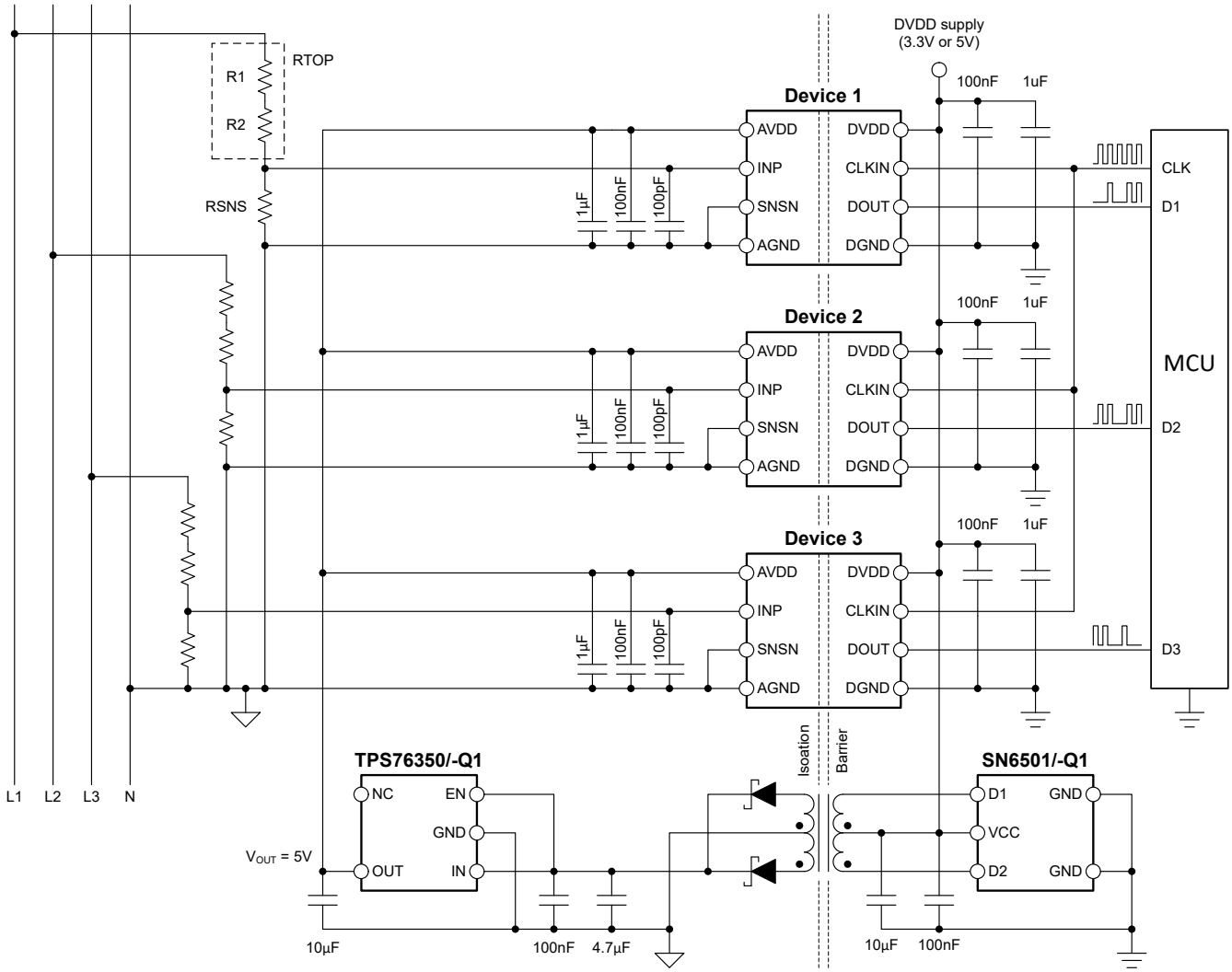


図 8-1. Using the AMC0x36 in a Typical Application

8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	VALUE
System input voltage (phase to neutral)	$230V_{RMS}$ ±10%, 50Hz
High-side supply voltage	5V
Low-side supply voltage	3.3V
Maximum resistor operating voltage	125V
Voltage drop across the sense resistor (RSNS) for a linear response	±1V (maximum)
Current through the resistive divider, I_{CROSS}	200µA (maximum)

8.2.2 Detailed Design Procedure

The peak input voltage is 230V x √2 x 1.1 = 360V. The 200µA maximum cross-current requirement determines that the total impedance of the resistive divider is 1.8 MΩ. The impedance of the resistive divider is dominated by the top resistors (shown exemplary as R1 and R2 in 図 8-1) and the voltage drop across RSNS can be neglected for a short time. The maximum allowed voltage drop per unit resistor is specified as 125V; therefore, the minimum number of unit resistors in the top portion of the resistive divider is 360V / 125V ≅ 3. The calculated unit value is 1.8MΩ / 3 = 600kΩ and the next closest value from the E96 series is 604kΩ.

Size RSNS such that the voltage drop at maximum input voltage (360V) equals the linear full-scale input voltage (V_{FSR}) of the AMC0x36. RSNS is calculated as RSNS = V_{FSR} / (V_{Peak} – V_{FSR}) × R_{TOP} where R_{TOP} is the total value of the top resistor string (3 × 604kΩ = 1.812MΩ). The resulting value for RSNS is 5.05kΩ. The next closest value from the E96 series is 4.99kΩ.

表 8-2 summarizes the design of the resistive divider.

表 8-2. Resistor Value Examples

PARAMETER	VALUE
Unit resistor value, R_{TOP}	604kΩ
Number of unit resistors in R_{TOP}	3
Sense resistor value, RSNS	4.99kΩ
Total resistance value (R_{TOP} + RSNS)	1.817MΩ
Resulting current through resistive divider, I_{CROSS}	198.1µA
Resulting full-scale voltage drop across sense resistor RSNS	989mV
Peak power dissipated in R_{TOP} unit resistor	23.7mW
Total peak power dissipated in resistive divider	71.3mW

8.2.2.1 Input Filter Design

Place a RC filter in front of the device to improve signal-to-noise performance of the signal path. Input noise with a frequency close to the ΔΣ modulator sampling frequency (typically 10MHz) is folded back into the low-frequency range by the modulator. The purpose of the RC filter is to attenuate high-frequency noise below the desired noise level of the measurement. In practice, a cutoff frequency that is two orders of magnitude lower than the modulator frequency yields good results.

Most voltage-sensing applications use high-impedance resistive dividers in front of the isolated modulator to scale down the input voltage. In this case, a single capacitor, as shown in 図 8-2, is sufficient to filter the input signal. For (R1 + R2) >> RSNS, the cut-off frequency of the input filter is 1 / (2 x π x RSNS x C5). For example, RSNS =10kΩ and C5 = 100pF results in a cutoff frequency of 160kHz.

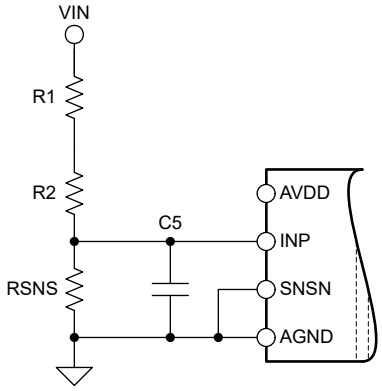


図 8-2. Input Filter

8.2.2.2 Bitstream Filtering

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). 式 2 represents a $sinc^3$-type filter, which is a very simple filter that is built with minimal effort and hardware.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is also done with a $sinc^3$ filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

An example code for implementing a $sinc^3$ filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

For modulator output bitstream filtering, a device from TI's C2000 or Sitara microcontroller families is recommended. These families support multichannel dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one path provides high-accuracy results for the control loop and the other provides a fast-response path for overcurrent detection.

A *delta sigma modulator filter calculator* is available for download at www.ti.com that aids in the filter design and selecting the right OSR and filter order to achieve the desired output resolution and filter response time.

8.2.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. 図 8-3 shows the ENOB of the AMC0x36 with different oversampling ratios.

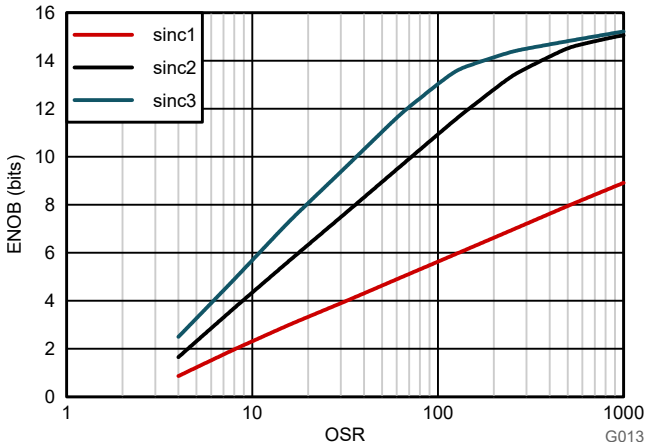


図 8-3. Measured Effective Number of Bits vs Oversampling Ratio

8.3 Best Design Practices

Do not leave the analog input (INP pin) of the AMC0x36 unconnected when the device is powered up. If the device input is left floating, the output of the device is not valid.

Do not connect protection diodes to the input (INP pin) of the AMC0x36. Diode leakage current potentially introduces significant measurement error especially at high temperatures. The input pin is protected against high voltages by the ESD protection circuit and the high impedance of the external resistive divider.

8.4 Power Supply Recommendations

In a typical application, the high-side power supply (AVDD) for the AMC0x36 is generated from the low-side supply (DVDD) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC0x36 does not require any specific power-up sequencing. The high-side power supply (AVDD) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (DVDD) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. 図 8-4 shows a decoupling diagram for the AMC0x36.

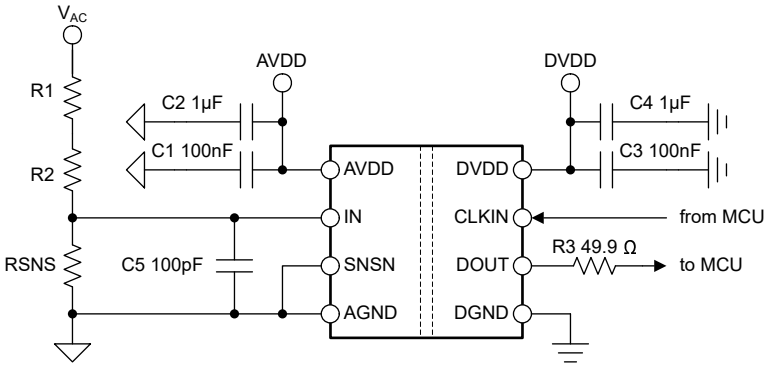


図 8-4. Decoupling of the AMC0x36

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

8.5 Layout

8.5.1 Layout Guidelines

The *Layout Example* section provides a layout recommendation showing the critical placement of the decoupling and filter capacitors. Decoupling and filter capacitors are placed as close as possible to the AMC0x36 input pins.

8.5.2 Layout Example

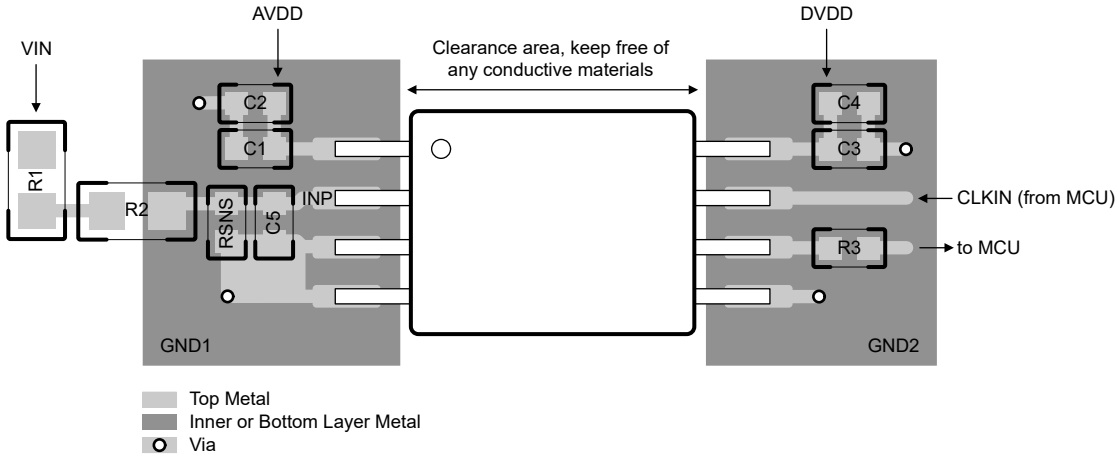


図 8-5. Recommended Layout of the AMC0x36

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB)* application report
- Texas Instruments, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application report
- Texas Instruments, *Delta Sigma Modulator Filter Calculator* design tool

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC0236DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C0236	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

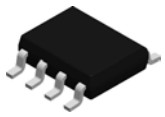
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

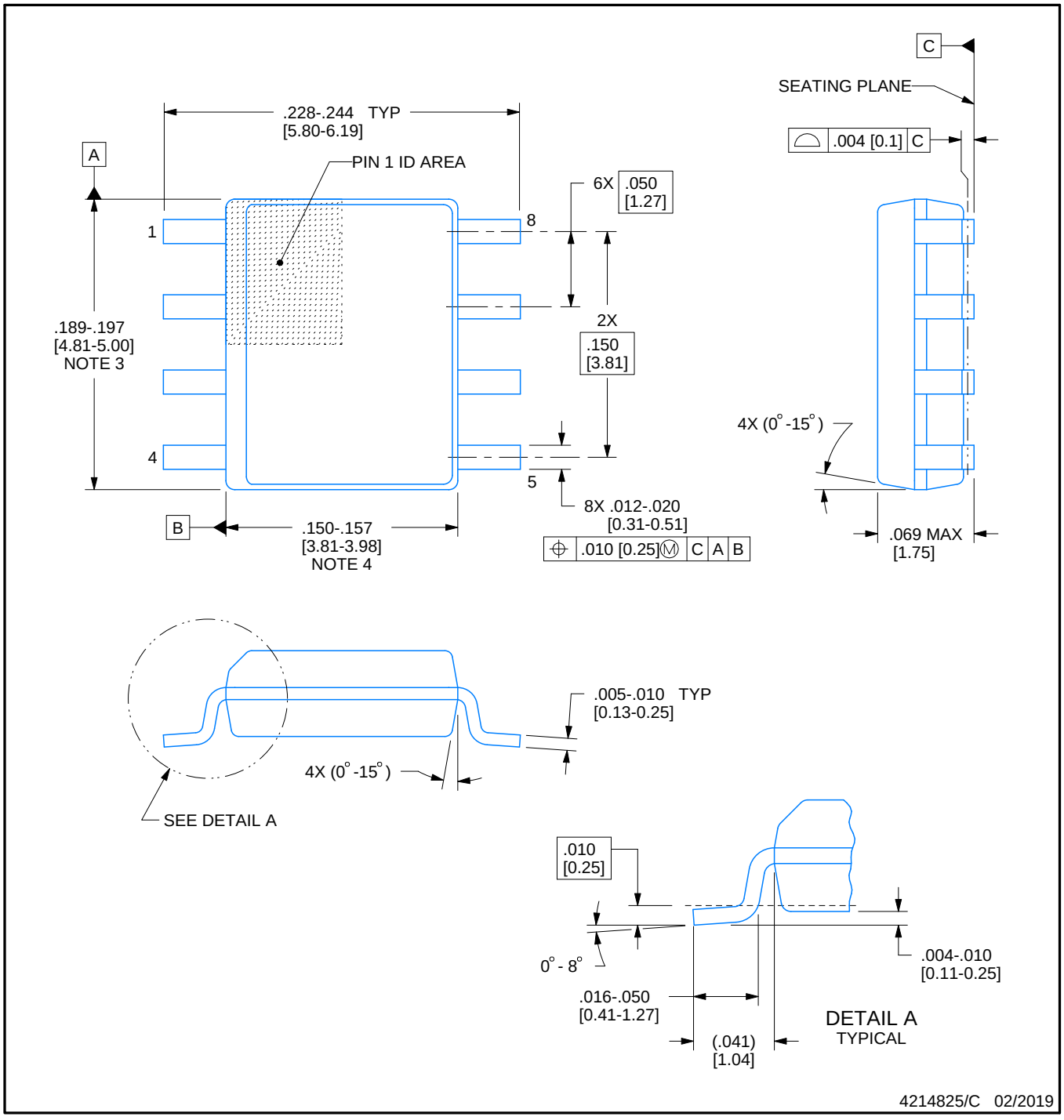


PACKAGE OUTLINE

D0008A

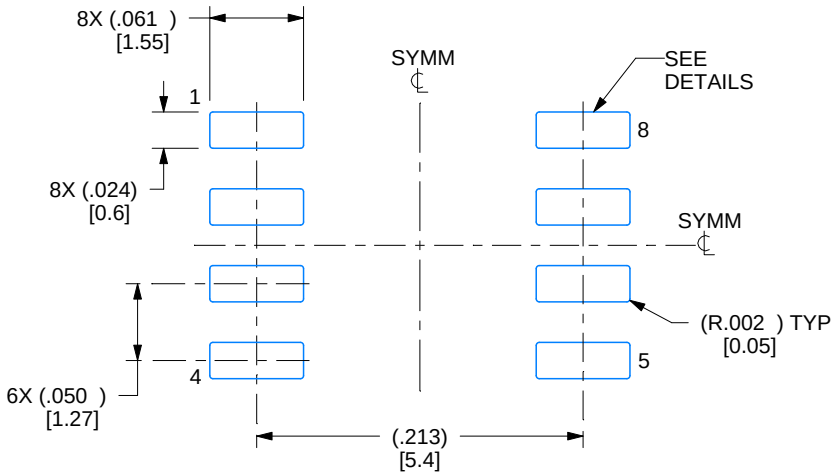
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

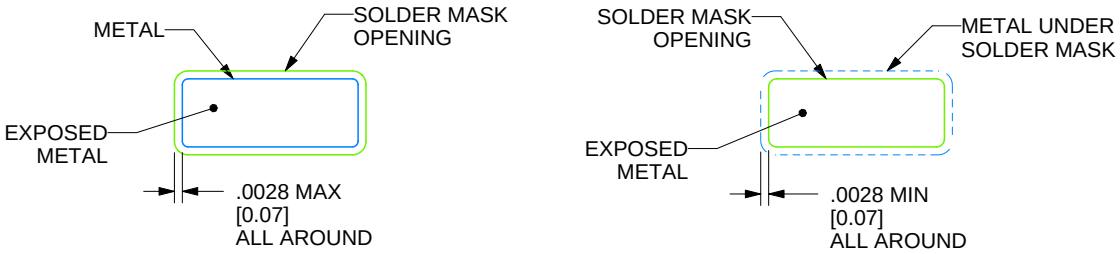


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

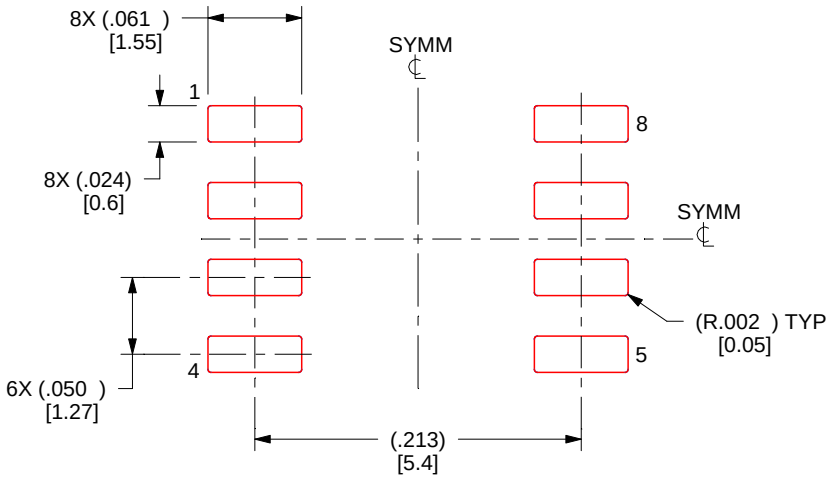
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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