



# 10-Bit, Octal-Channel ADC Up to 65MSPS

Check for Samples: [ADS5287](#)

## FEATURES

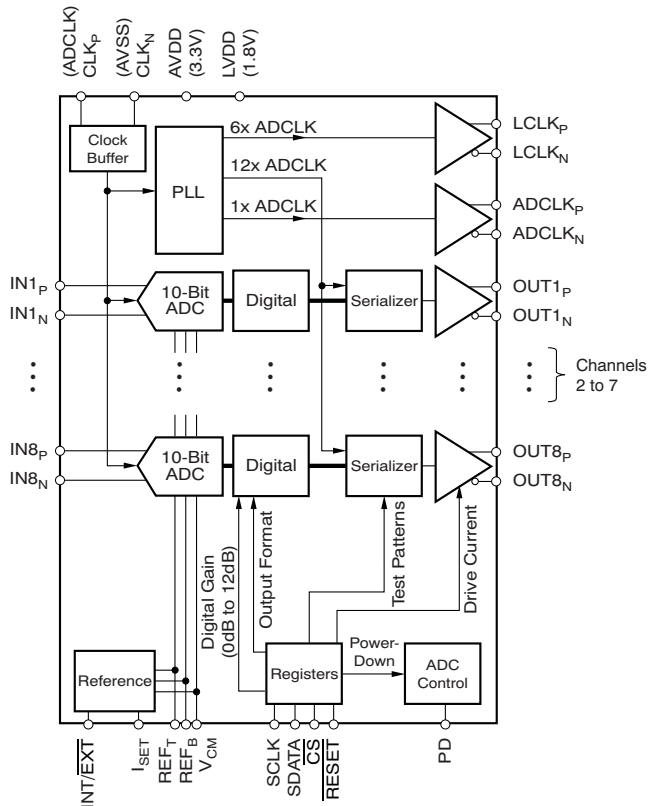
- **Speed and Resolution Grades:**
  - 10-bit, 65MSPS
- **Power Dissipation:**
  - 46mW/Channel at 30MSPS
  - 53mW/Channel at 40MSPS
  - 62mW/Channel at 50MSPS
  - 74mW/Channel at 65MSPS
- **61.7dBFS SNR at 10MHz IF**
- **Analog Input Full-Scale Range: 2V<sub>PP</sub>**
- **Low-Frequency Noise Suppression Mode**
- **6dB Overload Recovery in One Clock**
- **External and Internal (Trimmed) Reference**
- **3.3V Analog Supply, 1.8V Digital Supply**
- **Single-Ended or Differential Clock:**
  - Clock Duty Cycle Correction Circuit (DCC)
- **Programmable Digital Gain: 0dB to 12dB**
- **Serialized DDR LVDS Output**
- **Programmable LVDS Current Drive, Internal Termination**
- **Test Patterns for Enabling Output Capture**
- **Straight Offset Binary or Two's Complement Output**
- **Package Options:**
  - 9mm × 9mm QFN-64

## APPLICATIONS

- **Medical Imaging**
- **Wireless Base-Station Infrastructure**
- **Test and Measurement Instrumentation**

## DESCRIPTION

The ADS5287 is a high-performance, low-power, octal channel analog-to-digital converter (ADC). Available in a 9mm × 9mm QFN package, with serialized low-voltage differential signaling (LVDS) outputs and a wide variety of programmable features, the ADS5287 is highly customizable for a wide range of applications and offers an unprecedented level of system integration. An application note, XAPP774 (available at [www.xilinx.com](http://www.xilinx.com)), describes how to interface the serial LVDS outputs of TI's ADCs to Xilinx® field-programmable gate arrays (FPGAs). The ADS5287 is specified over the industrial temperature range of –40°C to +85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**RELATED PRODUCTS**

MODEL	RESOLUTION (BITS)	SAMPLE RATE (MSPS)	CHANNELS
<a href="#">ADS5281</a>	12	50	8
<a href="#">ADS5282</a>	12	65	8
<a href="#">ADS5287</a>	10	65	8
<a href="#">ADS5270</a>	12	40	8
<a href="#">ADS5271</a>	12	50	8
<a href="#">ADS5272</a>	12	65	8
<a href="#">ADS5273</a>	12	70	8
<a href="#">ADS5242</a>	12	65	4

**Table 1. ORDERING INFORMATION<sup>(1)</sup> <sup>(2)</sup>**

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY <sup>(3)</sup>
ADS5287	QFN-64	RGC	-40°C to +85°C	AZ5287	ADS5287IRGCT	Tape and Reel
					ADS5287IRGCR	Tape and Reel

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) These devices meet the following planned eco-friendly classification:  
**Green (RoHS and No Sb/Br):** Texas Instruments defines *Green* to mean Pb-free (RoHS compatible) and free of bromine (Br)- and antimony (Sb)-based flame retardants. Refer to the [Quality and Lead-Free \(Pb-Free\) Data](#) web site for more information. These devices have a Cu NiPdAu lead/ball finish.
- (3) Refer to the Package Option Addendum at the end of this document for specific transport media and quantity information.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range, unless otherwise noted.

	ADS5287	UNIT
Supply voltage range, AVDD	-0.3 to +3.9	V
Supply voltage range, LVDD	-0.3 to +2.2	V
Voltage between AVSS and LVSS	-0.3 to +0.3	V
External voltage applied to REF <sub>T</sub> pin	-0.3 to +3	V
External voltage applied to REF <sub>B</sub> pin	-0.3 to +2	V
Voltage applied to analog input pins	-0.3 to minimum [3.6, (AVDD + 0.3)]	V
Voltage applied to digital input pins	-0.3 to minimum [3.9, (AVDD + 0.3)]	V
Peak solder temperature	+260	°C
Junction temperature	+125	°C
Storage temperature range	-65 to +150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to *absolute maximum conditions* for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	ADS5287			UNIT
	MIN	TYP	MAX	
<b>SUPPLIES, ANALOG INPUTS, AND REFERENCE VOLTAGES</b>				
AVDD Analog supply voltage	3.0	3.3	3.6	V
LVDD Digital supply voltage	1.7	1.8	1.9	V
Differential input voltage range		2		V <sub>PP</sub>
Input common-mode voltage		V <sub>CM</sub> ± 0.05		V
REF <sub>T</sub> External reference mode		2.5		V
REF <sub>B</sub> External reference mode		0.5		V
<b>CLOCK INPUTS</b>				
ADCLK input sample rate 1/ t <sub>c</sub>	10		50, 65	MSPS
Input clock amplitude differential (V <sub>CLKP</sub> –V <sub>CLKN</sub> ) peak-to-peak				
Sine wave, ac-coupled		3.0		V <sub>PP</sub>
LVPECL, ac-coupled		1.6		V <sub>PP</sub>
LVDS, ac-coupled		0.7		V <sub>PP</sub>
Input clock CMOS, single-ended (V <sub>CLKP</sub> )				
V <sub>IL</sub>			0.6	V
V <sub>IH</sub>	2.2			V
Input clock duty cycle		50		%
<b>DIGITAL OUTPUTS</b>				
ADCLK <sub>P</sub> and ADCLK <sub>N</sub> outputs (LVDS)	10	1x (sample rate)	50, 65	MHz
LCLK <sub>P</sub> and LCLK <sub>N</sub> outputs (LVDS)	60	6x (sample rate)	300, 390	MHz
C <sub>LOAD</sub> Maximum external capacitance from each pin to LVSS		5		pF
R <sub>LOAD</sub> Differential load resistance between the LVDS output pairs		100		Ω
T <sub>A</sub> Operating free-air temperature	–40		+85	°C

**INITIALIZATION REGISTERS**

If the analog input is ac-coupled, the following registers must be written to in the order listed below.

	ADDRESS (hex)	DATA (hex)
Initialization Register 1	01	0010
Initialization Register 5	E2	00C0

To disable the PLL configuration switching (especially useful in systems where a system-level timing calibration is done once after power-up), the following registers must be written to in the order listed below. Also, see section [PLL Operation Across Sampling Frequency](#).

	ADDRESS (hex)	DATA (hex)
For 10 ≤ F <sub>s</sub> ≤ 25 <sup>(1)</sup>	E3	0060
For 15 ≤ F <sub>s</sub> ≤ 45 <sup>(1)</sup>	E3	00A0

(1) where F<sub>s</sub> = sampling clock frequency

## DIGITAL CHARACTERISTICS

DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. At  $C_{LOAD} = 5\text{pF}^{(1)}$ ,  $I_{OUT} = 3.5\text{mA}^{(2)}$ ,  $R_{LOAD} = 100\Omega^{(2)}$ , and no internal termination, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS5287			UNIT
		MIN	TYP	MAX	
<b>DIGITAL INPUTS</b>					
High-level input voltage		1.4			V
Low-level input voltage				0.3	V
High-level input current			33		$\mu\text{A}$
Low-level input current			-33		$\mu\text{A}$
Input capacitance			3		pF
<b>LVDS OUTPUTS</b>					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, $ V_{OD} $			350		mV
$V_{OS}$ output offset voltage	Common-mode voltage of $OUT_P$ and $OUT_N$		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1)  $C_{LOAD}$  is the effective external single-ended load capacitance between each output pin and ground.

(2)  $I_{OUT}$  refers to the LVDS buffer current setting;  $R_{LOAD}$  is the differential load resistance between the LVDS output pair.

## ELECTRICAL CHARACTERISTICS

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = +85^{\circ}\text{C}$ ,  $AVDD = 3.3\text{V}$ ,  $LVDD = 1.8\text{V}$ , clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode,  $I_{SET}$  resistor = 56.2k $\Omega$ , and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

PARAMETER	TEST CONDITIONS	ADS5287			UNIT	
		MIN	TYP	MAX		
<b>INTERNAL REFERENCE VOLTAGES</b>						
$V_{REFB}$	Reference bottom		0.5		V	
$V_{REFT}$	Reference top		2.5		V	
	$V_{REFT} - V_{REFB}$	1.95	2.0	2.05	V	
$V_{CM}$	Common-mode voltage (internal)	1.425	1.5	1.575	V	
	$V_{CM}$ output current		$\pm 2$		mA	
<b>EXTERNAL REFERENCE VOLTAGES</b>						
$V_{REFB}$	Reference bottom	0.4	0.5	0.6	V	
$V_{REFT}$	Reference top	2.4	2.5	2.6	V	
	$V_{REFT} - V_{REFB}$	1.9	2.0	2.1	V	
<b>ANALOG INPUT</b>						
	Differential input voltage range		2.0		$V_{PP}$	
	Differential input capacitance		3		pF	
	Analog input bandwidth		520		MHz	
	Analog input common-mode range	DC-coupled input	$V_{CM} \pm 0.05$		V	
	Analog input common-mode current	Per input pin per MSPS of sampling speed	2.5		$\mu\text{A}/\text{MHz}$ per pin	
	Voltage overload recovery time	Recovery from 6dB overload to within 1% accuracy	1		Clock cycle	
	Voltage overload recovery repeatability	Standard deviation seen on a periodic first data within full-scale range in a 6dB overloaded sine wave	1		LSB	
<b>DC ACCURACY</b>						
	Offset error		-1.25	$\pm 0.2$	+1.25	%FS
	Offset error temperature coefficient <sup>(1)</sup>			$\pm 5$		ppm/ $^{\circ}\text{C}$
	Channel gain error	Excludes error in internal reference		-0.8		%FS
	Channel gain error temperature coefficient	Excludes temperature coefficient of internal reference		$\pm 10$		ppm/ $^{\circ}\text{C}$
	Internal reference error temperature coefficient <sup>(2)</sup>			$\pm 15$		ppm/ $^{\circ}\text{C}$
DC PSRR	DC power-supply rejection ratio <sup>(3)</sup>			1.5		mV/V
<b>POWER-DOWN MODES</b>						
	Power in complete power-down mode			45		mW
	Power in partial power-down mode	Clock at 65MSPS		135		mW
	Power with no clock			88		mW
<b>DYNAMIC PERFORMANCE</b>						
	Crosstalk	5MHz full-scale signal applied to seven channels, measurement taken on channel with no input signal		-90		dBc
	Two-tone, third-order intermodulation distortion	$f_1 = 9.5\text{MHz}$ at -7dBFS $f_2 = 10.2\text{MHz}$ at -7dBFS		-92		dBFS
<b>DC ACCURACY</b>						
	No missing codes			Assured		
DNL	Differential nonlinearity		-0.55	$\pm 0.1$	+0.55	LSB
INL	Integral nonlinearity		-1	$\pm 0.1$	+1	LSB
<b>POWER SUPPLY—INTERNAL REFERENCE MODE</b>						

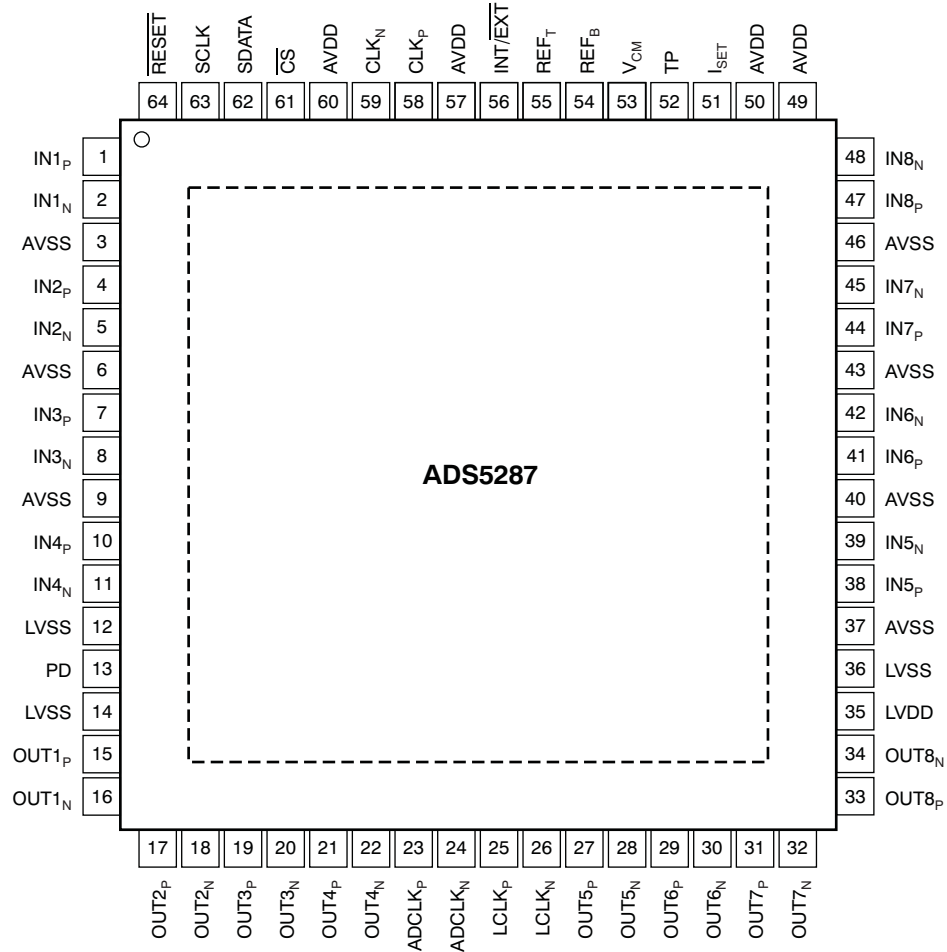
- (1) The offset temperature coefficient in ppm/ $^{\circ}\text{C}$  is defined as  $(O_1 - O_2) \times 10^6 / (T_1 - T_2) / 1024$ , where  $O_1$  and  $O_2$  are the offset codes in LSB at the two extreme temperatures,  $T_1$  and  $T_2$ .
- (2) The internal reference temperature coefficient is defined as  $(REF_1 - REF_2) \times 10^6 / (T_1 - T_2) / 2$ , where  $REF_1$  and  $REF_2$  are the internal reference voltages ( $V_{REFT} - V_{REFB}$ ) at the two extreme temperatures,  $T_1$  and  $T_2$ .
- (3) DC PSRR is defined as the ratio of the change in the ADC output (expressed in mV) to the change in supply voltage (in volts).

## ELECTRICAL CHARACTERISTICS (continued)

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = +85^{\circ}\text{C}$ ,  $AVDD = 3.3\text{V}$ ,  $LVDD = 1.8\text{V}$ , clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode,  $I_{SET}$  resistor = 56.2k $\Omega$ , and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

PARAMETER		TEST CONDITIONS	ADS5287			UNIT
			MIN	TYP	MAX	
IAVDD	Analog supply current			139	165	mA
ILVDD	Digital current	Zero input to all channels		87	97	mA
	Total power			615	719.1	mW
	Incremental power saving	Obtained on powering down one channel at a time		61		mW
<b>POWER SUPPLY—EXTERNAL REFERENCE MODE</b>						
IAVDD	Analog supply current			132		mA
ILVDD	Digital current	Zero input to all channels		87		mA
	Total power			592		mW
	Incremental power saving	Obtained on powering down one channel at a time		59		mW
<b>EXTERNAL REFERENCE LOADING</b>						
	Switching current	Current drawn by the eight ADCs from the external reference voltages; sourcing for $REF_T$ , sinking for $REF_B$ .		3.5		mA
<b>DYNAMIC CHARACTERISTICS</b>						
SFDR	Spurious-free dynamic range	$f_{IN} = 5\text{MHz}$ , single-ended clock	72	85		dBc
		$f_{IN} = 30\text{MHz}$ , differential clock		80		dBc
HD2	Magnitude of second harmonic	$f_{IN} = 5\text{MHz}$ , single-ended clock	72	85		dBc
		$f_{IN} = 30\text{MHz}$ , differential clock		82		dBc
HD3	Magnitude of third harmonic	$f_{IN} = 5\text{MHz}$ , single-ended clock	72	85		dBc
		$f_{IN} = 30\text{MHz}$ , differential clock		80		dBc
THD	Total harmonic distortion	$f_{IN} = 5\text{MHz}$ , single-ended clock	70	80		dBc
		$f_{IN} = 30\text{MHz}$ , differential clock		78		dBc
SNR	Signal-to-noise ratio	$f_{IN} = 5\text{MHz}$ , single-ended clock	60.5	61.7		dBc
		$f_{IN} = 30\text{MHz}$ , differential clock		61.7		dBc
SINAD	Signal-to-noise and distortion	$f_{IN} = 5\text{MHz}$ , single-ended clock	60.4	61.6		dBc
		$f_{IN} = 30\text{MHz}$ , differential clock		61.6		dBc

## PIN CONFIGURATION

**QFN-64 PowerPAD™  
TOP VIEW**

**Table 2. PIN DESCRIPTIONS: QFN-64**

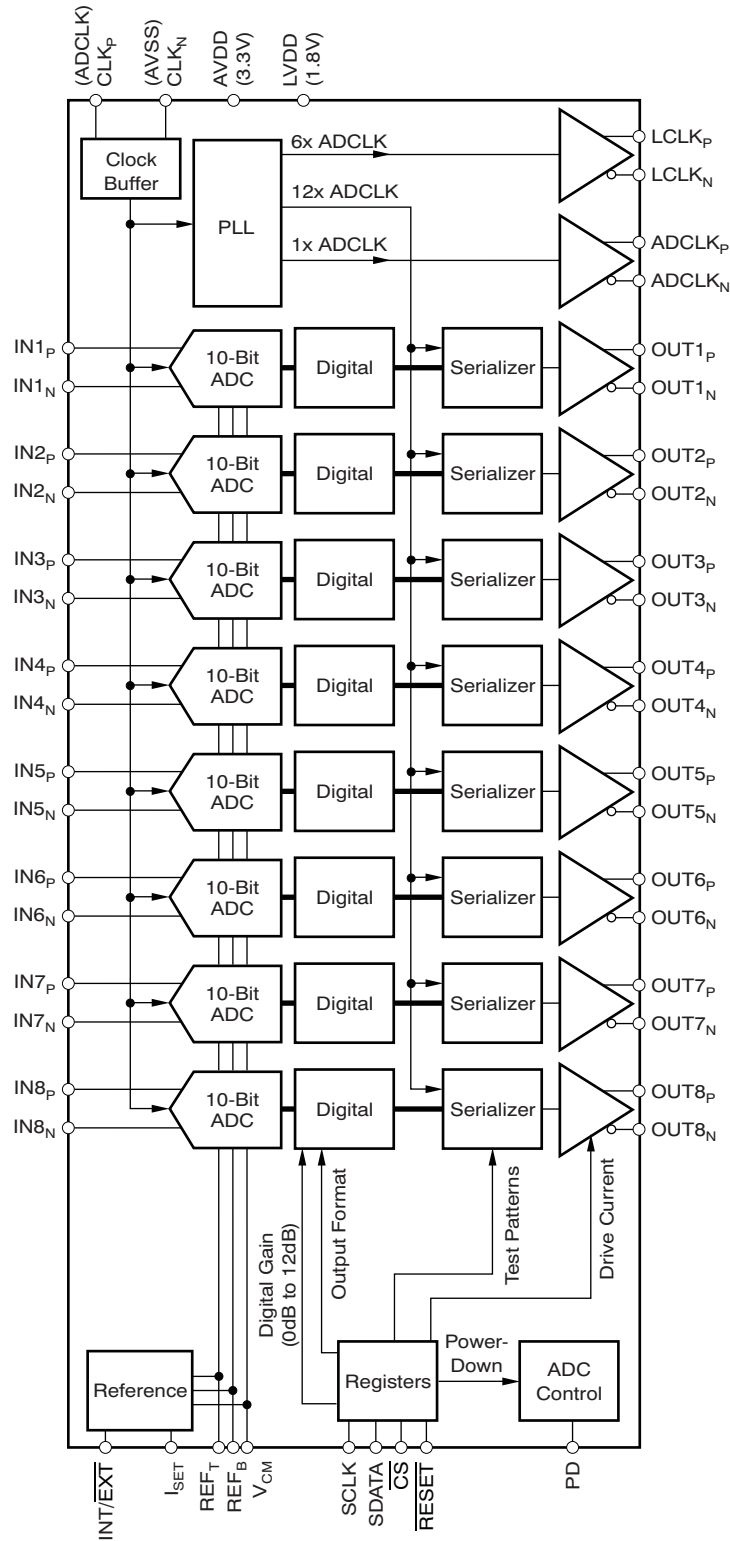
PIN NAME	DESCRIPTION	PIN NUMBER	# OF PINS
ADCLK <sub>N</sub>	LVDS frame clock (1X)—negative output	24	1
ADCLK <sub>P</sub>	LVDS frame clock (1X)—positive output	23	1
AVDD	Analog power supply, 3.3V	49, 50, 57, 60	4
AVSS	Analog ground	3, 6, 9, 37, 40, 43, 46	7
CLK <sub>N</sub>	Negative differential clock input Tie CLK <sub>N</sub> to 0V for a single-ended clock	59	1
CLK <sub>P</sub>	Positive differential clock input	58	1
$\overline{CS}$	Serial enable chip select—active low digital input	61	1
IN1 <sub>N</sub>	Negative differential input signal, channel 1	2	1
IN1 <sub>P</sub>	Positive differential input signal, channel 1	1	1
IN2 <sub>N</sub>	Negative differential input signal, channel 2	5	1
IN2 <sub>P</sub>	Positive differential input signal, channel 2	4	1
IN3 <sub>N</sub>	Negative differential input signal, channel 3	8	1
IN3 <sub>P</sub>	Positive differential input signal, channel 3	7	1
IN4 <sub>N</sub>	Negative differential input signal, channel 4	11	1
IN4 <sub>P</sub>	Positive differential input signal, channel 4	10	1

**Table 2. PIN DESCRIPTIONS: QFN-64 (continued)**

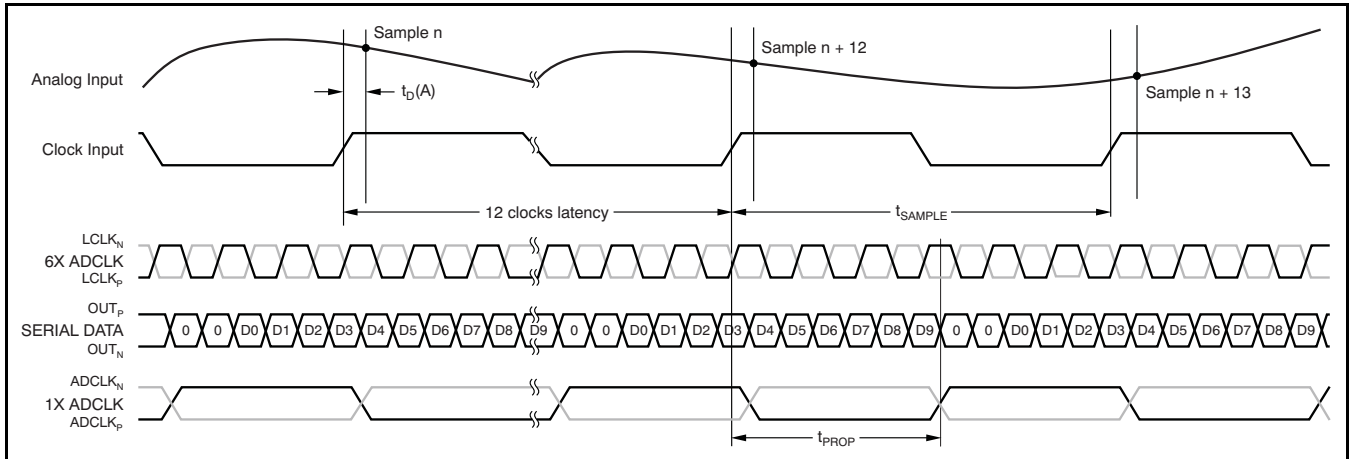
PIN NAME	DESCRIPTION	PIN NUMBER	# OF PINS
IN5 <sub>N</sub>	Negative differential input signal, channel 5	39	1
IN5 <sub>P</sub>	Positive differential input signal, channel 5	38	1
IN6 <sub>N</sub>	Negative differential input signal, channel 6	42	1
IN6 <sub>P</sub>	Positive differential input signal, channel 6	41	1
IN7 <sub>N</sub>	Negative differential input signal, channel 7	45	1
IN7 <sub>P</sub>	Positive differential input signal, channel 7	44	1
IN8 <sub>N</sub>	Negative differential input signal, channel 8	48	1
IN8 <sub>P</sub>	Positive differential input signal, channel 8	47	1
INT/EXT	Internal/external reference mode select input	56	1
I <sub>SET</sub>	Bias pin—56.2kΩ to ground	51	1
LCLK <sub>N</sub>	LVDS bit clock (6X)—negative output	26	1
LCLK <sub>P</sub>	LVDS bit clock (6X)—positive output	25	1
LVDD	Digital and I/O power supply, 1.8V	35	1
LVSS	Digital ground	12, 14, 36	3
OUT1 <sub>N</sub>	LVDS channel 1—negative output	16	1
OUT1 <sub>P</sub>	LVDS channel 1—positive output	15	1
OUT2 <sub>N</sub>	LVDS channel 2—negative output	18	1
OUT2 <sub>P</sub>	LVDS channel 2—positive output	17	1
OUT3 <sub>N</sub>	LVDS channel 3—negative output	20	1
OUT3 <sub>P</sub>	LVDS channel 3—positive output	19	1
OUT4 <sub>N</sub>	LVDS channel 4—negative output	22	1
OUT4 <sub>P</sub>	LVDS channel 4—positive output	21	1
OUT5 <sub>N</sub>	LVDS channel 5—negative output	28	1
OUT5 <sub>P</sub>	LVDS channel 5—positive output	27	1
OUT6 <sub>N</sub>	LVDS channel 6—negative output	30	1
OUT6 <sub>P</sub>	LVDS channel 6—positive output	29	1
OUT7 <sub>N</sub>	LVDS channel 7—negative output	32	1
OUT7 <sub>P</sub>	LVDS channel 7—positive output	31	1
OUT8 <sub>N</sub>	LVDS channel 8—negative output	34	1
OUT8 <sub>P</sub>	LVDS channel 8—positive output	33	1
PD	Power-down input	13	1
REF <sub>B</sub>	Negative reference input/output	54	1
REF <sub>T</sub>	Positive reference input/output	55	1
RESET	Active low RESET input	64	1
SCLK	Serial clock input	63	1
SDATA	Serial data input	62	1
TP	Test pin, do not use	52	1
V <sub>CM</sub>	Common-mode output pin, 1.5V output	53	1



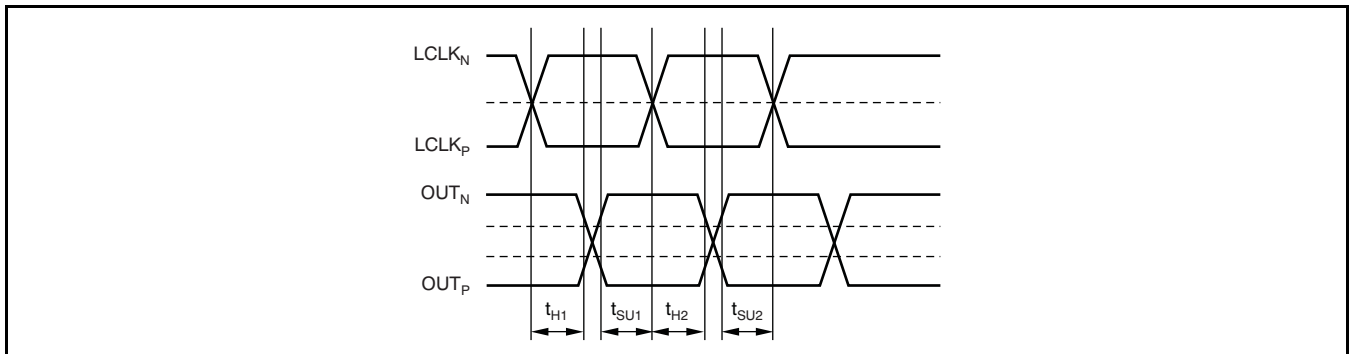
FUNCTIONAL BLOCK DIAGRAM



**LVDS TIMING DIAGRAM**



**DEFINITION OF SETUP AND HOLD TIMES**



$$t_{SU} = \min(t_{SU1}, t_{SU2})$$

$$t_H = \min(t_{H1}, t_{H2})$$

**TIMING CHARACTERISTICS<sup>(1)</sup>**

PARAMETER	TEST CONDITIONS	ADS5287			UNIT
		MIN	TYP	MAX	
t <sub>A</sub>	Aperture delay	1.5		4.5	ns
	Aperture delay variation	Channel-to-channel within the same device (3σ)			ps
t <sub>J</sub>	Aperture jitter		400		fs
t <sub>WAKE</sub>	Wake-up time	Time to valid data after coming out of COMPLETE POWER-DOWN mode			μs
		Time to valid data after coming out of PARTIAL POWER-DOWN mode (with clock continuing to run during power-down)			μs
		Time to valid data after stopping and restarting the input clock			μs
	Data latency		12		Clock cycles

(1) Timing parameters are ensured by design and characterization; not production tested.

## LVDS OUTPUT TIMING CHARACTERISTICS<sup>(1)</sup>

Typical values are at +25°C, minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = +85^{\circ}\text{C}$ , sampling frequency = as specified,  $C_{LOAD} = 5\text{pF}$ <sup>(2)</sup>,  $I_{OUT} = 3.5\text{mA}$ ,  $R_{LOAD} = 100\Omega$ <sup>(3)</sup>, and no internal termination, unless otherwise noted.

PARAMETER	TEST CONDITIONS <sup>(4)</sup>	ADS5287									UNIT	
		40MSPS			50MSPS			65MSPS				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{SU}$	Data setup time <sup>(5)</sup>	Data valid <sup>(6)</sup> to zero-crossing of LCLK <sub>P</sub>	0.67			0.47			0.27			ns
$t_H$	Data hold time <sup>(5)</sup>	Zero-crossing of LCLK <sub>P</sub> to data becoming invalid <sup>(6)</sup>	0.85			0.65			0.4			ns
$t_{PROP}$	Clock propagation delay	Input clock (ADCLK) rising edge cross-over to output clock (ADCLK <sub>P</sub> ) rising edge cross-over	10	14	16.6	10	12.5	14.1	9.7	11.5	14	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (LCLK <sub>P</sub> – LCLK <sub>N</sub> )	45.5	50	53	45	50	53.5	41	50	57	
	Bit clock cycle-to-cycle jitter			250			250			250		ps, pp
	Frame clock cycle-to-cycle jitter			150			150			150		ps, pp
$t_{RISE}$ , $t_{FALL}$	Data rise time, data fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns
$t_{CLKRISE}$ , $t_{CLKFALL}$	Output clock rise time, output clock fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns

- (1) Timing parameters are ensured by design and characterization; not production tested.
- (2)  $C_{LOAD}$  is the effective external single-ended load capacitance between each output pin and ground.
- (3)  $I_{OUT}$  refers to the LVDS buffer current setting;  $R_{LOAD}$  is the differential load resistance between the LVDS output pair.
- (4) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load.
- (5) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
- (6) Data valid refers to a logic high of +100mV and a logic low of –100mV.

## LVDS OUTPUT TIMING CHARACTERISTICS<sup>(1)</sup>

Typical values are at +25°C, minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = +85^{\circ}\text{C}$ , sampling frequency = as specified,  $C_{LOAD} = 5\text{pF}$ <sup>(2)</sup>,  $I_{OUT} = 3.5\text{mA}$ ,  $R_{LOAD} = 100\Omega$ <sup>(3)</sup>, and no internal termination, unless otherwise noted.

PARAMETER	TEST CONDITIONS <sup>(4)</sup>	ADS5287									UNIT	
		30MSPS			20MSPS			10MSPS				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{SU}$	Data setup time <sup>(5)</sup>	Data valid <sup>(6)</sup> to zero-crossing of LCLK <sub>P</sub>	0.8			1.5			3.7			ns
$t_H$	Data hold time <sup>(5)</sup>	Zero-crossing of LCLK <sub>P</sub> to data becoming invalid <sup>(6)</sup>	1.2			1.9			3.9			ns
$t_{PROP}$	Clock propagation delay	Input clock (ADCLK) rising edge cross-over to output clock (ADCLK <sub>P</sub> ) rising edge cross-over	9.5	13.5	17.3	9.5	14.5	17.3	10	14.7	17.1	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (LCLK <sub>P</sub> – LCLK <sub>N</sub> )	46.5	50	52	48	50	51	49	50	51	
	Bit clock cycle-to-cycle jitter			250			250			750		ps, pp
	Frame clock cycle-to-cycle jitter			150			150			500		ps, pp
$t_{RISE}$ , $t_{FALL}$	Data rise time, data fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns
$t_{CLKRISE}$ , $t_{CLKFALL}$	Output clock rise time, output clock fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns

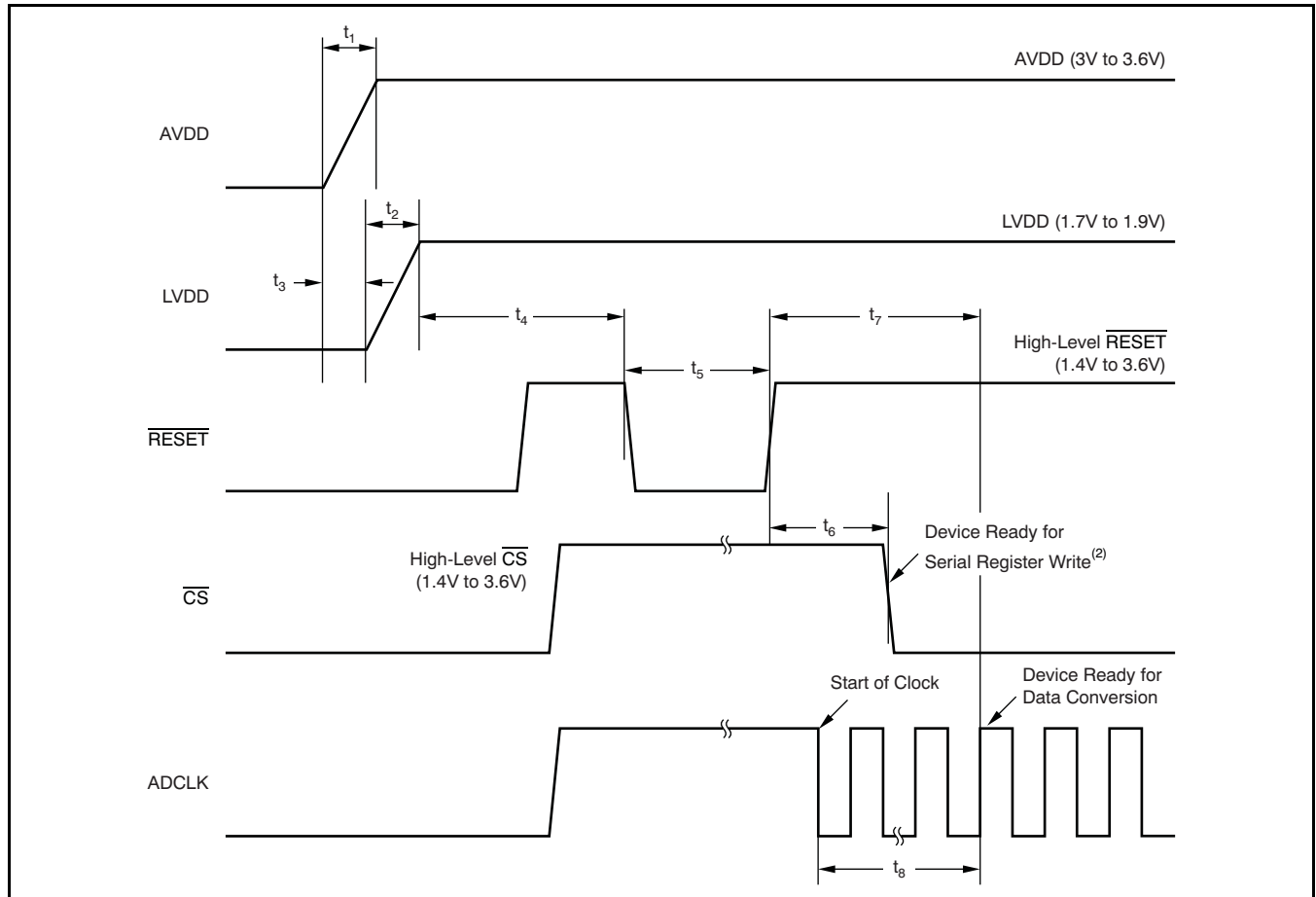
- (1) Timing parameters are ensured by design and characterization; not production tested.
- (2)  $C_{LOAD}$  is the effective external single-ended load capacitance between each output pin and ground.
- (3)  $I_{OUT}$  refers to the LVDS buffer current setting;  $R_{LOAD}$  is the differential load resistance between the LVDS output pair.
- (4) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load.
- (5) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
- (6) Data valid refers to a logic high of +100mV and a logic low of –100mV.

### LVDS OUTPUT TIMING CHARACTERISTICS

PARAMETER <sup>(1)</sup>	TEST CONDITIONS	TIMINGS WHEN USING REGISTER 0xE3 <sup>(2)</sup> At 40 MSPS		
		MIN	TYP	MAX
Data setup time	Data valid <sup>(3)</sup> to zero-crossing of LCLKP	0.60		
Data hold time	Zero-crossing of LCLKP to data becoming invalid <sup>(3)</sup>	0.92		
Clock propagation delay	Input clock (ADCLK) rising edge cross-over to output clock (ADCLK) rising edge crossover	8	12	14.6

- (1) Only the setup time, hold time and clock propagation delay parameters are affected. Rest of the parameters are same as given in previous two tables.
- (2) Only timing specifications for 40MSPS are affected when using register 0xE3 (as specified in the recommended operating table section). The timing specifications for other clock frequencies are same as given in previous two tables.
- (3) Data valid refers to logic high of +100mV and logic low of -100mV.

### RECOMMENDED POWER-UP SEQUENCING AND RESET TIMING

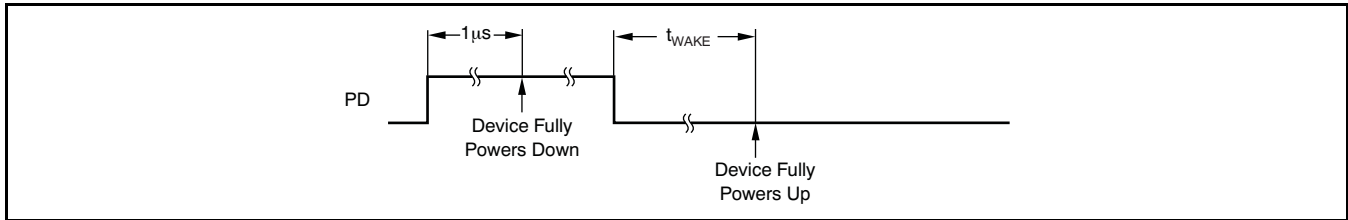


$10\mu\text{s} < t_1 < 50\text{ms}$ ,  $10\mu\text{s} < t_2 < 50\text{ms}$ ,  $-10\text{ms} < t_3 < 10\text{ms}$ ,  $t_4 > 10\text{ms}$ ,  $t_5 > 100\text{ns}$ ,  $t_6 > 100\text{ns}$ ,  $t_7 > 10\text{ms}$ , and  $t_8 > 100\mu\text{s}$ .

(1) The AVDD and LVDD power-on sequence does not matter as long as  $-10\text{ms} < t_3 < 10\text{ms}$ . Similar considerations apply while shutting down the device.

(2) Write initialization registers listed in the [Initialization Registers](#) table.

**POWER-DOWN TIMING**



Power-up time shown is based on 1 μF bypass capacitors on the reference pins. t<sub>WAKE</sub> is the time it takes for the device to wake up completely from power-down mode. The ADS5287 has two power-down modes: complete power-down mode and partial power-down mode. The device can be configured in partial power-down mode through a register setting.

t<sub>WAKE</sub> < 50 μs for complete power-down mode.

t<sub>WAKE</sub> < 2 μs for partial power-down mode (provided the clock is not shut off during power-down).

## SERIAL INTERFACE

The ADS5287 has a set of internal registers that can be accessed through the serial interface formed by pins  $\overline{CS}$  (chip select, active low), SCLK (serial interface clock), and SDATA (serial interface data). When  $\overline{CS}$  is low, the following actions occur:

- Serial shift of bits into the device is enabled
- SDATA (serial data) is latched at every rising edge of SCLK
- SDATA is loaded into the register at every 24th SCLK rising edge

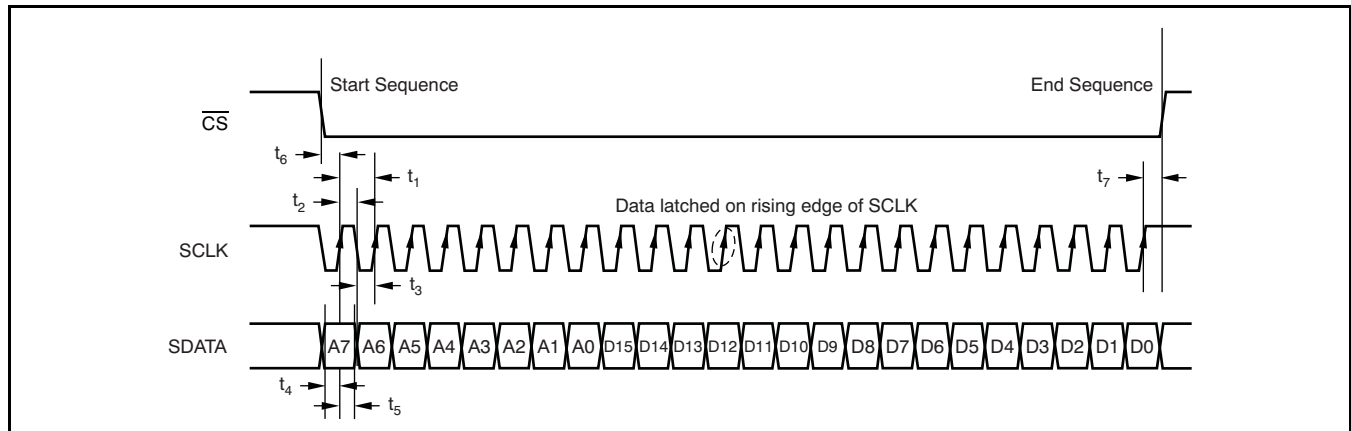
If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active  $\overline{CS}$  pulse. The first eight bits form the register address and the remaining 16 bits form the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (a few hertz) and also with a non-50% SCLK duty cycle.

### Register Initialization

After power-up, the internal registers **must** be initialized to the respective default values. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a low-going pulse on the  $\overline{RESET}$  pin; or
2. Through a software reset; using the serial interface, set the RST bit high. Setting this bit initializes the internal registers to the respective default values and then self-resets the RST bit low. In this case, the  $\overline{RESET}$  pin stays high (inactive).

### SERIAL INTERFACE TIMING



PARAMETER	DESCRIPTION	ADS5287			UNIT
		MIN	TYP	MAX	
$t_1$	SCLK period	50			ns
$t_2$	SCLK high time	20			ns
$t_3$	SCLK low time	20			ns
$t_4$	Data setup time	5			ns
$t_5$	Data hold time	5			ns
$t_6$	$\overline{CS}$ fall to SCLK rise	8			ns
$t_7$	Time between last SCLK rising edge to $\overline{CS}$ rising edge	8			ns

## SERIAL REGISTER MAP

**Table 3. SUMMARY OF FUNCTIONS SUPPORTED BY SERIAL INTERFACE<sup>(1) (2) (3) (4)</sup>**

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION	DEFAULT
00																X	RST	Self-clearing software RESET.	Inactive
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>	Channel-specific ADC power-down mode.	Inactive
								X									PDN_PARTIAL	Partial power-down mode (fast recovery from power-down).	Inactive
						X											PDN_COMPLETE	Register mode for complete power-down (slower recovery).	Inactive
11						X											PDN_PIN_CFG	Configures the PD pin for partial power-down mode.	Complete power-down
														X	X	X	ILVDS_LCLK<2:0>	LVDS current drive programmability for LCLK <sub>N</sub> and LCLK <sub>P</sub> pins.	3.5mA drive
										X	X	X					ILVDS_FRAME<2:0>	LVDS current drive programmability for ADCLK <sub>N</sub> and ADCLK <sub>P</sub> pins.	3.5mA drive
12						X	X	X									ILVDS_DAT<2:0>	LVDS current drive programmability for OUT <sub>N</sub> and OUT <sub>P</sub> pins.	3.5mA drive
		X															EN_LVDS_TERM	Enables internal termination for LVDS buffers.	Termination disabled
		1												X	X	X	TERM_LCLK<2:0>	Programmable termination for LCLK <sub>N</sub> and LCLK <sub>P</sub> buffers.	Termination disabled
		1							X	X	X						TERM_FRAME<2:0>	Programmable termination for ADCLK <sub>N</sub> and ADCLK <sub>P</sub> buffers.	Termination disabled
14						X	X	X									TERM_DAT<2:0>	Programmable termination for OUT <sub>N</sub> and OUT <sub>P</sub> buffers.	Termination disabled
									X	X	X	X	X	X	X	X	LFNS_CH<8:1>	Channel-specific, low-frequency noise suppression mode enable.	Inactive
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>	Swaps the polarity of the analog input pins electrically.	IN <sub>P</sub> is positive input
25										X	0	0					EN_RAMP	Enables a repeating full-scale ramp pattern on the outputs.	Inactive
										0	X	0					DUALCUSTOM_PAT	Enables the mode wherein the output toggles between two defined codes.	Inactive
										0	0	X					SINGLE_CUSTOM_PAT	Enables the mode wherein the output is a constant specified code.	Inactive
															X	X	BITS_CUSTOM1<9:8>	2MSBs for a single custom pattern (and for the first code of the dual custom pattern). <9> is the MSB.	Inactive
													X	X			BITS_CUSTOM2<9:8>	2MSBs for the second code of the dual custom pattern.	Inactive
26	X	X	X	X	X	X	X	X									BITS_CUSTOM1<7:0>	8 lower bits for the single custom pattern (and for the first code of the dual custom pattern). <0> is the LSB.	Inactive
27	X	X	X	X	X	X	X	X									BITS_CUSTOM2<7:0>	8 lower bits for the second code of the dual custom pattern.	Inactive
2A													X	X	X	X	GAIN_CH1<3:0>	Programmable gain channel 1.	0dB gain
									X	X	X	X					GAIN_CH2<3:0>	Programmable gain channel 2.	0dB gain
					X	X	X	X									GAIN_CH3<3:0>	Programmable gain channel 3.	0dB gain
	X	X	X	X													GAIN_CH4<3:0>	Programmable gain channel 4.	0dB gain
2B	X	X	X	X													GAIN_CH5<3:0>	Programmable gain channel 5.	0dB gain
					X	X	X	X									GAIN_CH6<3:0>	Programmable gain channel 6.	0dB gain
									X	X	X	X					GAIN_CH7<3:0>	Programmable gain channel 7.	0dB gain
													X	X	X	X	GAIN_CH8<3:0>	Programmable gain channel 8.	0dB gain

(1) The unused bits in each register (identified as blank table cells) must be programmed as '0'.

(2) X = Register bit referenced by the corresponding name and description (default is 0).

(3) Bits marked as '0' should be forced to 0, and bits marked as '1' should be forced to 1 when the particular register is programmed.

(4) Multiple functions in a register should be programmed in a single write operation.

**Table 3. SUMMARY OF FUNCTIONS SUPPORTED BY SERIAL INTERFACE<sup>(1) (2) (3) (4)</sup> (continued)**

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION	DEFAULT
42	1															X	DIFF_CLK	Differential clock mode.	Single-ended clock
	1													X			EN_DCC	Enables the duty-cycle correction circuit.	Disabled
	1												X				EXT_REF_VCM	Drives the external reference mode through the V <sub>CM</sub> pin.	External reference drives REF <sub>T</sub> and REF <sub>B</sub>
	1									X	X						PHASE_DDR<1:0>	Controls the phase of LCLK output relative to data.	90 degrees
45															0	X	PAT_DESKEW	Enables deskew pattern mode.	Inactive
															X	0	PAT_SYNC	Enables sync pattern mode.	Inactive
46	1						1							X			BTC_MODE	Binary two's complement format for ADC output.	Straight offset binary
	1						1						X				MSB_FIRST	Serialized ADC output comes out MSB-first.	LSB-first output
	1						1					X					EN_SDR	Enables SDR output mode (LCLK becomes a 12x input clock).	DDR output mode
	1		X				1					1					FALL_SDR	Controls whether the LCLK rising or falling edge comes in the middle of the data window when operating in SDR output mode.	Rising edge of LCLK in middle of data window

**SUMMARY OF FEATURES**

FEATURES	DEFAULT	SELECTION	POWER IMPACT (relative to default) AT f <sub>s</sub> = 65MSPS
<b>ANALOG FEATURES</b>			
Internal or external reference (driven on the REF <sub>T</sub> and REF <sub>B</sub> pins)	N/A	Pin	Internal reference mode takes approximately 23mW more power on AVDD
External reference driven on the V <sub>CM</sub> pin	Off	Register 42	Approximately 9mW less power on AVDD
Duty cycle correction circuit	Off	Register 42	Approximately 7mW more power on AVDD
Low-frequency noise suppression	Off	Register 14	With zero input to the ADC, low-frequency noise suppression causes digital switching at f <sub>s</sub> /2, thereby increasing LVDD power by approximately 7mW/channel
Single-ended or differential clock	Single-ended	Register 42	Differential clock mode takes approximately 7mW more power on AVDD
Power-down mode	Off	Pin and register 0F	Refer to the <i>Power-Down Modes</i> section in the <a href="#">Electrical Characteristics</a> table
<b>DIGITAL FEATURES</b>			
Programmable digital gain (0dB to 12dB)	0dB	Registers 2A and 2B	No difference
Straight offset or BTC output	Straight offset	Register 46	No difference
Swap polarity of analog input pins	Off	Register 24	No difference
<b>LVDS OUTPUT PHYSICAL LAYER</b>			
LVDS internal termination	Off	Register 12	Approximately 7mW more power on AVDD
LVDS current programmability	3.5mA	Register 11	As per LVDS clock and data buffer current setting
<b>LVDS OUTPUT TIMING</b>			
LSB- or MSB-first output	LSB-first	Register 46	No difference
DDR or SDR output	DDR	Register 46	SDR mode takes approximately 2mW more power on LVDD (at f <sub>s</sub> = 30MSPS)
LCLK phase relative to data output	Refer to <a href="#">Figure 1</a>	Register 42	No difference



## DESCRIPTION OF SERIAL REGISTERS

### SOFTWARE RESET

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
00																X	RST

Software reset is applied when the RST bit is set to '1'; setting this bit resets all internal registers and self-clears to '0'.

### POWER-DOWN MODES

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>
								X									PDN_PARTIAL
						0	X										PDN_COMPLETE
						X	0										PDN_PIN_CFG

Each of the eight channels can be individually powered down. PDN\_CH<N> controls the power-down mode for the ADC channel <N>.

In addition to channel-specific power-down, the ADS5287 also has two global power-down modes—partial power-down mode and complete power-down mode. Partial power-down mode partially powers down the chip; recovery from this mode is much quicker, provided that the clock has been running for at least 50µs before exiting this mode. Complete power-down mode, on the other hand, completely powers down the chip, and involves a much longer recovery time.

In addition to programming the device for either of these two power-down modes (through either the PDN\_PARTIAL or PDN\_COMPLETE bits, respectively), the PD pin itself can be configured as either a partial power-down pin or a complete power-down pin control. For example, if PDN\_PIN\_CFG = 0 (default), when the PD pin is high, the device enters complete power-down mode. However, if PDN\_PIN\_CFG = 1, when the PD pin is high, the device enters partial power-down mode.

### LVDS DRIVE PROGRAMMABILITY

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
11														X	X	X	ILVDS_LCLK<2:0>
										X	X	X					ILVDS_FRAME<2:0>
						X	X	X									ILVDS_DAT<2:0>

The LVDS drive strength of the bit clock (LCLK<sub>P</sub> or LCLK<sub>N</sub>) and the frame clock (ADCLK<sub>P</sub> or ADCLK<sub>N</sub>) can be individually programmed. The LVDS drive strengths of all the data outputs OUT<sub>P</sub> and OUT<sub>N</sub> can also be programmed to the same value.

All three drive strengths (bit clock, frame clock, and data) are programmed using sets of three bits. Table 4 shows an example of how the drive strength of the bit clock is programmed (the method is similar for the frame clock and data drive strengths).

**Table 4. Bit Clock Drive Strength<sup>(1)</sup>**

ILVDS_LCLK<2>	ILVDS_LCLK<1>	ILVDS_LCLK<0>	LVDS DRIVE STRENGTH FOR LCLK <sub>P</sub> AND LCLK <sub>N</sub>
0	0	0	3.5mA (default)
0	0	1	2.5mA
0	1	0	1.5mA
0	1	1	0.5mA
1	0	0	7.5mA
1	0	1	6.5mA
1	1	0	5.5mA
1	1	1	4.5mA

(1) Current settings lower than 1.5mA are not recommended.

**LVDS INTERNAL TERMINATION PROGRAMMABILITY**

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
12		X															EN_LVDS_TERM
		1												X	X	X	TERM_LCLK<2:0>
		1								X	X	X					TERM_FRAME<2:0>
		1					X	X	X								TERM_DAT<2:0>

The LVDS buffers have high-impedance current sources driving the outputs. When driving traces whose characteristic impedance is not perfectly matched with the termination impedance on the receiver side, there may be reflections back to the LVDS output pins of the ADS5287 that cause degraded signal integrity. By enabling an internal termination (between the positive and negative outputs) for the LVDS buffers, the signal integrity can be significantly improved in such scenarios. To set the internal termination mode, the EN\_LVDS\_TERM bit should be set to '1'. Once this bit is set, the internal termination values for the bit clock, frame clock, and data buffers can be independently programmed using sets of three bits. Table 5 shows an example of how the internal termination of the LVDS buffer driving the bit clock is programmed (the method is similar for the frame clock and data buffers). These termination values are only typical values and can vary by up to ±20% across temperature and from device to device.

**Table 5. Bit Clock Drive Strengths**

TERM_LCLK<2>	TERM_LCLK<1>	TERM_LCLK<0>	INTERNAL TERMINATION BETWEEN LCLK <sub>P</sub> AND LCLK <sub>N</sub> IN Ω
0	0	0	None
0	0	1	260
0	1	0	150
0	1	1	94
1	0	0	125
1	0	1	80
1	1	0	66
1	1	1	55

## LOW-FREQUENCY NOISE SUPPRESSION MODE

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>

The low-frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around dc). Setting this mode shifts the low-frequency noise of the ADS5287 to approximately  $f_s/2$ , thereby moving the noise floor around dc to a much lower value. LFNS\_CH<8:1> enables this mode individually for each channel.

## ANALOG INPUT INVERT

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>

Normally, the  $IN_P$  pin represents the positive analog input pin, and  $IN_N$  represents the complementary negative input. Setting the bits marked INVERT\_CH<8:1> (individual control for each channel) causes the inputs to be swapped.  $IN_N$  now represents the positive input, and  $IN_P$  the negative input.

## LVDS TEST PATTERNS

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
25										X	0	0					EN_RAMP
										0	X	0					DUALCUSTOM_PAT
										0	0	X					SINGLE_CUSTOM_PAT
															X	X	BITS_CUSTOM1<9:8>
													X	X			BITS_CUSTOM2<9:8>
26	X	X	X	X	X	X	X	X									BITS_CUSTOM1<7:0>
27	X	X	X	X	X	X	X	X									BITS_CUSTOM2<7:0>
45															0	X	PAT_DESKEW
															X	0	PAT_SYNC

The ADS5287 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. Setting EN\_RAMP to '1' causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.

The device can also be programmed to output a constant code by setting SINGLE\_CUSTOM\_PAT to '1', and programming the desired code in BITS\_CUSTOM1<9:0>. In this mode, BITS\_CUSTOM1<9:0> take the place of the 10-bit ADC data at the output, and are controlled by LSB-first and MSB-first modes in the same way as normal ADC data are.

The device may also be made to toggle between two consecutive codes by programming DUAL\_CUSTOM\_PAT to '1'. The two codes are represented by the contents of BITS\_CUSTOM1<9:0> and BITS\_CUSTOM2<9:0>.

In addition to custom patterns, the device may also be made to output two preset patterns:

- Deskew patten:** Set using PAT\_DESKEW, this mode causes the 12 serial bits to come out as 0101010101 (the rightmost bit representing the first bit in the LSB-first mode)
- Sync pattern:** Set using PAT\_SYNC, this mode causes the 12 serial bits to come out as 111111000000 (the rightmost bit representing the first bit in the LSB-first mode)

Note that only one of the above patterns should be active at any given instant.

**PROGRAMMABLE GAIN**

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2A									X	X	X	X	X	X	X	X	GAIN_CH1<3:0>
									X	X	X	X					GAIN_CH2<3:0>
					X	X	X	X									GAIN_CH3<3:0>
	X	X	X	X													GAIN_CH4<3:0>
2B	X	X	X	X													GAIN_CH5<3:0>
					X	X	X	X									GAIN_CH6<3:0>
									X	X	X	X					GAIN_CH7<3:0>
													X	X	X	X	GAIN_CH8<3:0>

In applications where the full-scale swing of the analog input signal is much less than the 2V<sub>PP</sub> range supported by the ADS5287, a programmable gain can be set to achieve the full-scale output code even with a lower analog input swing. The programmable gain not only fills the output code range of the ADC, but also enhances the SNR of the device by utilizing quantization information from some extra internal bits. The programmable gain for each channel can be individually set using a set of four bits, indicated as GAIN\_CHN<3:0> for Channel N. The gain setting is coded in binary from 0dB to 12dB, as shown in [Table 6](#).

**Table 6. Gain Setting for Channel 1**

GAIN_CH1<3>	GAIN_CH1<2>	GAIN_CH1<1>	GAIN_CH1<0>	CHANNEL 1 GAIN SETTING
0	0	0	0	0dB
0	0	0	1	1dB
0	0	1	0	2dB
0	0	1	1	3dB
0	1	0	0	4dB
0	1	0	1	5dB
0	1	1	0	6dB
0	1	1	1	7dB
1	0	0	0	8dB
1	0	0	1	9dB
1	0	1	0	10dB
1	0	1	1	11dB
1	1	0	0	12dB
1	1	0	1	Do not use
1	1	1	0	Do not use
1	1	1	1	Do not use

## CLOCK, REFERENCE, AND DATA OUTPUT MODES

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
42	1															X	DIFF_CLK
	1													X			EN_DCC
	1												X				EXT_REF_VCM
	1									X	X						PHASE_DDR<1:0>
46	1						1							X			BTC_MODE
	1						1						X				MSB_FIRST
	1						1					X					EN_SDR
	1		X				1					1					FALL_SDR

### INPUT CLOCK

The ADS5287 is configured by default to operate with a single-ended input clock—CLK<sub>P</sub> is driven by a CMOS clock and CLK<sub>N</sub> is tied to '0'. However, by programming DIFF\_CLK to '1', the device can be made to work with a differential input clock on CLK<sub>P</sub> and CLK<sub>N</sub>. Operating with a low-jitter differential clock usually gives better SNR performance, especially at input frequencies greater than 30MHz.

In cases where the duty cycle of the input clock falls outside the 45% to 55% range, it is recommended to enable an internal duty cycle correction circuit. This enabling is done by setting the EN\_DCC bit to '1'.

### EXTERNAL REFERENCE

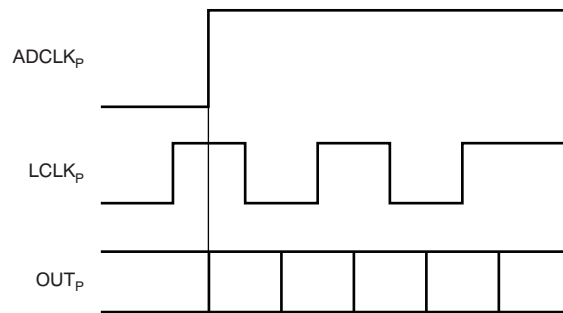
The ADS5287 can be made to operate in external reference mode by pulling the INT/ $\overline{\text{EXT}}$  pin to '0'. In this mode, the REF<sub>T</sub> and REF<sub>B</sub> pins should be driven with voltage levels of 2.5V and 0.5V, respectively, and must have enough drive strength to drive the switched capacitance loading of the reference voltages by each ADC. The advantage of using the external reference mode is that multiple ADS5287 units can be made to operate with the same external reference, thereby improving parameters such as gain matching across devices. However, in applications that do not have an available high drive, differential external reference, the ADS5287 can still be driven with a single external reference voltage on the V<sub>CM</sub> pin. When EXT\_REF\_VCM is set as '1' (and the INT/ $\overline{\text{EXT}}$  pin is set to '0'), the V<sub>CM</sub> pin is configured as an input pin, and the voltages on REF<sub>T</sub> and REF<sub>B</sub> are generated as shown in [Equation 1](#) and [Equation 2](#).

$$V_{\text{REF}_T} = 1.5V + \frac{V_{\text{CM}}}{1.5V} \quad (1)$$

$$V_{\text{REF}_B} = 1.5V - \frac{V_{\text{CM}}}{1.5V} \quad (2)$$

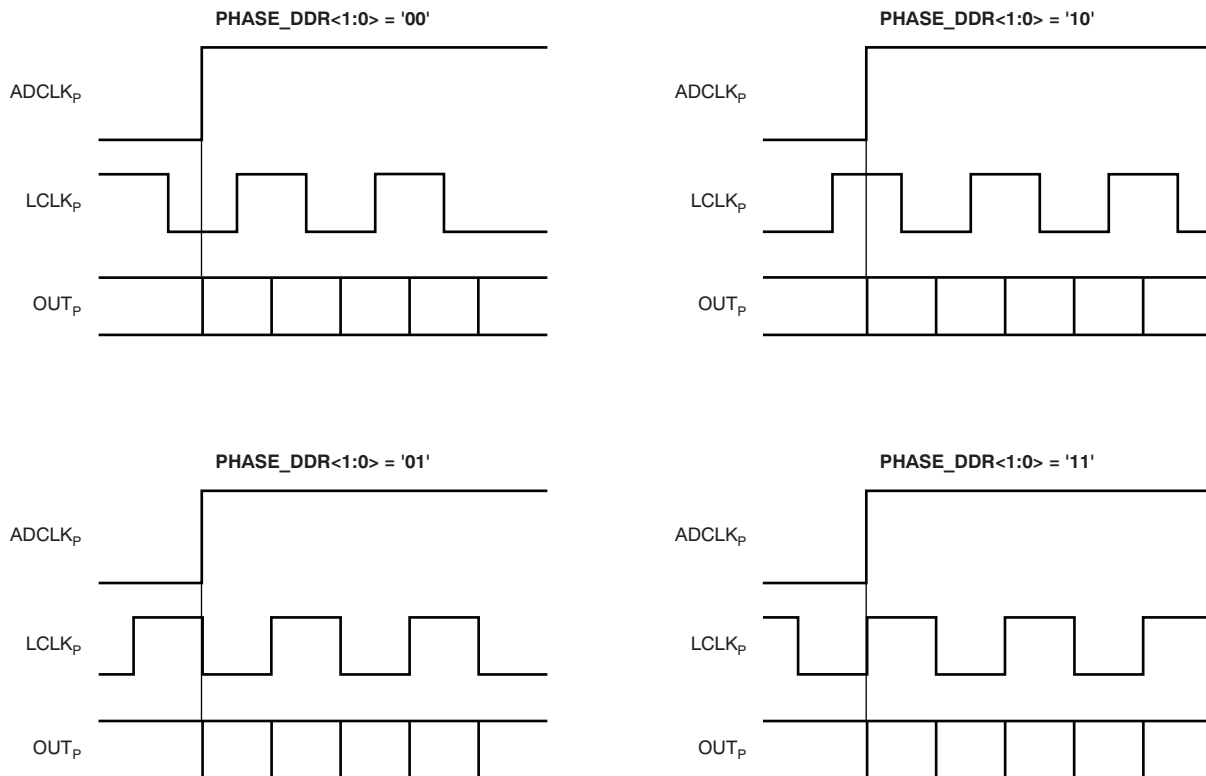
### BIT CLOCK PROGRAMMABILITY

The output interface of the ADS5287 is normally a DDR interface, with the LCLK rising edge and falling edge transitions in the middle of alternate data windows. [Figure 1](#) shows this default phase.



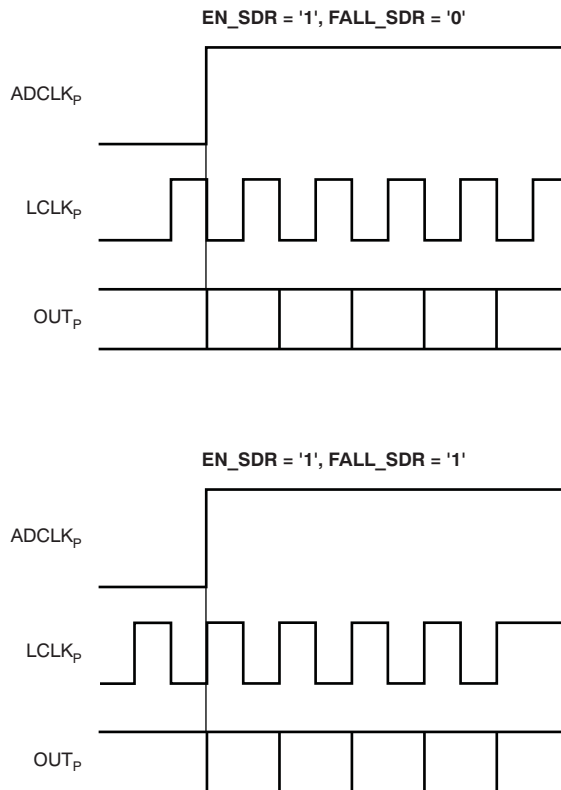
**Figure 1. Default Phase of LCLK**

The phase of LCLK can be programmed relative to the output frame clock and data using bits PHASE\_DDR<1:0>. The LCLK phase modes are shown in [Figure 2](#).



**Figure 2. Phase Programmability Modes for LCLK**

In addition to programming the phase of LCLK in the DDR mode, the device can also be made to operate in SDR mode by setting the EN\_SDR bit to '1'. In this mode, the bit clock (LCLK) is output at 12x times the input clock, or twice the rate as in DDR mode. Depending on the state of FALL\_SDR, LCLK may be output in either of the two manners shown in Figure 3. As shown in Figure 3, only the LCLK rising (or falling) edge is used to capture the output data in SDR mode.



**Figure 3. SDR Interface Modes**

The SDR mode does not work well beyond 40MSPS because the LCLK frequency becomes very high.

**DATA OUTPUT FORMAT MODES**

The ADC output, by default, is in straight offset binary mode. Programming the BTC\_MODE bit to '1' inverts the MSB, and the output becomes binary two's complement mode.

Also by default, the first two bits of the frame (following the rising edge of ADCLK<sub>p</sub>) are zeroes, followed by the LSB of the ADC output. Programming the MSB\_FIRST mode inverts the bit order in the word. Thus, in the MSB\_FIRST mode, the MSB is output as the first bit following the ADCLK<sub>p</sub> rising edge. The two zeroes come after the LSB at the end of the word.

### TYPICAL CHARACTERISTICS

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}C$  to  $T_{MAX} = +85^{\circ}C$ ,  $AVDD = 3.3V$ ,  $LVDD = 1.8V$ , clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode,  $I_{SET}$  resistor = 56.2k $\Omega$ , and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

**SPECTRAL PERFORMANCE**  
( $f_S = 40MHz, f_{IN} = 10MHz$ )

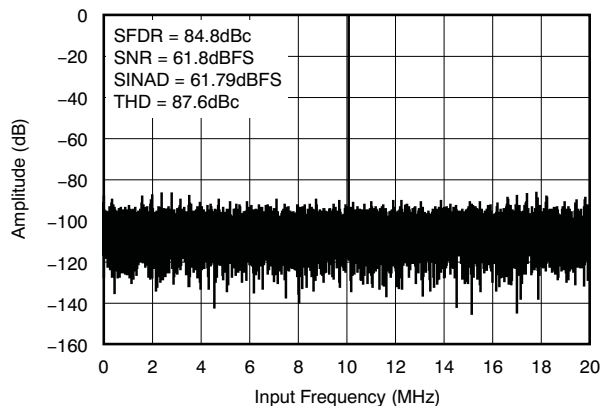


Figure 4.

**SPECTRAL PERFORMANCE**  
( $f_S = 40MHz, f_{IN} = 25MHz$ )

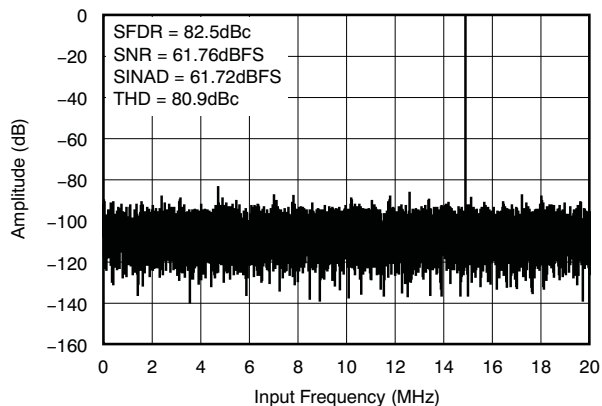


Figure 5.

**SPECTRAL PERFORMANCE**  
( $f_S = 50MHz, f_{IN} = 10MHz$ )

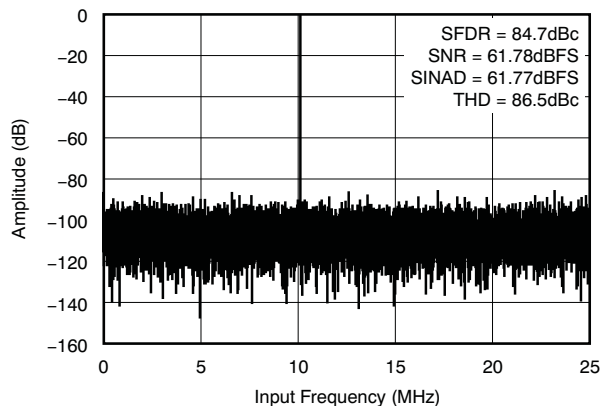


Figure 6.

**SPECTRAL PERFORMANCE**  
( $f_S = 50MHz, f_{IN} = 25MHz$ )

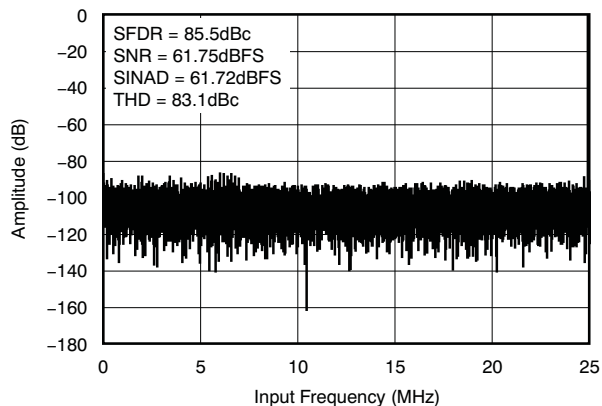


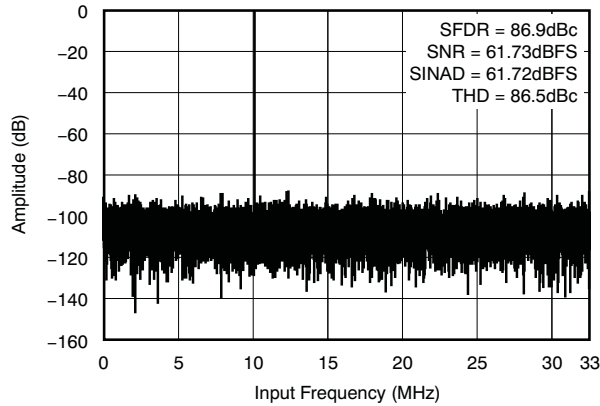
Figure 7.



**TYPICAL CHARACTERISTICS (continued)**

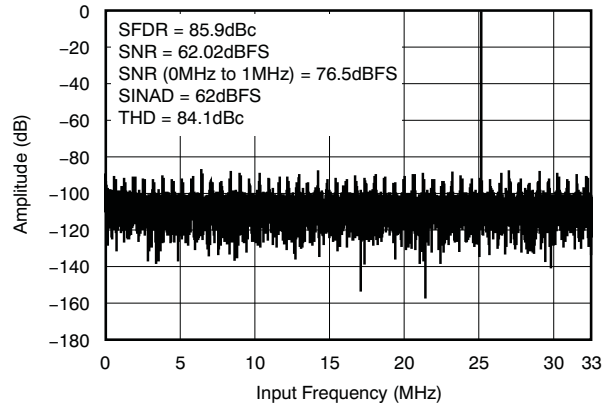
Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}C$  to  $T_{MAX} = +85^{\circ}C$ , AVDD = 3.3V, LVDD = 1.8V, clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode, I<sub>SET</sub> resistor = 56.2kΩ, and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

**SPECTRAL PERFORMANCE**  
( $f_S = 65MHz$ ,  $f_{IN} = 10MHz$ )



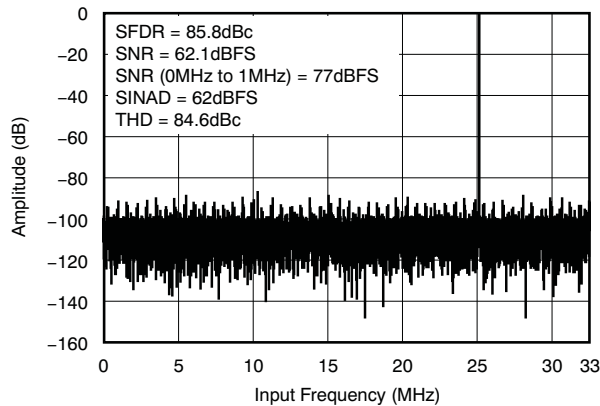
**Figure 8.**

**SPECTRAL PERFORMANCE**  
( $f_S = 65MHz$ ,  $f_{IN} = 25MHz$ )



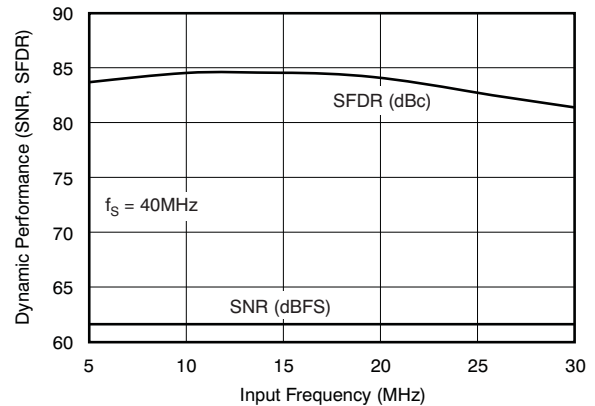
**Figure 9.**

**SPECTRAL PERFORMANCE, LOW-FREQUENCY NOISE SUPPRESSION MODE ENABLED**  
( $f_S = 65MHz$ ,  $f_{IN} = 25MHz$ )



**Figure 10.**

**DYNAMIC PERFORMANCE vs INPUT FREQUENCY**



**Figure 11.**

### TYPICAL CHARACTERISTICS (continued)

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}C$  to  $T_{MAX} = +85^{\circ}C$ , AVDD = 3.3V, LVDD = 1.8V, clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode,  $I_{SET}$  resistor = 56.2k $\Omega$ , and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

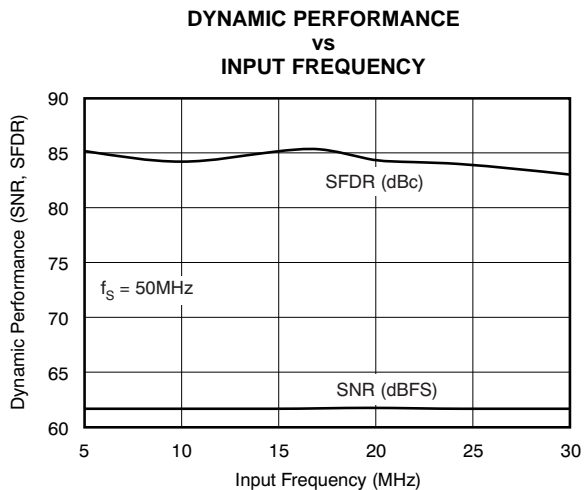


Figure 12.

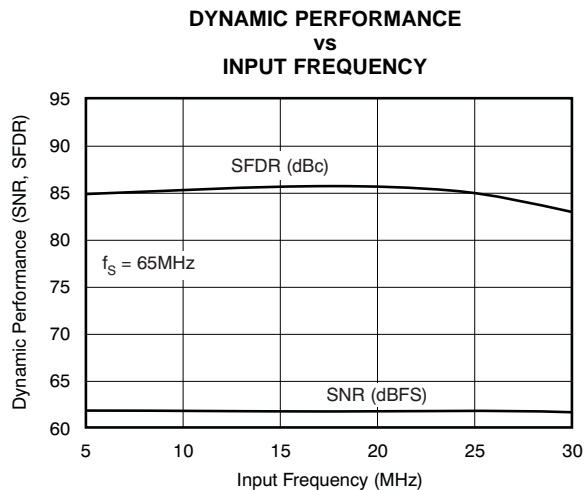


Figure 13.

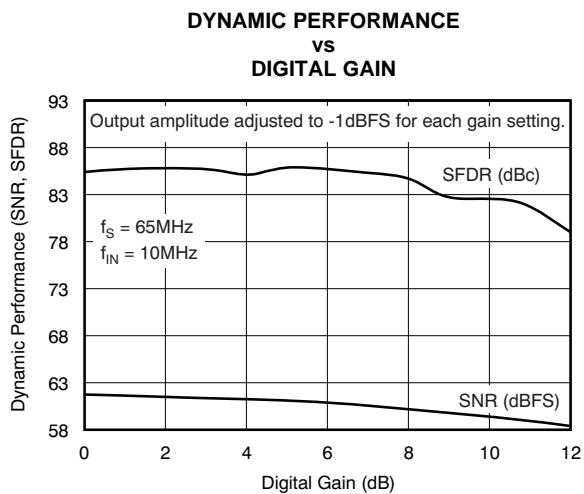


Figure 14.

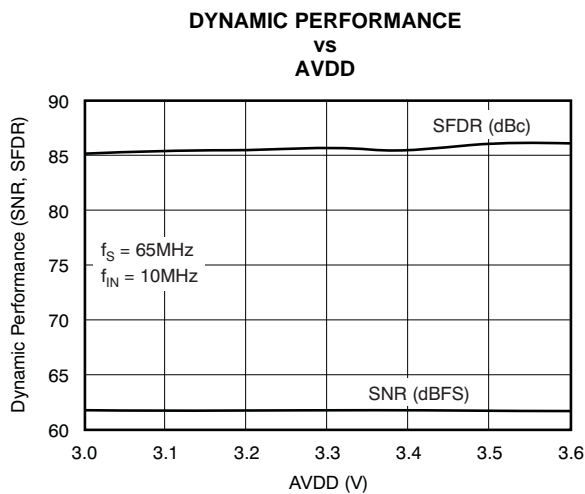


Figure 15.

**TYPICAL CHARACTERISTICS (continued)**

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}C$  to  $T_{MAX} = +85^{\circ}C$ , AVDD = 3.3V, LVDD = 1.8V, clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode,  $I_{SET}$  resistor = 56.2k $\Omega$ , and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

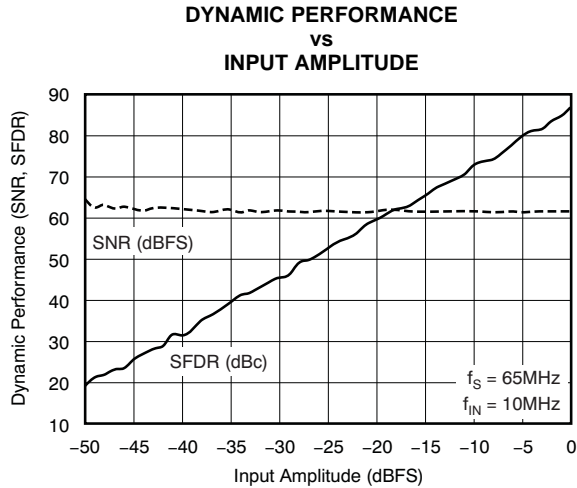


Figure 16.

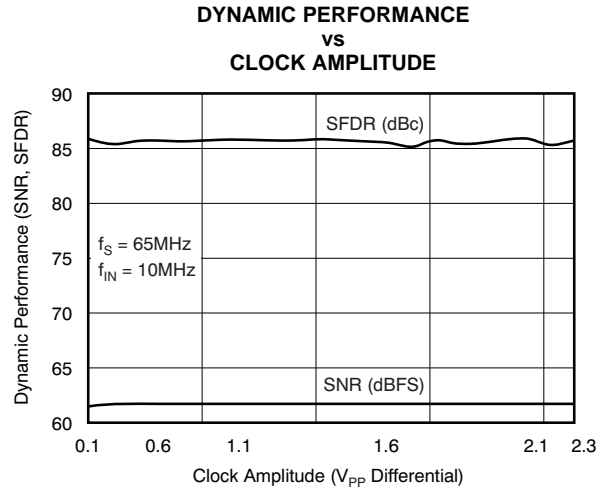


Figure 17.

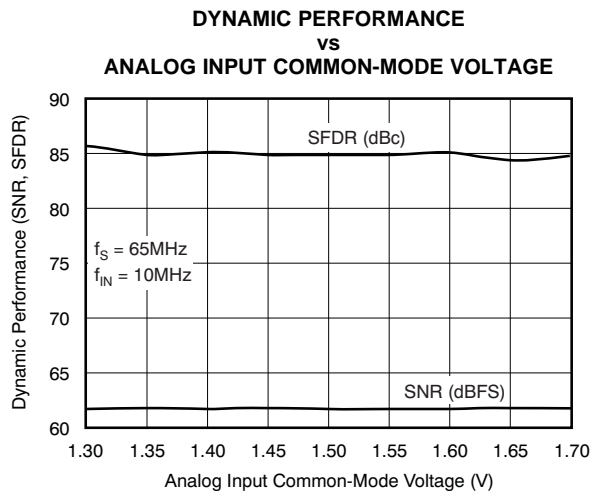


Figure 18.

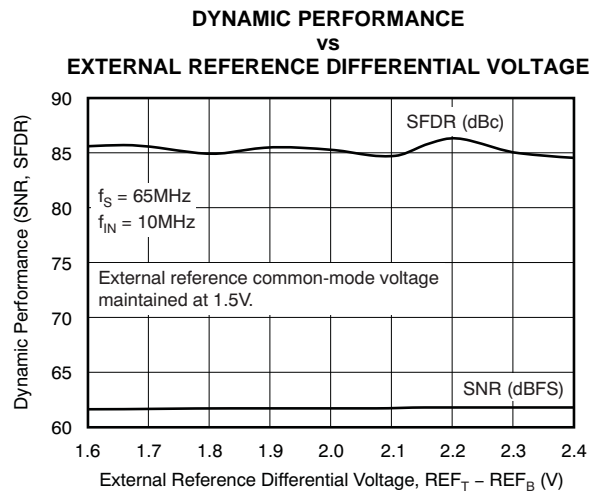


Figure 19.

### TYPICAL CHARACTERISTICS (continued)

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}C$  to  $T_{MAX} = +85^{\circ}C$ ,  $AVDD = 3.3V$ ,  $LVDD = 1.8V$ , clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode,  $I_{SET}$  resistor = 56.2k $\Omega$ , and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

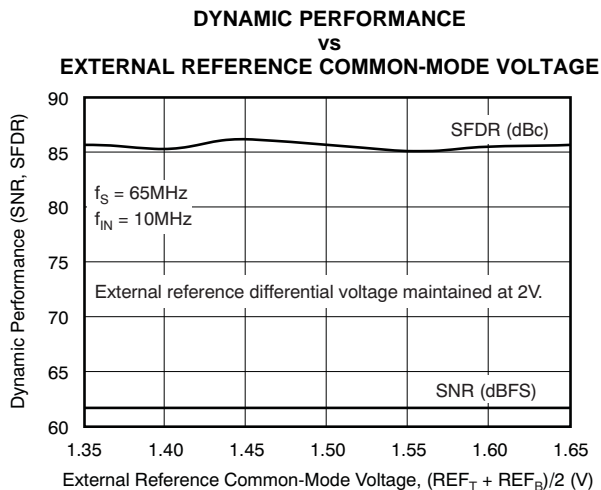


Figure 20.

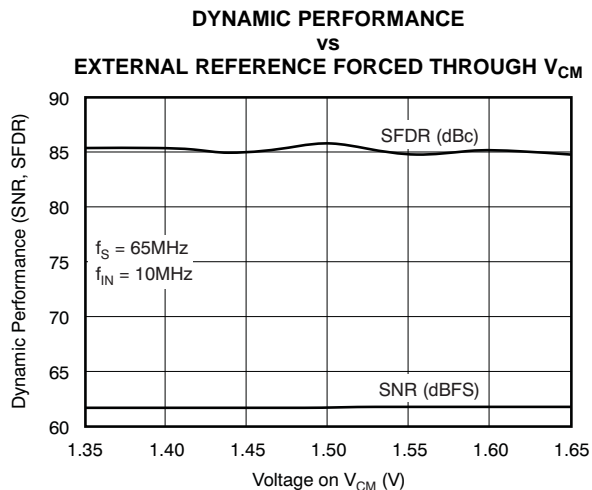


Figure 21.

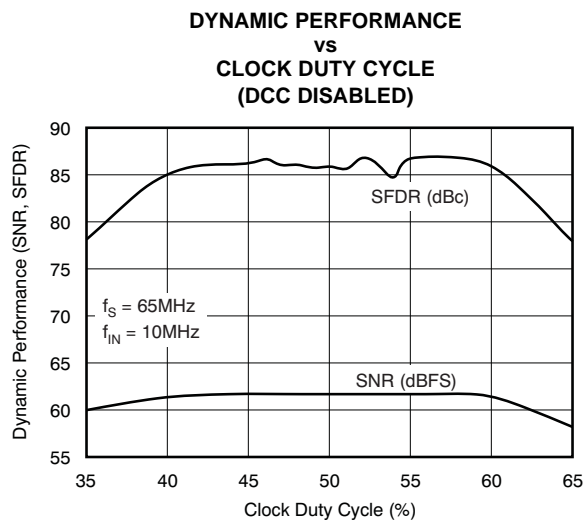


Figure 22.

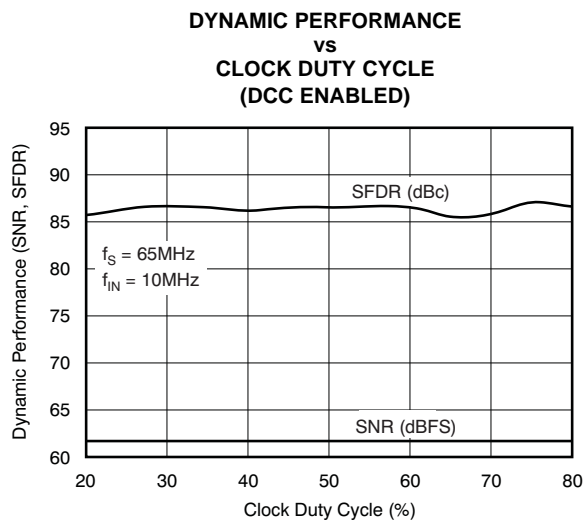


Figure 23.

**TYPICAL CHARACTERISTICS (continued)**

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}C$  to  $T_{MAX} = +85^{\circ}C$ ,  $AVDD = 3.3V$ ,  $LVDD = 1.8V$ , clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode,  $I_{SET}$  resistor = 56.2k $\Omega$ , and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

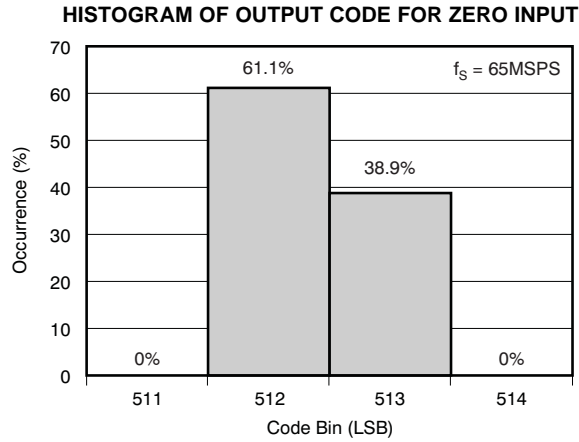


Figure 24.

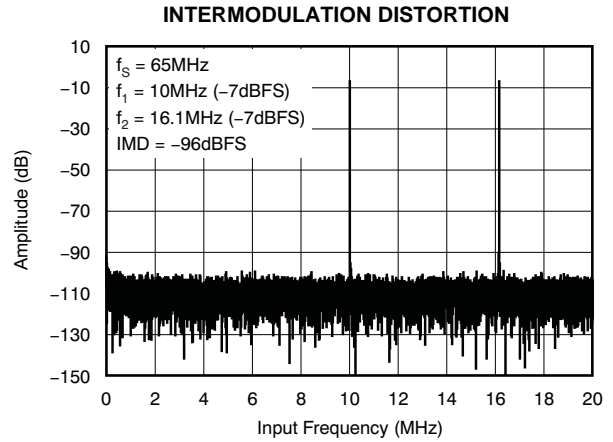


Figure 25.

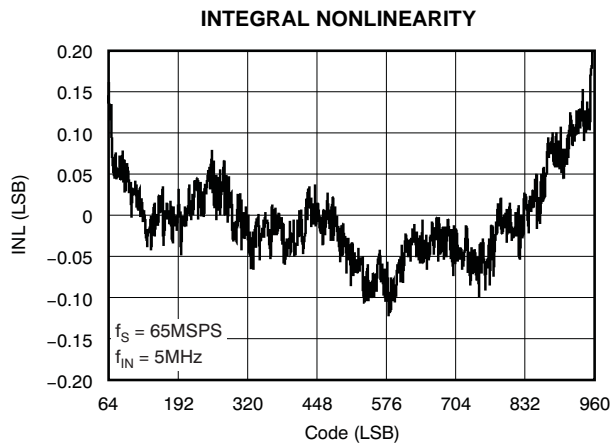


Figure 26.

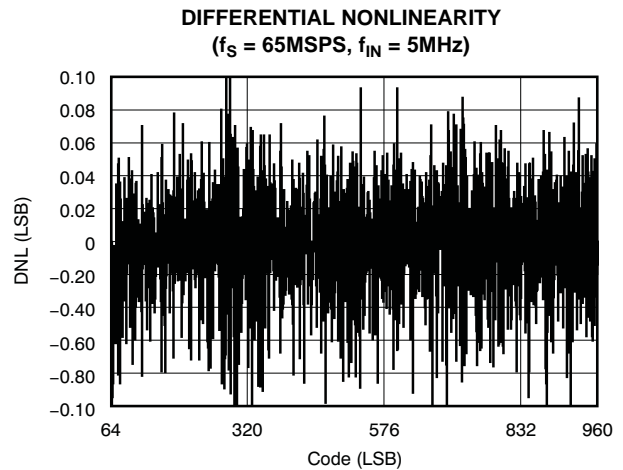
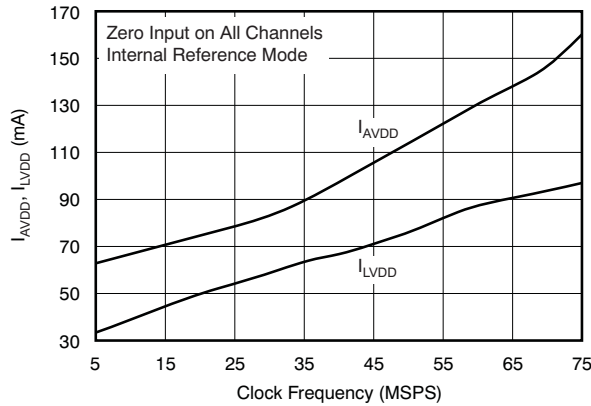


Figure 27.

**TYPICAL CHARACTERISTICS (continued)**

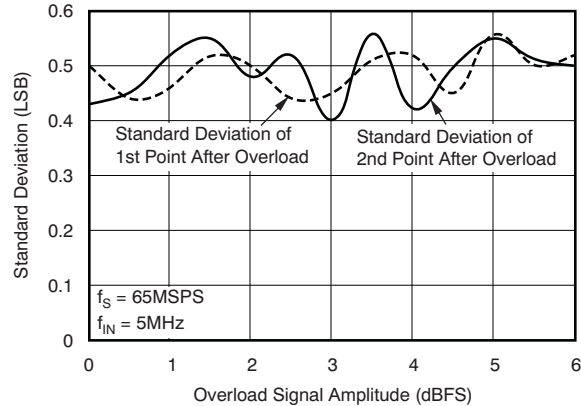
Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of  $T_{MIN} = -40^{\circ}C$  to  $T_{MAX} = +85^{\circ}C$ ,  $AVDD = 3.3V$ ,  $LVDD = 1.8V$ , clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, -1dBFS differential analog input, internal reference mode,  $I_{SET}$  resistor = 56.2k $\Omega$ , and LVDS buffer current setting = 3.5mA, unless otherwise noted. Typical values at +25°C.

**AVDD AND LVDD POWER-SUPPLY CURRENTS vs CLOCK FREQUENCY**

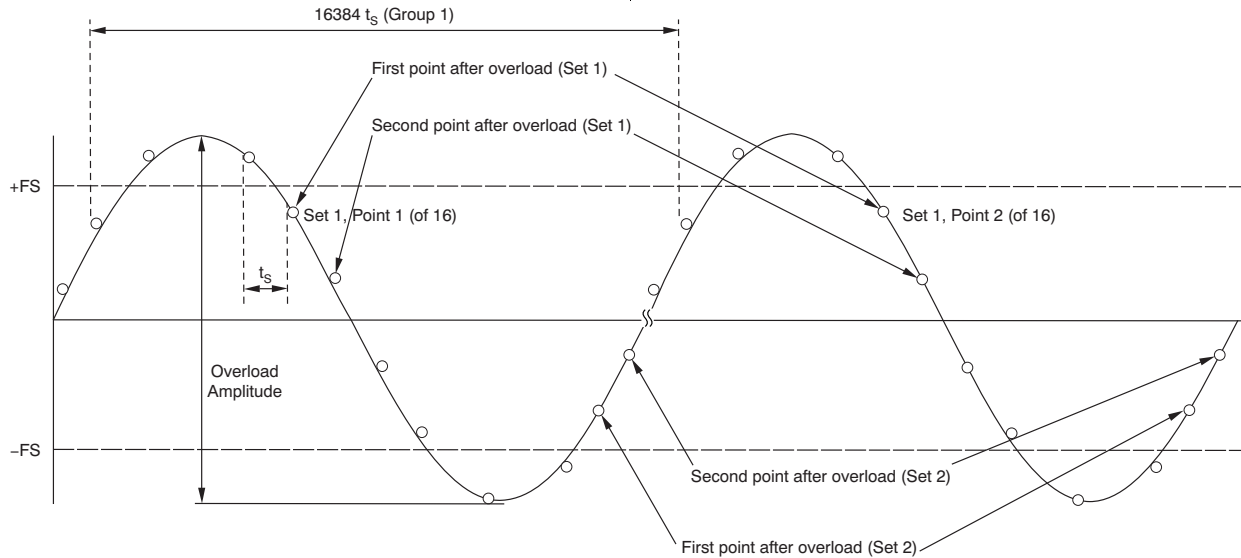


**Figure 28.**

**OVERLOAD RECOVERY AT 65MSPS**



**Figure 29.**



**NOTES:**

- Input sine wave phase is repetitive over 16384 clock cycles.
- 16 such repetitive groups (of 16384 clock cycles) are captured—a total of 262,144 points.
- Standard deviation of every set of *first and second points after overload* are analyzed over the 16 groups.
- Worst case of all such standard deviations are plotted in the graphs.

**Figure 30. Overload Recovery**

## APPLICATION INFORMATION

### THEORY OF OPERATION

The ADS5287 is an 8-channel, high-speed, CMOS ADC. Two zeroes are appended on the LSB side to the 10 bits given out by each channel. The resulting 12 bits are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the ADS5287 operate from a single clock (ADCLK). The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 12x clock required for the serializer is generated internally from ADCLK using a phase-locked loop (PLL). A 6x and a 1x clock are also output in LVDS format, along with the data, to enable easy data capture. The ADS5287 operates from internally-generated reference voltages that are trimmed to achieve a high level of accuracy. Trimmed references improve the gain matching across devices, and provide the option to operate the devices without having to externally drive and route reference lines. The nominal values of  $REF_T$  and  $REF_B$  are 2.5V and 0.5V, respectively. The references are internally scaled down differentially by a factor of 2. This scaling results in a differential input of  $-1V$  to correspond to the zero code of the ADC, and a differential input of  $+1V$  to correspond to the full-scale code (1023 LSB).  $V_{CM}$  (the common-mode voltage of  $REF_T$  and  $REF_B$ ) is also made available externally through a pin, and is nominally 1.5V.

The ADC employs a pipelined converter architecture that consists of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 10-bit level.

The ADC output goes to a serializer that operates from a 12x clock generated by the PLL. The 12 data bits from each channel are serialized and sent LSB first. In addition to serializing the data, the serializer also generates a 1x clock and a 6x clock. These clocks are generated in the same way the serialized data are generated, so these clocks maintain perfect synchronization with the data. The data and clock outputs of the serializer are buffered externally using LVDS buffers. Using LVDS buffers to transmit data externally has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the ADS5287.

The ADS5287 operates from two sets of supplies and grounds. The analog supply and ground set is identified as AVDD and AVSS, while the digital set is identified by LVDD and LVSS.

### ANALOG INPUT

The analog input consists of a switched-capacitor based, differential sample-and-hold architecture. This differential topology results in very good ac performance, even for high input frequencies at high sampling rates. The  $IN_N$  and  $IN_P$  pins must be externally biased around a common-mode voltage of 1.5V, available on  $V_{CM}$ . For a full-scale differential input, each input pin ( $IN_N$  and  $IN_P$ ) must swing symmetrically between  $V_{CM} + 0.5V$  and  $V_{CM} - 0.5V$ , resulting in a  $2V_{PP}$  differential input swing. The maximum input peak-to-peak differential swing is determined to be the difference between the internal reference voltages  $REF_T$  (2.5V nominal) and  $REF_B$  (0.5V nominal). [Figure 31](#) illustrates the model of the input driving circuit.

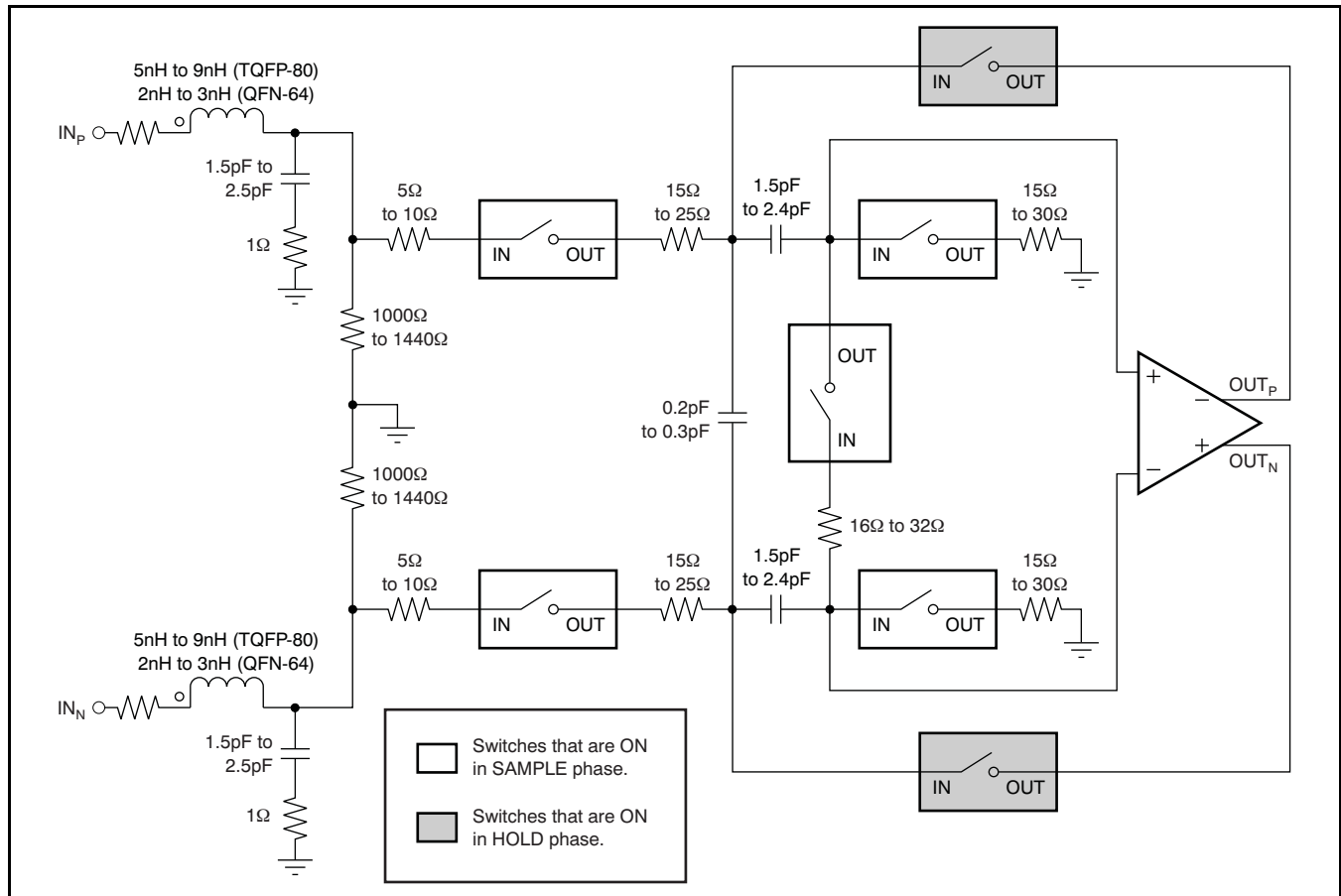


Figure 31. Analog Input Circuit Model

**Input Common-Mode Current**

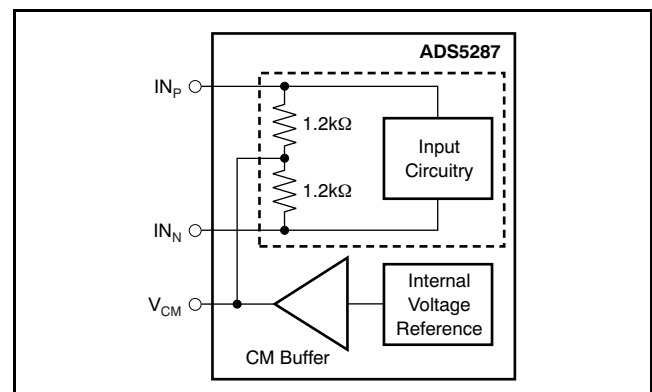
The input stage of all eight ADCs together sinks a common-mode current on the order of 2mA at 50MSPS. Equation 3 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{(2\text{mA}) \times f_s}{50\text{MSPS}} \tag{3}$$

If the driving stage is dc-coupled to the inputs, then Equation 3 can be used to determine its common-mode drive capability and impedance. The inputs can also be ac-coupled to the IN<sub>N</sub> and IN<sub>P</sub> pins. In that case, the input common-mode is set by two internal 1.2kΩ resistors connecting the input pins to V<sub>CM</sub>. This architecture is shown in Figure 32.

When the inputs are ac-coupled, there is a drop in the voltages at IN<sub>P</sub> and IN<sub>N</sub> relative to V<sub>CM</sub>. This can be computed from Equation 3. At 50MSPS, for example, the drop at each of the 16 input pins is 150mV, which is not optimal for ADC operation. Initialization Registers 1 and 5, described in the Initialization Register table, can be used to partially reduce the effect of this input common-mode drop

during ac-coupling by increasing V<sub>CM</sub> by roughly 75mV. When operating above 50MSPS, it is recommended that additional parallel resistors be added externally to restore the input common-mode to at least 1.4V, if the inputs are to be ac-coupled.



Dashed area denotes one of eight channels.

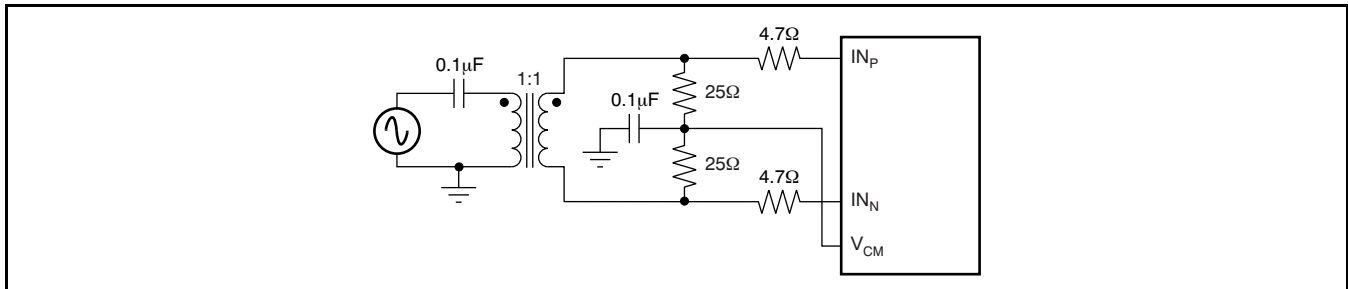
Figure 32. Common-Mode Biasing of Input Pins



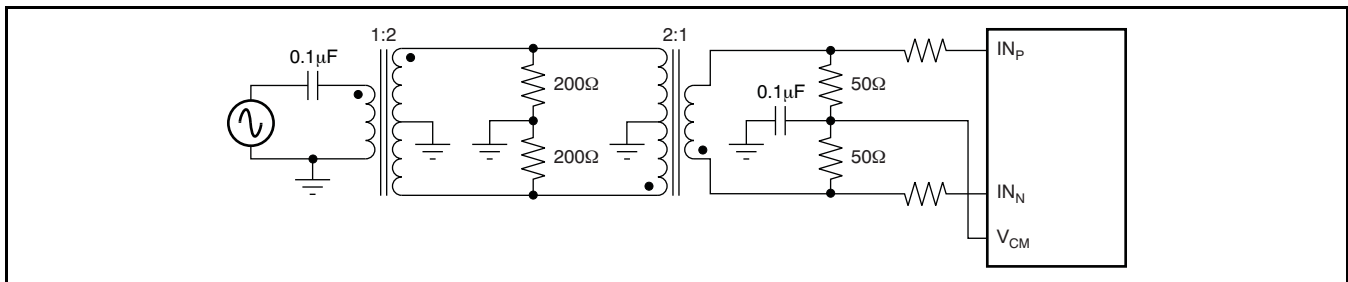
**Driving Circuit**

For optimum performance, the analog inputs must be driven differentially. This approach improves the common-mode noise immunity and even-order harmonic rejection. Input configurations using RF transformers suitable for low and high input frequencies are shown in Figure 33 and Figure 34, respectively. The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated by 50Ω resistor on the secondary side. Placing the termination on the secondary side helps to shield the kicks caused by the input sampling capacitors from the RF transformer leakage inductances. The termination is accomplished by two 25Ω resistors, connected in series, with the center point connected to the 1.5V common-mode. The 4.7Ω resistor in series with each input pin is required to damp the ringing caused by the device package parasitics.

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps to minimize this mismatch, and good performance is obtained for high-frequency input signals. An additional termination resistor pair is required between the two transformers, as shown in Figure 34. The center point of this termination is connected to ground to improve the balance between the positive and negative sides. The values of the terminations between the transformers and on the secondary side must be chosen to achieve an overall 50Ω (in the case of 50Ω source impedance).



**Figure 33. Drive Circuit at Low Input Frequencies**

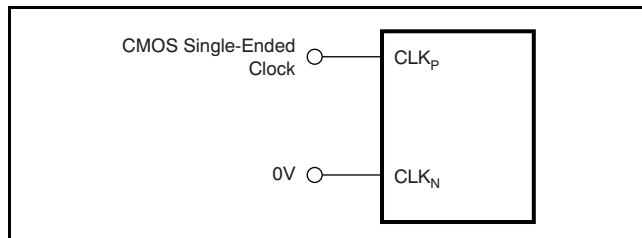


**Figure 34. Drive Circuit at High Input Frequencies**

### CLOCK INPUT

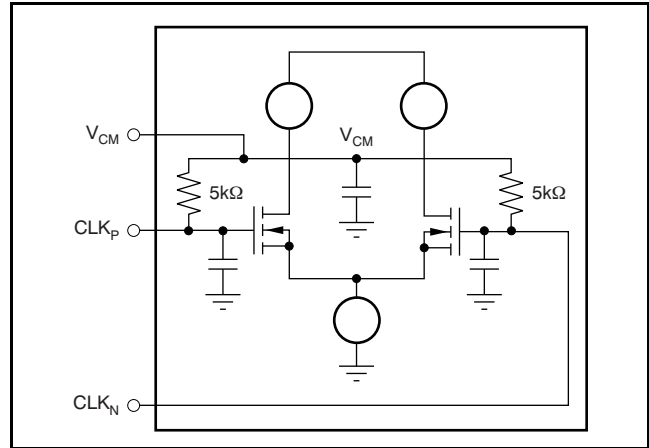
The eight channels on the device operate from a single ADCLK input. To ensure that the aperture delay and jitter are the same for all channels, a clock tree network is used to generate individual sampling clocks to each channel. The clock paths for all the channels are matched from the source point to the sampling circuit. This architecture ensures that the performance and timing for all channels are identical. The use of the clock tree for matching introduces an aperture delay that is defined as the delay between the rising edge of ADCLK and the actual instant of sampling. The aperture delays for all the channels are matched to the best possible extent. A mismatch of  $\pm 20\text{ps}$  ( $\pm 3\sigma$ ) could exist between the aperture instants of the eight ADCs within the same chip. However, the aperture delays of ADCs across two different chips can be several hundred picoseconds apart.

The ADS5287 can be made to operate either in CMOS single-ended clock mode (default is DIFF\_CLK = 0) or differential clock mode (SINE, LVPECL, or LVDS). When operating in the single-ended clock mode, CLK<sub>N</sub> must be forced to 0V<sub>DC</sub>, and the single-ended CMOS applied on the CLK<sub>P</sub> pin. This operation is shown in Figure 35.

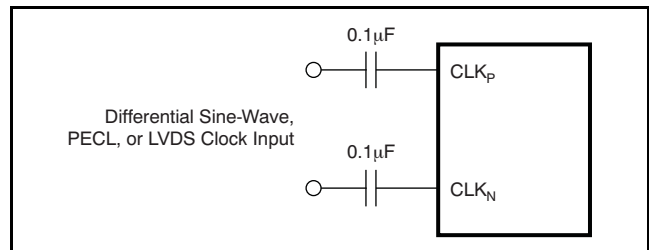


**Figure 35. Single-Ended Clock Driving Circuit (DIFF\_CLK = 0)**

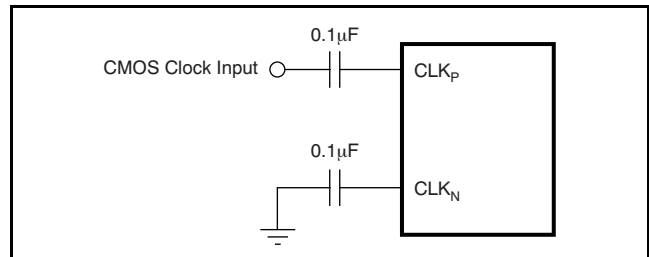
When configured to operate in the differential clock mode (register bit DIFF\_CLK = 1) the ADS5287 clock inputs can be driven differentially (SINE, LVPECL, or LVDS) with little or no difference in performance between them, or with a single-ended (LVCMOS). The common-mode voltage of the clock inputs is set to V<sub>CM</sub> using internal 5kΩ resistors, as shown in Figure 36. This method allows using transformer-coupled drive circuits for a sine wave clock or ac-coupling for LVPECL and LVDS clock sources, as shown in Figure 37. When operating in the differential clock mode, the single-ended CMOS clock can be ac-coupled to the CLK<sub>P</sub> input, with CLK<sub>N</sub> (pin 11) connected to ground with a 0.1μF capacitor, as shown in Figure 38.



**Figure 36. Internal Clock Buffer**



**Figure 37. Differential Clock Driving Circuit (DIFF\_CLK = 1)**



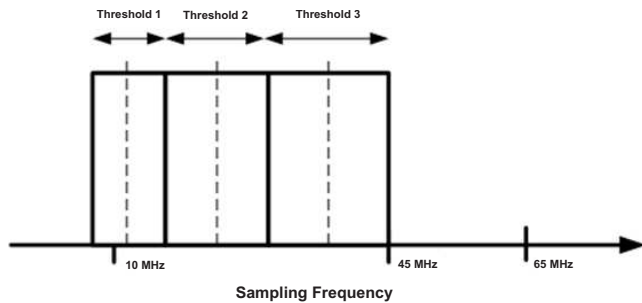
**Figure 38. Single-Ended Clock Driving Circuit When DIFF\_CLK = 1**

For best performance, the clock inputs must be driven differentially in order to reduce susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. If the duty cycle deviates from 50% by more than 2% or 3%, it is recommended to enable the DCC through register bit EN\_DCC.

## PLL OPERATION ACROSS SAMPLING FREQUENCY

The ADS528X uses a PLL for generating the high speed bit clock (LCLK), the frame clock (ADCLK) & internal clocks for the serializer operation.

To enable operation across the entire frequency range, the PLL is automatically configured to one of four states, depending on the sampling clock frequency range. The frequency range detection is automatic and each time the sampling frequency crosses a threshold, the PLL changes its configuration to a new state. To prevent unwanted toggling of PLL state around a threshold, the circuit has an inbuilt hysteresis. The ADS528x has three thresholds – taking into account the hysteresis range of each threshold, variation across devices and temperature, the thresholds can span the sampling clock frequency range from 10MHz to 45MHz.



**Figure 39. Variation of Thresholds Across Sampling Frequency**

Based on actual system clock frequency, there are two scenarios:

1. For sampling clock frequency < 45MSPS

After system power up, depending on the frequency of operation and the frequency threshold for the given device, the frequency range detection circuit may change state once. In some applications where a timing calibration might be done at the system level once after power up, this subsequent change of the PLL state might be undesirable as it can cause a loss of alignment in the received data. A software fix for eliminating this one-time change of PLL state exists using the serial register interface:

- Disable the automatic switch of the PLL configuration based on frequency detected.
- In addition to disabling the switching, it is also required to set the PLL to the correct configuration, depending on the sample clock frequency used in the system.

The following sequence of register writes must be followed:

Step 1: Write Address = 0x01, Data = 0x0010

Step 2: Disable the PLL automatic switch and set the PLL configuration depending on the clock frequency

SAMPLE CLOCK FREQUENCY RANGE (MSPS)		REGISTER SETTING (Hex)	
Min	Max	Address	Data
10	25	E3	0060
15	45	E3	00A0

With the above settings applied for the respective frequency ranges, the part will continue to operate as per the stated datasheet specifications for all timing parameters at all specified frequencies, EXCEPT for the timing specifications at 40MSPS. At 40MSPS, the affected parameters are – Data setup time, Data hold time and Clock propagation delay (refer to LVDS Timing ).

2. For sampling clock frequency ≥ 45MSPS

As there are no PLL thresholds beyond 45MHz, no change in PLL configuration can occur as the temperature in the system stabilizes. The ADS528x can be used in the system without using the above software fix.

## INPUT OVER-VOLTAGE RECOVERY

The differential peak-to-peak full-scale range supported by the ADS5287 is nominally 2.0V. The ADS5287 is specially designed to handle an over-voltage condition where the differential peak-to-peak voltage can be up to twice the ADC full-scale range. If the input common-mode is not considerably off from  $V_{CM}$  during overload (less than 300mV around the nominal value of 1.5V), recovery from an over-voltage pulse input of twice the amplitude of a full-scale pulse is expected to be within one clock cycle when the input switches from overload to zero signal.

## REFERENCE CIRCUIT

The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system would have about 12 octal ADCs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the ADCs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips.

All bias currents required for the internal operation of the device are set using an external resistor to ground at the  $I_{SET}$  pin. Using a 56.2kΩ resistor on  $I_{SET}$  generates an internal reference current of 20μA. This current is mirrored internally to generate the bias current for the internal blocks. Using a larger external

resistor at  $I_{SET}$  reduces the reference bias current and thereby scales down the device operating power. However, it is recommended that the external resistor be within 10% of the specified value of 56.2kΩ so that the internal bias margins for the various blocks are proper.

Buffering the internal bandgap voltage also generates the common-mode voltage  $V_{CM}$ , which is set to the midlevel of  $REF_T$  and  $REF_B$ , and is accessible on pin 53. It is meant as a reference voltage to derive the input common-mode if the input is directly coupled. It can also be used to derive the reference common-mode voltage in the external reference mode. The suggested decoupling for the reference pins is shown in Figure 40.

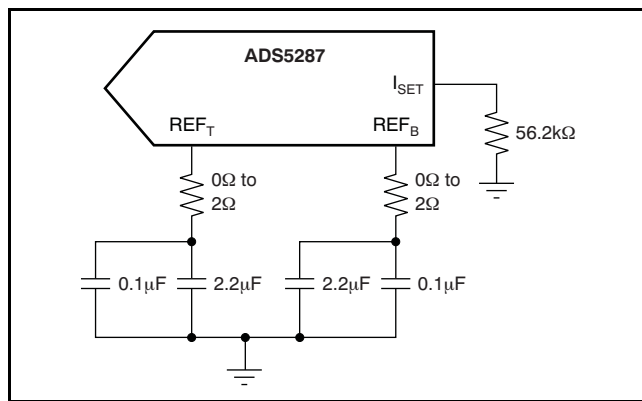


Figure 40. Suggested Decoupling on the Reference Pins

The device also supports the use of external reference voltages. There are two methods to force the references externally. The first method involves pulling INT/EXT low and forcing externally  $REF_T$  and  $REF_B$  to 2.5V and 0.5V nominally, respectively. In this mode, the internal reference buffer goes to a 3-state output. The external reference driving circuit should be designed to provide the required switching current for the eight ADCs inside the chip. It should be noted that in this mode,  $V_{CM}$  and  $I_{SET}$  continue to be generated from the internal bandgap voltage, as in the internal reference mode. It is therefore important to ensure that the common-mode voltage of the externally-forced reference voltages matches to within 50mV of  $V_{CM}$ .

The second method of forcing the reference voltages externally can be accessed by pulling INT/EXT low, and programming the serial interface to drive the external reference mode through the  $V_{CM}$  pin (register bit called EXT\_REF\_VCM). In this mode,  $V_{CM}$  becomes configured as an input pin that can be driven from external circuitry. The internal reference buffers driving  $REF_T$  and  $REF_B$  are active in this mode. Forcing 1.5V on the  $V_{CM}$  pin in the mode results in  $REF_T$  and  $REF_B$  coming to 2.5V and 0.5V, respectively. In general, the voltages on  $REF_T$  and  $REF_B$  in this mode are given by Equation 4 and Equation 5, respectively:

$$V_{REF_T} = 1.5V + \frac{V_{CM}}{1.5V} \tag{4}$$

$$V_{REF_B} = 1.5V - \frac{V_{CM}}{1.5V} \tag{5}$$

Table 7 describes the state of the reference voltage internal buffers during various combinations of the PD, INT/EXT, and EXT\_REF\_VCM register bits.

Table 7. State of Reference Voltages for Various Combinations of PD, INT/EXT, and EXT\_REF\_VCM

REGISTER BIT	INTERNAL BUFFER STATE							
	0	0	1	1	0	0	1	1
PD	0	0	1	1	0	0	1	1
INT/EXT	0	1	0	1	0	1	0	1
EXT_REF_VCM	0	0	0	0	1	1	1	1
$REF_T$ buffer	3-state	2.5V	3-state	2.5V <sup>(1)</sup>	$1.5V + V_{CM}/1.5V$	Do not use	2.5V <sup>(1)</sup>	Do not use
$REF_B$ buffer	3-state	0.5V	3-state	0.5V <sup>(1)</sup>	$1.5V - V_{CM}/1.5V$	Do not use	0.5V <sup>(1)</sup>	Do not use
$V_{CM}$ pin	1.5V	1.5V	1.5V	1.5V	Force	Do not use	Force	Do not use

(1) Weakly forced with reduced strength.

### NOISE COUPLING ISSUES

High-speed mixed signals are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffers. Maximum care is taken to isolate these noise sources from the sensitive analog blocks. As a starting point, the analog and digital domains of the device are clearly demarcated. AVDD and AVSS are used to denote the supplies for the analog

sections, while LVDD and LVSS are used to denote the digital supplies. Care is taken to ensure that there is minimal interaction between the supply sets within the device. The extent of noise coupled and transmitted from the digital to the analog sections depends on:

1. The effective inductances of each of the supply and ground sets.
2. The isolation between the digital and analog supply and ground sets.

Smaller effective inductance of the supply and ground pins leads to better noise suppression. For this reason, multiple pins are used to drive each supply and ground. It is also critical to ensure that the impedances of the supply and ground lines on the board are kept to the minimum possible values. Use of ground planes in the printed circuit board (PCB) as well as large decoupling capacitors between the supply and ground lines are necessary to obtain the best possible SNR performance from the device.

It is recommended that the isolation be maintained on the board by using separate supplies to drive AVDD and LVDD, as well as separate ground planes for AVSS and LVSS. The use of LVDS buffers reduces the injected noise considerably, compared to CMOS buffers. The current in the LVDS buffer is independent of the direction of switching. Also, the low output swing as well as the differential nature of the LVDS buffer results in low-noise coupling.

## REVISION HISTORY

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**Changes from Revision B (March 2008) to Revision C** **Page**

- Changed [Initialization Registers](#) section to include Initialization Register 1 ..... 3
  - In the [Input Common-Mode Current](#) section, changed *Initialization Register 5* to *Initialization Registers 1 and 5* to reflect change in [Initialization Registers](#) table ..... 32
- 

**Changes from Revision C (March 2008) to Revision D** **Page**

- Added table in the INITIALIZATION REGISTERS section ..... 3
  - Added table in the LVDS OUTPUT TIMING CHARACTERISTICS section ..... 12
  - Added PLL OPERATION ACROSS SAMPLING FREQUENCY section ..... 35
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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5287IRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5287	<a href="#">Samples</a>
ADS5287IRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5287	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5287IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5287IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

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