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JAJSHX5F-OCTOBER 2010-REVISED SEPTEMBER 2019

Design

ADS1118 超小型、低消費電力 16 ビット A/D コンバータ、 SPI™互換イ ンターフェイス、内部基準電圧、温度センサ付き

- 1 特長
- 超小型 X2QFN パッケージ: 2mm × 1.5mm × 0.4mm
- 広い電源電圧範囲:2V~5.5V
- 低消費電流

Texas

INSTRUMENTS

- 連続モード:わずか 150uA
- シングル・ショット・モード:自動パワー・ダウン
- データ・レートを設定可能: 8SPS~860SPS
- 収束時間は1サイクル
- 低ドリフト基準電圧を内蔵
- 内蔵温度センサ: 誤差 0.5℃ (最大値) : 0℃~70℃
- 内蔵発振器
- 内蔵 PGA
- 4 つのシングル・エンドまたは2 つの差動入力
- 2 アプリケーション
- 温度測定
 - 熱電対測定
 - 浴接点補償
 - サーミスタ測定
- ポータブル機器
- ファクトリ・オートメーションとプロセス制御

3 概要

ADS1118 は、高精度、低消費電力の 16 ビット・アナログ /デジタル・コンバータ (ADC) であり、最も一般的なセンサ 信号を測定するために必要なすべての機能を超小型リー ドレス X2QFN-10 パッケージまたは VSSOP-10 パッ ケージに統合しています。ADS1118 はプログラマブル・ ゲイン・アンプ (PGA)、基準電圧、発振器、高精度温度セ ンサを内蔵しています。これらの機能を備え 2V~5.5V の 幅広い電源電圧範囲に対応する ADS1118 は、電力とス ペースの制約が厳しいセンサ測定アプリケーションに理想 的です。

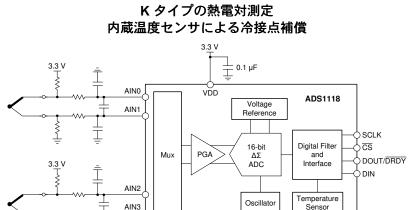
ADS1118 は、最大 860 サンプル/秒 (SPS) のデータ・ レートで変換を実行できます。PGA は

±256mV~±6.144Vの入力範囲に対応しているため、大 きな信号でも小さな信号でも高分解能で測定できます。入 カマルチプレクサ (MUX) により、2 つの差動または 4 つ のシングル・エンド入力を測定できます。高精度温度セン サは、システム・レベルの温度監視または熱電対の冷接点 補償に使用できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)			
ADC1110	X2QFN (10)	1.50mm×2.00mm			
ADS1118	VSSOP (10)	3.00mm×3.00mm			

⁽¹⁾ 提供されているすべてのパッケージについては、データシートの末 尾にある注文情報を参照してください。



GND

AIN3

Oscillato



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改訂履歴 4

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (October 2015) から Revision F に変更

•	Changed maximum VDD voltage from 5.5 V to 7 V in the Absolute Maximum Ratings table
•	Changed bit description of Config Register bit 0

Revision D (October 2013) から Revision E に変更

•	「ESD 定格」表、「機能説明」セクション、「ノイズ特性」セクション、「デバイスの機能モード」セクション、「アプリケーションと実 装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクショ ン、「メカニカル、パッケージ、および注文情報」セクション 追加
•	タイトル、「概要」セクション、「特長」セクション、および前面ページのブロック図を変更
•	Changed title from Product Family to Device Comparison Table and deleted Package Designator column
•	Updated descriptions and changed name of I/O column in Pin Configurations and Functions table
•	Changed digital input voltage range and added minimum specification for T _J in Absolute Maximum Ratings table
•	Added Differential input impedance specification in Electrical Characteristics
•	Changed Condition statement in <i>Timing Requirements: Serial Interface</i>
•	Moved t_{CSDOD} , t_{DOPD} , and t_{CSDOZ} parameters from <i>Timing Requirements</i> to <i>Switching Characteristics</i>
•	Moved t_{CSDOD} and t_{CSDOZ} values from MIN column to MAX column. 10
•	Deleted Noise vs Input Signal, Noise vs Supply Voltage, and Noise vs Input Signal plots
•	Updated Overview section and deleted "Gain = 2/3, 1, 2, 4, 8, or 16" from Functional Block Diagram 18
•	Updated Analog Inputs section
•	Updated Full-Scale Range (FSR) and LSB Size section
•	Updated Reset and Power Up section
•	Updated 32-Bit Data Transmission Cycle section
•	Updated Register Maps section



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Revision C (February 2013) から Revision D に変更

Revision B (August 2012) から Revision C に変更

•	ドキュメントを現行の標準に変更	1
•	「特長」の「低消費電流」の箇条書き項目に、シングル・ショット・モードの副項目を変更	1
•	「特長」の内蔵温度センサについての箇条書き項目を変更	1
•	「概要」セクション 変更	1
•	Changed Product Family table	6
•	Changed Function column name in Pin Descriptions table	6
•	Changed Analog Input, Full-scale input voltage range parameter row in Electrical Characteristics table	7
•	Changed footnotes 1 and 2 in Electrical Characteristics table	7
•	Changed conditions for Electrical Characteristics table	8
•	Changed System Performance, Integral nonlinearity and Gain Error test conditions in Electrical Characteristics table	8
•	Changed first two Temperature Sensor, Temperature sensor accuracy parameter test conditions in Electrical	
	Characteristics table	-
•	Changed Power-Supply Requirements, Supply current parameter test conditions in Electrical Characteristics table	
•	Changed footnote 3 of Timing Requirements: Serial Interface Timing table	
•	Updated Figure 3	
•	Updated Figure 9	
•	Changed title of Figure 11 to Figure 14	
•	Updated Figure 15 and Figure 33	
•	Changed conditions in Figure 21 to Figure 25	
•	Updated Figure 20	
•	Changed comments in Figure 27 to Figure 31	
•	Changed Overview section	
•	Updated Multiplexer section	
•	Changed Full-Scale Input section	
•	Changed Voltage Reference section	
•	Changed Oscillator section	
•	Added multiplication points to example equations in Converting from Digital Codes to Temperature section	
•	Changed Serial Interface, Chip Select, Serial Clock, Data Input, and Data Output and Data Ready sections	
•	Changed Data Retrieval section	
•	Changed Registers section	
•	Changed Aliasing, Reset and Power Up, Operating Modes, and Duty Cycling for Low Power sections	
•	Updated Figure 50	34



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Revision A (July 2011) から Revision B に変更

Revision A (July 2011) から Revision B に変更		Page
•	Added (VSSOP) to titles of Figure 20 to Figure 25	. 14
•	Added Figure 26 to Figure 31	. 15



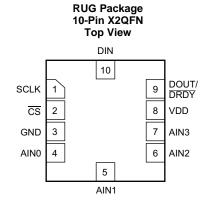
5 概要(続き)

ADS1118 は連続変換モードとシングル・ショット・モード (変換後、自動的にパワー・ダウン状態に移行する)のどちらででも動作します。シングル・ショット・モードを使用すると、アイドル期間中の消費電流を大幅に低減できます。データは、シリアル・ペリフェラル・インターフェイス (SPI™)で転送されます。ADS1118 は、-40℃~+125℃で動作が規定されています。

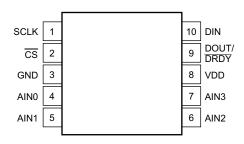
6 Device Comparison Table

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS Differential (Single-Ended)	PGA	INTERFACE	SPECIAL FEATURES
ADS1118	16	860	2 (4)	Yes	SPI	Temperature sensor
ADS1018	12	3300	2 (4)	Yes	SPI	Temperature sensor
ADS1115	16	860	2 (4)	Yes	l ² C	Comparator
ADS1114	16	860	1 (1)	Yes	l ² C	Comparator
ADS1113	16	860	1 (1)	No	I ² C	None
ADS1015	12	3300	2 (4)	Yes	l ² C	Comparator
ADS1014	12	3300	1 (1)	Yes	l ² C	Comparator
ADS1013	12	3300	1 (1)	No	l ² C	None

7 Pin Configuration and Functions







Pin Functions

PIN		ТҮРЕ	DESCRIPTION	
NO.	NAME	ITFE	DESCRIPTION	
1	SCLK	Digital input	Serial clock input	
2	CS	Digital input	Chip select; active low. Connect to GND if not used.	
3	GND	Supply	Ground	
4	AIN0	Analog input	Analog input 0. Leave unconnected or tie to VDD if not used.	
5	AIN1	Analog input	Analog input 1. Leave unconnected or tie to VDD if not used.	
6	AIN2	Analog input	Analog input 2. Leave unconnected or tie to VDD if not used.	
7	AIN3	Analog input	Analog input 3. Leave unconnected or tie to VDD if not used.	
8	VDD	Supply	Power supply. Connect a 100-nF power supply decoupling capacitor to GND.	
9	DOUT/DRDY	Digital output	Serial data output combined with data ready; active low	
10	DIN	Digital input	Serial data input	

8 Specifications

8.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	-0.3	7	V
Analog input voltage	AINO, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	V
Digital input voltage DIN, DOUT/DRDY, SCLK, CS		GND – 0.3	VDD + 0.3	V
Input current, continuous Any pin except power supply pins		-10	10	mA
Temperature	Junction, T _J	-40	150	°C
	Storage, T _{stq}	-60	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM MAX	UNIT
POWER	RSUPPLY				
VDD	Power supply	VDD to GND	2	5.5	V
ANALO	G INPUTS ⁽¹⁾				
FSR	Full-scale input voltage range ⁽²⁾	$V_{IN} = V_{(AINP)} - V_{(AINN)}$	Se	e Table 3	
V _(AINx)	Absolute input voltage		GND	VDD	V
DIGITA	L INPUTS				
	Input voltage		GND	VDD	V
TEMPE	RATURE RANGE				
T _A	Operating ambient temperature		-40	125	°C

(1) AINP and AINN denote the selected positive and negative inputs. AINx denotes one of the four available analog inputs.

(2) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

8.4 Thermal Information

		ADS	51118	
	THERMAL METRIC ⁽¹⁾	DGS (VSSOP)	RUG (X2QFN)	UNIT
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.8	245.2	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	51.5	69.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.4	172	°C/W
тιΨ	Junction-to-top characterization parameter	2.7	8.2	°C/W
ΨЈВ	Junction-to-board characterization parameter	106.5	170.8	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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8.5 Electrical Characteristics

Maximum and minimum specifications apply from $T_A = -40^{\circ}$ C to $+125^{\circ}$ C. Typical specifications are at $T_A = 25^{\circ}$ C. All specifications are at VDD = 3.3 V, data rate = 8 SPS, and full-scale range (FSR) = ± 2.048 V (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
ANALC	OG INPUTS	· · · ·					
		$FSR = \pm 6.144 V^{(1)}$		8			
		FSR = ±4.096 V ⁽¹⁾ , FSR = ±2.048 V		6			
	Common-mode input impedance	FSR = ±1.024 V		3		ΜΩ	
		FSR = ±0.512 V, FSR = ±0.256 V		100			
		$FSR = \pm 6.144 V^{(1)}$		22			
		FSR = ±4.096 V ⁽¹⁾		15			
	Differential input impedance	FSR = ±2.048 V		4.9		MΩ	
		FSR = ±1.024 V		2.4			
		FSR = ±0.512 V, FSR = ±0.256 V		710		kΩ	
SYSTE	M PERFORMANCE						
	Resolution (No missing codes)		16			Bits	
DR	Data rate		8, 16, 32, 64, 1	28, 250, 475,	, 860	SPS	
	Data rate variation	All data rates	-10%		10%		
	Output noise		See Noise Per	rformance sec	ction		
INL	Integral nonlinearity	DR = 8 SPS, FSR = ±2.048 V ⁽²⁾			1	LSB	
		FSR = ±2.048 V, differential inputs		±0.1	±2		
	Offset error	FSR = ±2.048 V, single-ended inputs		±0.25		LSB	
	Offset drift	FSR = ±2.048 V		0.002		LSB/°C	
	Offset power-supply rejection	FSR = ±2.048 V, DC supply variation		0.2		LSB/V	
	Offset channel match	Match between any two inputs		0.6		LSB	
	Gain error ⁽³⁾	FSR = ±2.048 V, T _A = 25°C		0.01%	0.15%		
		FSR = ±0.256 V		7			
	Gain drift ⁽³⁾⁽⁴⁾	FSR = ±2.048 V		5	40	ppm/°C	
		FSR = ±6.144 V ⁽¹⁾		5			
	Gain power-supply rejection			10		ppm/V	
	Gain match ⁽³⁾	Match between any two gains		0.01%	0.1%		
	Gain channel match	Match between any two inputs		0.01%	0.1%		
		At DC, FSR = ±0.256 V		105			
		At DC, FSR = ±2.048 V		100			
CMRR	Common-mode rejection ratio	At DC, FSR = ±6.144 V ⁽¹⁾		90		dB	
		f _{CM} = 50 Hz, DR = 860 SPS		105			
		f _{CM} = 60 Hz, DR = 860 SPS	105			1	
TEMPE	RATURE SENSOR	· · · ·					
	Temperature range		-40		125	°C	
	Temperature resolution			0.03125		°C/LSB	
		$T_A = 0^{\circ}C$ to $70^{\circ}C$		0.2	±0.5		
	Accuracy	$T_{A} = -40^{\circ}C \text{ to } +125^{\circ}C$		0.4	±1	°C	
		vs supply		0.03125	±0.25	°C/V	

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

(2) Best-fit INL; covers 99% of full-scale.

(3) Includes all errors from onboard PGA and voltage reference.

(4) Maximum value specified by characterization.



Electrical Characteristics (continued)

Maximum and minimum specifications apply from $T_A = -40^{\circ}$ C to $+125^{\circ}$ C. Typical specifications are at $T_A = 25^{\circ}$ C. All specifications are at VDD = 3.3 V, data rate = 8 SPS, and full-scale range (FSR) = ± 2.048 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGIT	AL INPUTS/OUTPUTS				·	
VIH	High-level input voltage		0.7 VDD		VDD	V
V _{IL}	Low-level input voltage		GND		0.2 VDD	V
V _{OH}	High-level output voltage	I _{OH} = 1 mA	0.8 VDD			V
V _{OL}	Low-level output voltage	I _{OL} = 1 mA	GND		0.2 VDD	V
Ι _Η	Input leakage, high	V _{IH} = 5.5 V	-10		10	μA
۱L	Input leakage, low	V _{IL} = GND	-10		10	μA
POWE	R SUPPLY					
		Power down, $T_A = 25^{\circ}C$		0.5	2	
	O	Power down			5	•
I _{VDD}	Supply current	Operating, $T_A = 25^{\circ}C$		150	200	μA
		Operating			300	
		VDD = 5 V		0.9		
P_D	Power dissipation	VDD = 3.3 V		0.5		mW
		VDD = 2 V		0.3		

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8.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	IAX	UNIT
t _{CSSC}	Delay time, CS falling edge to first SCLK rising edge ⁽¹⁾	100		ns
t _{sccs}	Delay time, final SCLK falling edge to $\overline{\text{CS}}$ rising edge	100		ns
t _{CSH}	Pulse duration, CS high	200		ns
t _{SCLK}	SCLK period	250		ns
t _{SPWH}	Pulse duration, SCLK high	100		ns
	Pulse duration, SCLK low ⁽²⁾	100		ns
t _{SPWL}	Pulse duration, SCLK low -		28	ms
t _{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t _{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t _{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

 $\overline{\text{CS}}$ can be tied low permanently in case the serial bus is not shared with any other device. Holding SCLK low longer than 28 ms resets the SPI interface. (1)

(2)

8.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	ΤΥΡ ΜΑΧ	UNIT
t _{CSDOD}	Propagation delay time, CS falling edge to DOUT driven	DOUT load = 20 pF 100 k Ω to GND		100	ns
t _{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF 100 k Ω to GND	0	50	ns
t _{CSDOZ}	Propagation delay time, CS rising edge to DOUT high impedance	DOUT load = 20 pF 100 k Ω to GND		100	ns

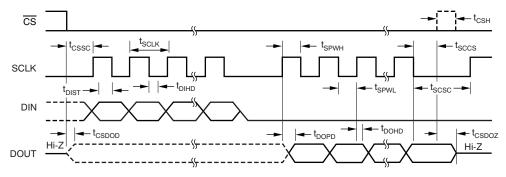
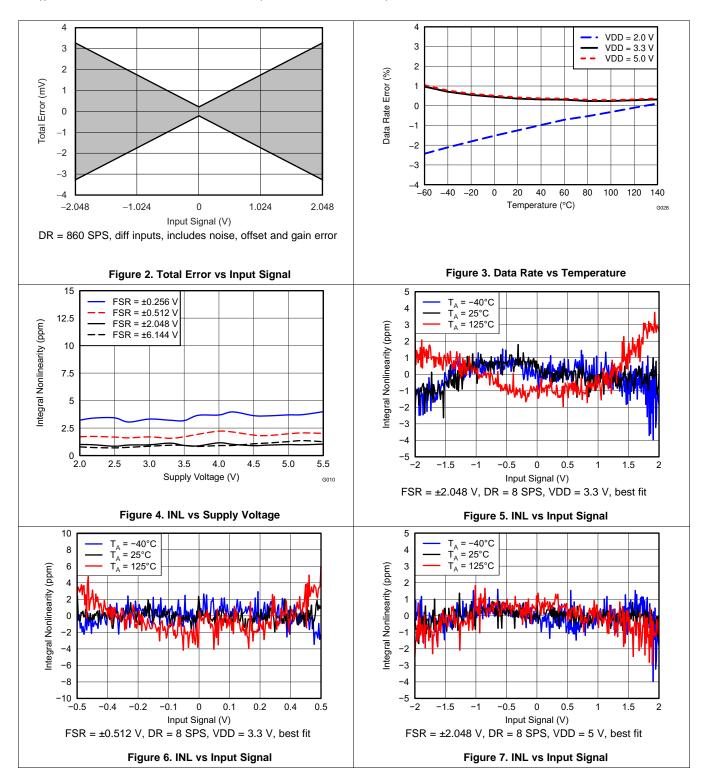


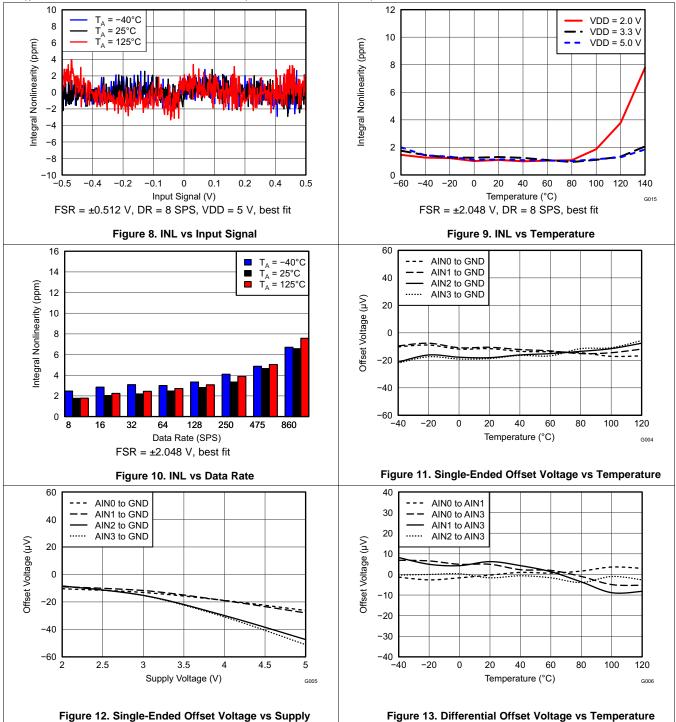
Figure 1. Serial Interface Timing



8.8 Typical Characteristics

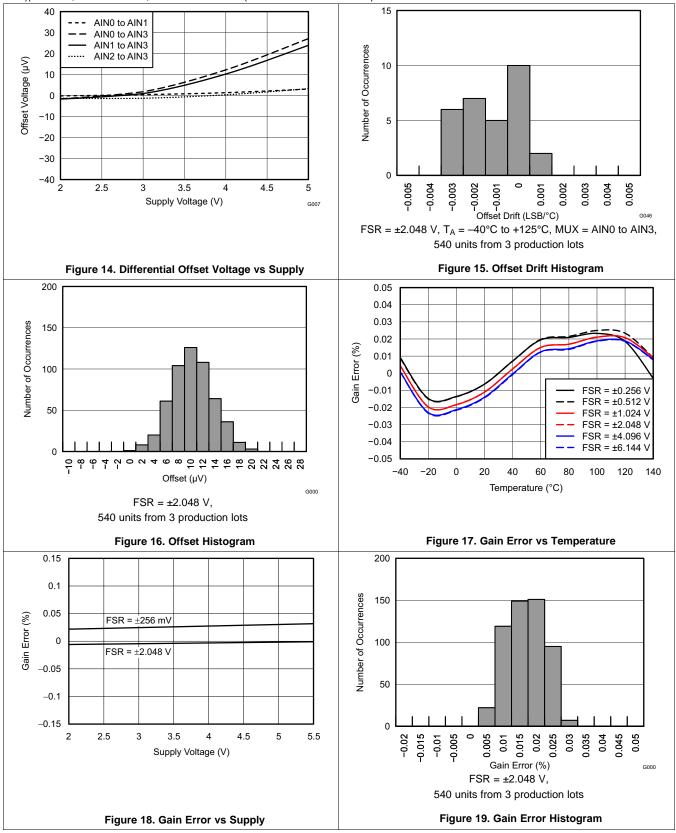


Typical Characteristics (continued)



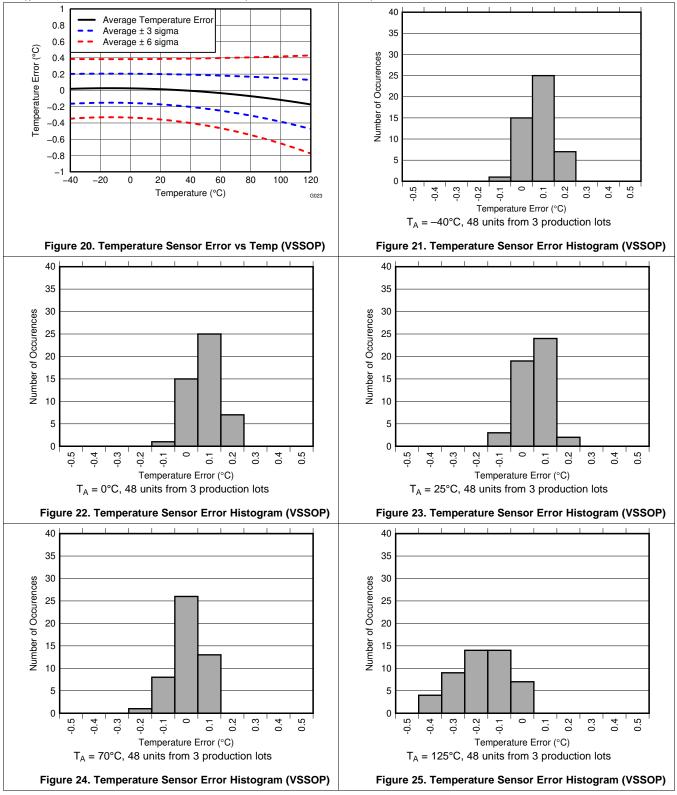


Typical Characteristics (continued)





Typical Characteristics (continued)





Typical Characteristics (continued)

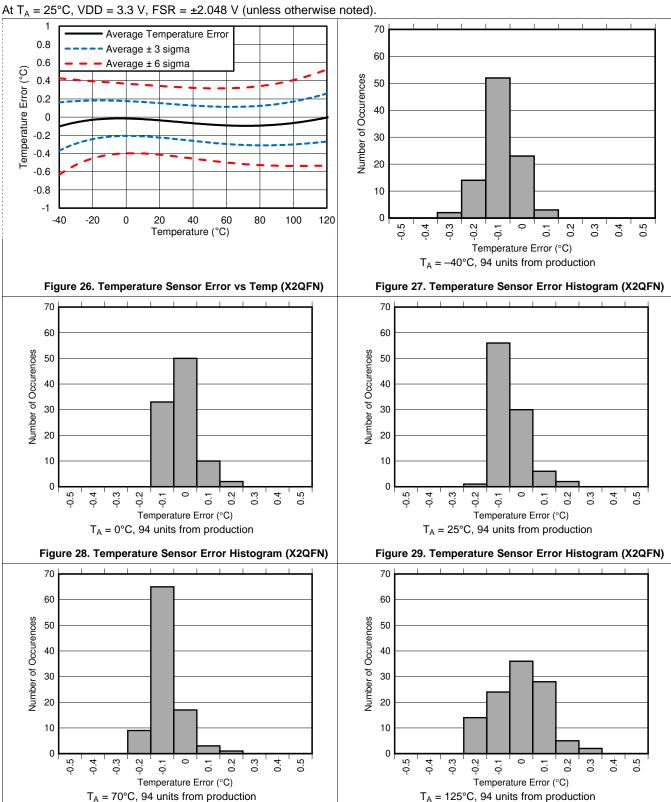
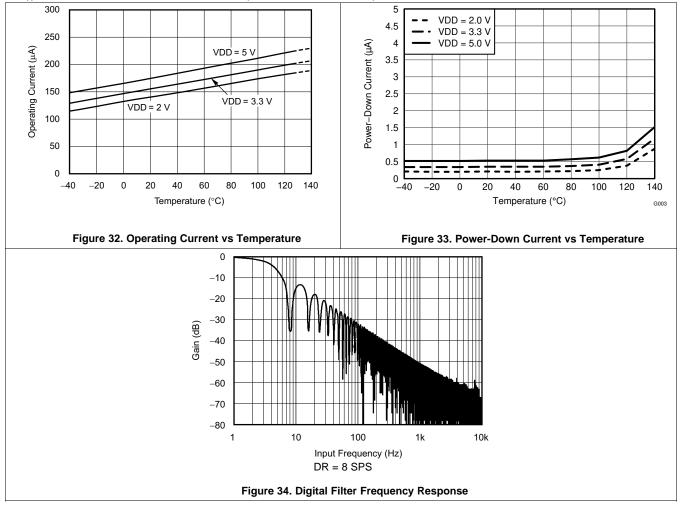


Figure 30. Temperature Sensor Error Histogram (X2QFN)

Figure 31. Temperature Sensor Error Histogram (X2QFN)



Typical Characteristics (continued)





9 Parameter Measurement Information

9.1 Noise Performance

Delta-sigma ($\Delta\Sigma$) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a $\Delta\Sigma$ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 1 and Table 2 summarize the device noise performance. Data are representative of typical noise performance at $T_A = 25^{\circ}$ C with the inputs shorted together externally. Table 1 show the input-referred noise in units of μV_{RMS} for the conditions shown. Note that μV_{PP} values are shown in parenthesis. Table 2 shows the corresponding data in effective number of bits (ENOB) calculated from μV_{RMS} values using Equation 1. The noise-free bits calculated from peak-to-peak noise values using Equation 2 are shown in parenthesis.

$ENOB = In (FSR / V_{RMS-Noise}) / In(2)$

Noise-Free Bits = In (FSR / V_{PP-Noise}) / In(2)

DATA RATE			FSR (Full-Scale	e Range)		
(SPS)	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
16	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
32	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
64	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
128	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (12.35)
250	187.5 (252.09)	125 (148.28)	62.5 (84.03)	31.25 (39.54)	15.62 (16.06)	7.81 (18.53)
475	187.5 (266.92)	125 (227.38)	62.5 (79.08)	31.25 (56.84)	15.62 (32.13)	7.81 (25.95)
860	187.5 (430.06)	125 (266.93)	62.5 (118.63)	31.25 (64.26)	15.62 (40.78)	7.81 (35.83)

Table 1. Noise in μV_{RMS} (μV_{PP}) at VDD = 3.3 V

	FSR (Full-Scale Range)						
(SPS)	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V	
8	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	
16	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	
32	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	
64	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	
128	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.33)	
250	16 (15.57)	16 (15.75)	16 (15.57)	16 (15.66)	16 (15.96)	16 (14.75)	
475	16 (15.49)	16 (15.13)	16 (15.66)	16 (15.13)	16 (14.95)	16 (14.26)	
860	16 (14.8)	16 (14.9)	16 (15.07)	16 (14.95)	16 (14.61)	16 (13.8)	

(1)

(2)



10 Detailed Description

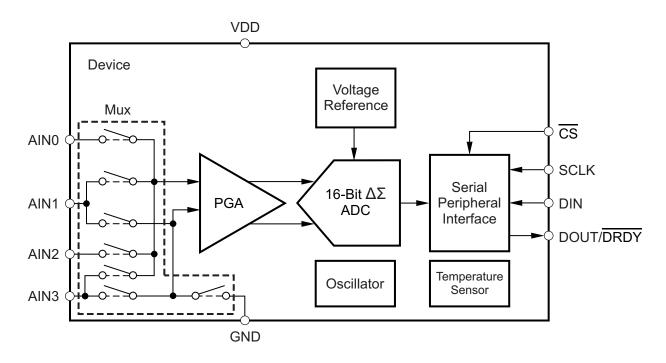
10.1 Overview

The ADS1118 is a very small, low-power, 16-bit, delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC). The ADS1118 consists of a $\Delta\Sigma$ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. *Functional Block Diagram* shows the ADS1118 functional block diagram.

The ADS1118 ADC core measures a differential signal, V_{IN} , that is the difference of $V_{(AINP)}$ and $V_{(AINN)}$. The converter core consists of a differential, switched-capacitor $\Delta\Sigma$ modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1118 has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

10.2 Functional Block Diagram





10.3 Feature Description

10.3.1 Multiplexer

The ADS1118 contains an input multiplexer (mux), as shown in Figure 35. Either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 can be measured differentially to AIN3. The multiplexer is configured by bits MUX[2:0] in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

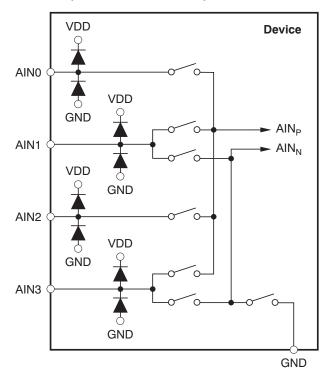


Figure 35. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes indicate negative differential signals; that is, $(V_{(AINP)} - V_{(AINN)}) < 0$. Electrostatic discharge (ESD) diodes to VDD and GND protect the ADS1118 inputs. To prevent the ESD diodes from turning on, keep the absolute voltage on any input within the range given in Equation 3:

$$GND - 0.3 V < V_{(AINx)} < VDD + 0.3 V$$

(3)

If the voltages on the input pins can possibly violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see the *Absolute Maximum Ratings* table).

Also, overdriving one unused input on the ADS1118 may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, clamp the signal with external Schottky diodes.



Feature Description (continued)

10.3.2 Analog Inputs

The ADS1118 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. This frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency ($f_{(MOD)}$). ADS1118 has a 1 MHz internal oscillator which is further divided by a factor of 4 to generate the modulator frequency at 250 kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 36. The resistance is set by the capacitor values and the rate at which they are switched. Figure 37 shows the setting of the switches illustrated in Figure 36. During the sampling phase, switches S₁ are closed. This event charges C_{A1} to V_(AINP), C_{A2} to V_(AINN), and C_B to (V_(AINP) - V_(AINN)). During the discharge phase, S₁ is first opened and then S₂ is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7 V and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the ADS1118 analog inputs. The average value of this current can be used to calculate the effective impedance (Z_{eff}), where Z_{eff} = V_{IN} / I_{AVERAGE}.

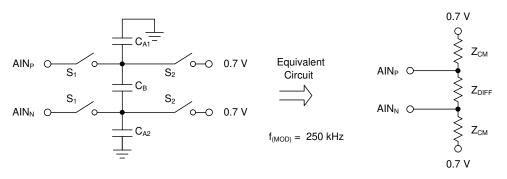


Figure 36. Simplified Analog Input Circuit

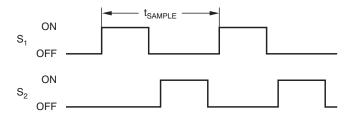


Figure 37. S₁ and S₂ Switch Timing

The common-mode input impedance is measured by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6 M Ω for the default full-scale range. In Figure 36, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the full-scale range. In Figure 36, the differential input impedance is Z_{DIFF} .

Make sure to consider the typical value of the input impedance. Unless the input source has a low impedance, the ADS1118 input impedance may affect the measurement accuracy. For sources with high-output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible, and can be ignored.



Feature Description (continued)

10.3.3 Full-Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented before the ADS1118 $\Delta\Sigma$ core. The full-scale range is configured by three bits (PGA[2:0]) in the Config Register and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, ±0.256 V. Table 3 shows the FSR together with the corresponding LSB size. LSB size is calculated from full-scale voltage by the formula shown in Equation 4. However, analog input voltages may never exceed the analog input voltage limits given in the *Electrical Characteristics*. If a supply voltage of VDD greater than 4 V is used, the ±6.144 V full-scale range allows input voltages to extend up to the supply. Note though that in this case, or whenever the supply voltage is less than the full-scale range (for example, VDD = 3.3 V and full-scale range = ±4.096 V), a full-scale ADC output code cannot be obtained. This inability means that some dynamic range is lost.

LSB =	FSR /	2 ¹⁶
-------	-------	-----------------

(4)

FSR	LSB SIZE
±6.144 V ⁽¹⁾	187.5 μV
±4.096 V ⁽¹⁾	125 μV
±2.048 V	62.5 μV
±1.024 V	31.25 μV
±0.512 V	15.625 μV
±0.256 V	7.8125 μV

Table 3. Full-Scale Range and Corresponding LSB Size

 This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V must be applied to this device.

10.3.4 Voltage Reference

The ADS1118 has an integrated voltage reference. An external reference cannot be used with this device. Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics*.

10.3.5 Oscillator

The ADS1118 has an integrated oscillator running at 1 MHz. No external clock is required to operate the device. Note that the internal oscillator drifts over temperature and time. The output data rate will scale proportional with the oscillator frequency.

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10.3.6 Temperature Sensor

The ADS1118 offers an integrated precision temperature sensor. The temperature sensor mode is enabled by setting bit TS_MODE = 1 in the Config Register. Temperature data are represented as a 14-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format, as shown in Table 4.

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
-0.25	11 1111 1111 1000	3FF8
-25	11 1100 1110 0000	3CE0
-40	11 1011 0000 0000	3B00

 Table 4. 14-Bit Temperature Data Format

10.3.6.1 Converting from Temperature to Digital Codes

For positive temperatures:

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit, left justified format with the MSB = 0 to denote the positive sign. **Example:** $50^{\circ}C / (0.03125^{\circ}C/count) = 1600 = 0640h = 00\ 0110\ 0100\ 0000$

For negative temperatures:

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then denote the negative sign with the MSB = 1.

Example: $|-25^{\circ}C| / (0.03125^{\circ}C/count) = 800 = 0320h = 00 0011 0010 0000$

Twos complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

10.3.6.2 Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.03125° C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all of the bits. Then multiply the result by -0.03125° C.

Example: The device reads back 0960h: 0960h has an MSB = 0.

0960h × 0.03125°C = 2400 × 0.03125°C = 75°C

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.

Subtract 1 and complement the result: 3CE0h \rightarrow 0320h

 $0320h \times (-0.03125^{\circ}C) = 800 \times (-0.03125^{\circ}C) = -25^{\circ}C$



10.4 Device Functional Modes

10.4.1 Reset and Power Up

When the ADS1118 powers up, a reset is performed. As part of the reset process, the ADS1118 sets all of its bits in the Config Register to the respective default settings. By default, the ADS1118 enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1118 is intended to relieve systems with tight power-supply requirements from encountering a surge during power up.

10.4.2 Operating Modes

The ADS1118 operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the Config register selects the respective operating mode.

10.4.2.1 Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, the ADS1118 enters a power-down state, and operates in single-shot mode. This power-down state is the default state for the ADS1118 when power is first applied. Although powered down, the device still responds to commands. The ADS1118 remains in this power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is asserted, the device powers up, resets the SS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a 1 to the SS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the Config register.

10.4.2.2 Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0), the ADS1118 continuously performs conversions. When a conversion completes, the ADS1118 places the result in the Conversion register and immediately begins another conversion. To switch to single-shot mode, write a 1 to the MODE bit in the Config register, or reset the device.

10.4.3 Duty Cycling for Low Power

The noise performance of a $\Delta\Sigma$ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADS1118 supports duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1118 in power-down state with a data rate set to 860 SPS can be operated by a microcontroller that instructs a single-shot conversion every 125 ms (8 SPS). Because a conversion at 860 SPS only requires approximately 1.2 ms, the ADS1118 enters power-down state for the remaining 123.8 ms. In this configuration, the ADS1118 consumes approximately 1/100th the power that is otherwise consumed in continuous conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADS1118 offers lower data rates that do not implement duty cycling and also offers improved noise performance if required.



10.5 Programming

10.5.1 Serial Interface

The SPI-compatible serial interface consists of either four signals (\overline{CS} , SCLK, DIN, and DOUT/ \overline{DRDY}), or three signals (in which case \overline{CS} may be tied low). The interface is used to read conversion data, read and write registers, and control device operation.

10.5.2 Chip Select (CS)

The chip select pin (CS) selects the ADS1118 for SPI communication. This feature is useful when multiple devices share the same serial bus. Keep CS low for the duration of the serial communication. When CS is taken high, the serial interface is reset, SCLK is ignored, and DOUT/DRDY enters a high-impedance state. In this state, DOUT/DRDY cannot provide data-ready indication. In situations where multiple devices are present and DOUT/DRDY must be monitored, lower CS periodically. At this point, the DOUT/DRDY pin either immediately goes high to indicate that no new data are available, or immediately goes low to indicate that new data are present in the Conversion register and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption.

10.5.3 Serial Clock (SCLK)

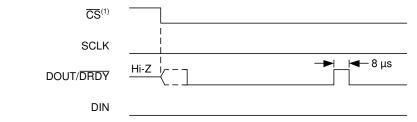
The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/DRDY pins into and out of the ADS1118. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for 28 ms, the serial interface resets and the next SCLK pulse starts a new communication cycle. This time-out feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

10.5.4 Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1118. The device latches data on DIN on the SCLK falling edge. The ADS1118 never drives the DIN pin.

10.5.5 Data Output and Data Ready (DOUT/DRDY)

The data output and data ready pin (DOUT/DRDY) is used with SCLK to read conversion and register data from the ADS1118. Data on DOUT/DRDY are shifted out on the SCLK rising edge. DOUT/DRDY is also used to indicate that a conversion is complete and new data are available. This pin transitions low when new data are ready for retrieval. DOUT/DRDY is also able to trigger a microcontroller to start reading data from the ADS1118. In continuous-conversion mode, DOUT/DRDY transitions high again 8 µs before the next data ready signal (DOUT/DRDY low) if no data are retrieved from the device. This transition is shown in Figure 38. Complete the data transfer before DOUT/DRDY returns high.



(1) CS may be held low. If CS is low, DOUT/DRDY asserts low indicating new data are available.

Figure 38. DOUT/DRDY Behavior Without Data Retrieval in Continuous Conversion Mode

When CS is high, <u>DOUT/DRDY</u> is configured by default with a weak internal pullup resistor. This feature reduces the risk of DOUT/DRDY floating near midsupply and causing leakage current in the master device. To disable this pullup resistor and place the device into a high-impedance state, set the PULL_UP_EN bit to 0 in the Config Register.



Programming (continued)

10.5.6 Data Format

The ADS1118 provides 16 bits of data in binary twos complement format. A positive full-scale input produces an output code of 7FFFh and a negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 5 summarizes the ideal output codes for different input signals. Figure 39 shows code transitions versus input voltage.

	•
INPUT SIGNAL, V _{IN} (AIN _P – AIN _N)	IDEAL OUTPUT CODE ⁽¹⁾
≥ +FS (2 ¹⁵ – 1)/2 ¹⁵	7FFFh
+FS/2 ¹⁵	0001h
0	0
-FS/2 ¹⁵	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

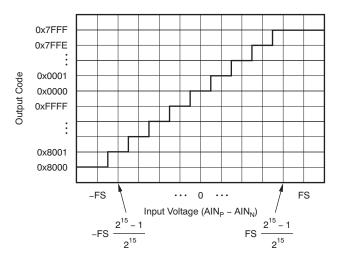


Figure 39. ADS1118 Code Transition Diagram

10.5.7 Data Retrieval

Data is written to and read from the ADS1118 in the same manner for both single-shot and continuous conversion modes, without having to issue any commands. The operating mode for the ADS1118 is selected by the MODE bit in the Config register.

Set the MODE bit to 0 to put the device in continuous-<u>conversion</u> mode. In continuous-conversion mode, the device is constantly starting new conversions even when CS is high.

Set the MODE bit to 1 for single-shot mode. In single-shot mode, a new conversion only starts by writing a 1 to the SS bit.

The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/DRDY asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/DRDY. The MSB of the data (bit 15) on DOUT/DRDY is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/DRDY, new Config register data are latched on DIN on the SCLK falling edge.

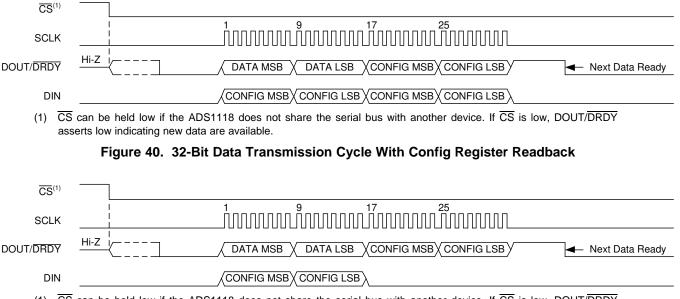
The ADS1118 also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits (only used when the CS line can be controlled and is not permanently tied low).



10.5.7.1 32-Bit Data Transmission Cycle

The data in a 32-bit data transmission cycle consists of four bytes: two bytes for the conversion result, and an additional two bytes for the Config Register read back. The device always reads the MSB first.

Write the same Config register setting twice during one transmission cycle as shown in Figure 40. If convenient, write the Config register setting once during the first half of the transmission cycle, and then hold the DIN pin either low (as shown in Figure 41) or high during the second half of the cycle. If no update to the Config register is required, hold the DIN pin either low or high during the entire transmission cycle. The Config register setting written in the first two bytes of a 32-bit transmission cycle is read back in the last two bytes of the same cycle.



(1) CS can be held low if the ADS1118 does not share the serial bus with another device. If CS is low, DOUT/DRDY asserts low indicating new data are available.

Figure 41. 32-Bit Data Transmission Cycle: DIN Held Low

10.5.7.2 16-Bit Data Transmission Cycle

If Config Register data are not required to be readback, the ADS1118 conversion data can also be clocked out in a short 16-bit data transmission cycle, as shown in Figure 42. Therefore, CS must be taken high after the 16th SCLK cycle. Taking CS high resets the SPI interface. The next time CS is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/DRDY is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/DRDY is high, the same result from the previous data transmission cycle is read.

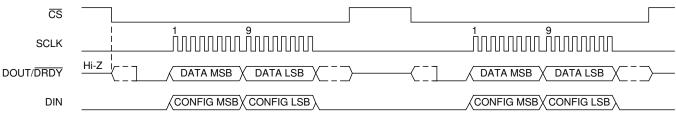


Figure 42. 16-Bit Data Transmission Cycle



10.6 Register Maps

The ADS1118 has two registers that are accessible through the SPI interface. The Conversion Register contains the result of the last conversion. The Config Registerallows the user to change the ADS1118 operating modes and query the status of the devices.

10.6.1 Conversion Register [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary twos complement format. Following power up, the Conversion register is cleared to 0, and remains 0 until the first conversion is completed. The register format is shown in Figure 43.

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R-0h							
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Conversion Register Field Descriptions

Bit	Field	Туре	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

10.6.2 Config Register [reset = 058Bh]

The 16-bit Config register can be used to control the ADS1118 operating mode, input selection, data rate, full-scale range, and temperature sensor mode. The register format is shown in Figure 44.

Figure 44. Config Register

15	14	13	12	11	10	9	8
SS		MUX[2:0]			PGA[2:0]		MODE
R/W-0h		R/W-0h			R/W-2h		R/W-1h
7	6	5	4	3	2	1	0
	DR[2:0]		TS_MODE	PULL_UP_EN	NOP[1:0]		Reserved
	R/W-4h		R/W-0h	R/W-1h	R/W	′-1h	R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Config Register Field Descriptions

Bit	Field	Туре	Reset	Description
15 SS				Single-shot conversion start This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing.
	R/W	Oh	When writing: 0 = No effect 1 = Start a single conversion (when in power-down state) Always reads back 0 (default).	
14:12	MUX[2:0]	R/W	Oh	Input multiplexer configurationThese bits configure the input multiplexer. $000 = AIN_P$ is AIN0 and AIN_N is AIN1 (default) $001 = AIN_P$ is AIN0 and AIN_N is AIN3 $010 = AIN_P$ is AIN1 and AIN_N is AIN3 $011 = AIN_P$ is AIN2 and AIN_N is AIN3 $100 = AIN_P$ is AIN0 and AIN_N is GND $101 = AIN_P$ is AIN1 and AIN_N is GND $110 = AIN_P$ is AIN2 and AIN_N is GND $110 = AIN_P$ is AIN2 and AIN_N is GND

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Bit	Field	Туре	Reset	Description
11:9	PGA[2:0]	R/W	2h	Programmable gain amplifier configuration These bits configure the programmable gain amplifier. $000 = FSR \text{ is } \pm 6.144 \text{ V}^{(1)}$ $001 = FSR \text{ is } \pm 4.096 \text{ V}^{(1)}$ $010 = FSR \text{ is } \pm 2.048 \text{ V} (default)$ $011 = FSR \text{ is } \pm 0.244 \text{ V}$ $100 = FSR \text{ is } \pm 0.512 \text{ V}$ $101 = FSR \text{ is } \pm 0.256 \text{ V}$ $111 = FSR \text{ is } \pm 0.256 \text{ V}$ $111 = FSR \text{ is } \pm 0.256 \text{ V}$
8	MODE	R/W	1h	Device operating mode This bit controls the ADS1118 operating mode. 0 = Continuous conversion mode 1 = Power-down and single-shot mode (default)
7:5	DR[2:0]	R/W	4h	Data rate These bits control the data rate setting. 000 = 8 SPS 001 = 16 SPS 010 = 32 SPS 011 = 64 SPS 100 = 128 SPS (default) 101 = 250 SPS 110 = 475 SPS 111 = 860 SPS
4	TS_MODE	R/W	0h	Temperature sensor mode This bit configures the ADC to convert temperature or input signals. 0 = ADC mode (default) 1 = Temperature sensor mode
3	PULL_UP_EN	R/W	1h	Pullup enable This bit enables a weak internal pullup resistor on the DOUT/DRDY pin only when CS is high. When enabled, an internal 400-kΩ resistor connects the bus line to supply. When disabled, the DOUT/DRDY pin floats. 0 = Pullup resistor disabled on DOUT/DRDY pin 1 = Pullup resistor enabled on DOUT/DRDY pin (default)
2:1	NOP[1:0]	R/W	1h	 No operation The NOP[1:0] bits control whether data are written to the Config register or not. For data to be written to the Config register, the NOP[1:0] bits must be '01'. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register. 00 = Invalid data, do not update the contents of the Config register 01 = Valid data, update the Config register (default) 10 = Invalid data, do not update the contents of the Config register 11 = Invalid data, do not update the contents of the Config register
0	Reserved	R	1h	Reserved Writing either 0 or 1 to this bit has no effect. Always reads back 1.

Table 7. Config Register Field Descriptions (continued)

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V must be applied to this device.



11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The ADS1118 is a precision, 16-bit $\Delta\Sigma$ ADC that offers many integrated features to ease the measurement of the most common sensor types including various type of temperature and bridge sensors. The following sections give example circuits and suggestions for using the ADS1118 in various situations.

11.1.1 Serial Interface Connections

The principle serial interface connections for the ADS1118 are shown in Figure 45.

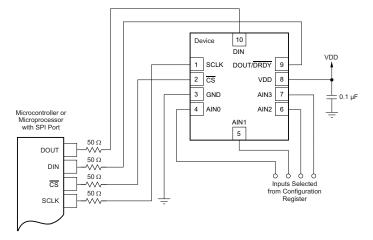


Figure 45. Typical Connections of the ADS1118

Most microcontroller SPI peripherals can operate with the ADS1118. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the ADS1118 can be found in the *Timing Requirements: Serial Interface* section.

It is a good practice to place $50-\Omega$ resistors in the series path to each of the digital pins to provide some short circuit protection. Care must be taken to still meet all SPI timing requirements because these additional series resistors along with the bus parasitic capacitances present on the digital signal lines could slew the signals.

The fully-differential input of the ADS1118 is ideal for connecting to differential sources (such as thermocouples and thermistors) with a moderately low source impedance. Although the ADS1118 can read fully-differential signals, the device cannot accept negative voltages on either of its inputs because of ESD protection diodes on each pin. When an input exceeds supply or drops below ground, these diodes turn on to prevent any ESD damage to the device.

11.1.2 GPIO Ports for Communication

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADS1118 can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface only requires that the pins be configured as push or pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 28 ms, the communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 28 ms between pulses.

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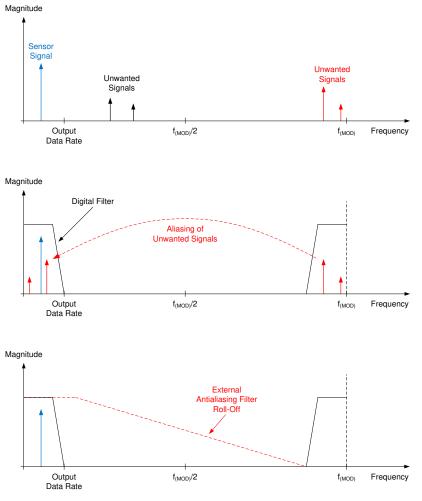


Application Information (continued)

11.1.3 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter repeats at multiples of the sampling frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.





Many sensor signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. In this case, the sensor signal does not alias back into the pass-band when using a $\Delta\Sigma$ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed-circuit-board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.



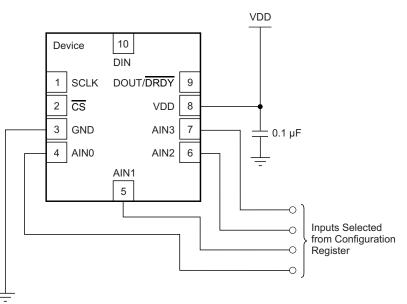
Application Information (continued)

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{(MOD)}$ / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1118 attenuates signals to a certain degree, as shown in Figure 34. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10x higher is generally a good starting point for a system design.

11.1.4 Single-Ended Inputs

Although the ADS1118 has two differential inputs, the device can measure four single-ended signals. Figure 47 shows a single-ended connection scheme. The ADS1118 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection in the Config Register. The single-ended signal can range from 0 V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to this circuit because the ADS1118 can only accept positive voltages with respect to ground. The ADS1118 does not lose linearity within the input range.

The ADS1118 offers a differential input voltage range of \pm FS. The single-ended circuit shown in Figure 47 however only uses the positive half of the ADS1118 FS input voltage range because differentially negative inputs are not produced. Because only half of the FS range is used, one bit of resolution is lost. For optimal noise performance, TI recommends using differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.



NOTE: Digital pin connections omitted for clarity.

Figure 47. Measuring Single-Ended Inputs

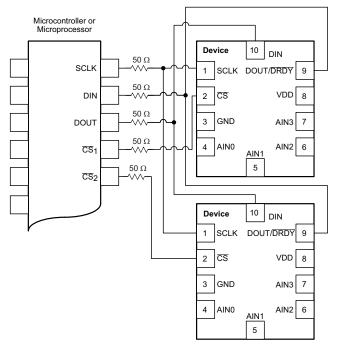
The ADS1118 is also designed to allow AIN3 to serve as a common point for measurements by adjusting the mux configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration the ADS1118 can operate with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when $GND < V_{(AIN3)} < VDD$; however, common-mode noise attenuation is not offered.



Application Information (continued)

11.1.5 Connecting Multiple Devices

When connecting multiple ADS1118 devices to a single SPI bus, SCLK, DIN, and DOUT/DRDY can be safely shared by using a dedicated chip-select (CS) for each SPI-enabled device. By default, when CS goes high for the ADS1118, DOUT/DRDY is pulled up to VDD by a weak pullup resistor. This feature is intended to prevent DOUT/DRDY from floating near mid-rail and causing excess current leakage on a microcontroller input. If the PULL_UP_EN bit in the Config Register is set to 0, the DOUT/DRDY pin enters a 3-state mode when CS transitions high. The ADS1118 cannot issue a data ready pulse on DOUT/DRDY when CS is high. To evaluate when a new conversion is ready from the ADS1118 when using multiple devices, the master can periodically drop CS to the ADS1118. When CS goes low, the DOUT/DRDY pin immediately drives either high or low. If the DOUT/DRDY line drives low on a low CS, new data are currently available for clocking out at any time. If the DOUT/DRDY line drives high, no new data are available and the ADS1118 returns the last read conversion result. Valid data can be retrieved from the ADS1118 at anytime without concern of data corruption. If a new conversion is initiated.



NOTE: Power and input connections omitted for clarity.

Figure 48. Connecting Multiple ADS1118s



ADS1118 JAJSHX5F – OCTOBER 2010– REVISED SEPTEMBER 2019

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Application Information (continued)

11.1.6 Pseudo Code Example

The flow chart in Figure 49 shows a pseudo code sequence with the required steps to set up communication between the device and a microcontroller to take subsequent readings from the ADS1118. As an example, the default Config Register settings are changed to set up the device in FSR = ± 0.512 V, continuous conversion mode and 64-SPS data rate.

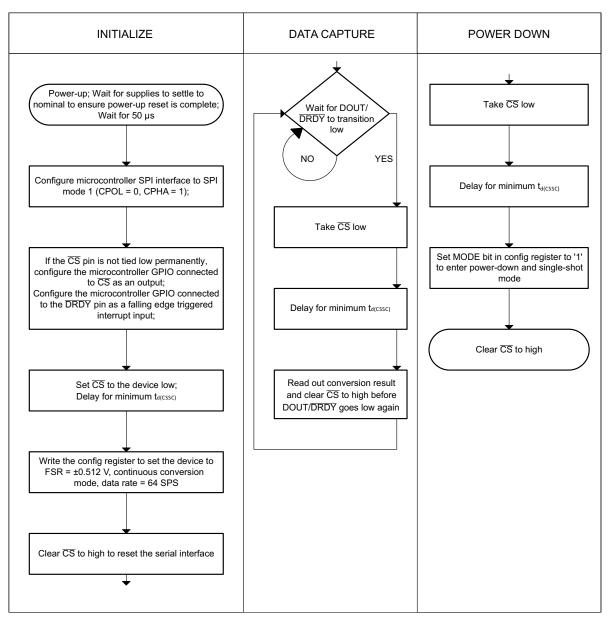


Figure 49. Pseudo Code Example Flow Chart



11.2 Typical Application

Figure 50 shows the basic connections for an independent, two-channel thermocouple measurement system when using the internal high-precision temperature sensor for cold-junction compensation. Apart from the thermocouples, the only external circuitry required are biasing resistors, first order low-pass, anti-aliasing filters, and a power supply decoupling capacitor.

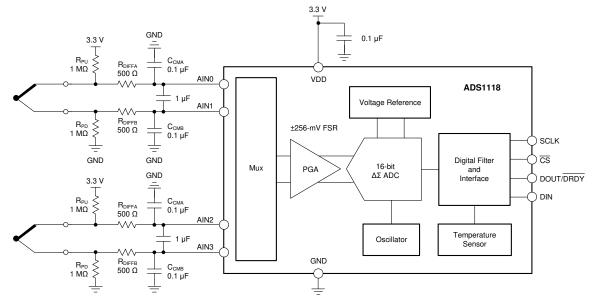


Figure 50. Two-Channel Thermocouple Measurement System

11.2.1 Design Requirements

Table 8 shows the design parameters for this application.

5							
DESIGN PARAMETER	VALUE						
Supply voltage	3.3 V						
Reference voltage	Internal						
Update rate	≥100 readings per second						
Thermocouple type	К						
Temperature measurement range	–200°C to +1250°C						
Measurement accuracy at $T_A = 25^{\circ}C^{(1)}$	±0.7°C						

Table 8. Design Parameters

(1) With offset calibration, and no gain calibration. Measurement does not account for thermocouple inaccuracy.

11.2.2 Detailed Design Procedure

The biasing resistors (R_{PU} and R_{PD}) serve two purposes. The first purpose is to set the common-mode voltage of the thermocouple to within the specified voltage range of the device. The second purpose is to offer a weak pullup and pulldown to detect an open thermocouple lead. When one of the thermocouple leads fails open, the positive input will be pulled to VDD and the negative input will be pulled to GND. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition. When choosing the values of the biasing resistors, care must be taken so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 M Ω to 50 M Ω .



Although the device digital filter attenuates high-frequency components of noise, TI recommends providing a firstorder, passive RC filter at the inputs to further improve performance. The differential RC filter formed by R_{DIFFA} , R_{DIFFB} , and the differential capacitor C_{DIFF} offers a cutoff frequency that is calculated using Equation 5. While the digital filter of the ADS1118 strongly attenuates high-frequency components of noise, TI recommends to provide a first-order, passive RC filter to further suppress high-frequency noise and avoid aliasing. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. TI recommends limiting the filter resistor values to below 1 k Ω .

$$f_{C} = 1 / [2\pi \cdot (R_{DIFFA} + R_{DIFFB}) \cdot C_{DIFF}]$$

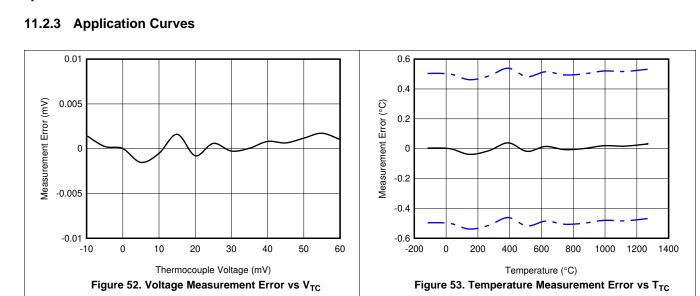
(5)

Two common-mode filter capacitors (C_{CMA} and C_{CMB}) are also added to offer attenuation of high-frequency, common-mode noise components. TI recommends that the differential capacitor C_{DIFF} be at least an order of magnitude (10x) larger than these common-mode capacitors because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The highest measurement resolution is achieved when the largest potential input signal is slightly lower than the FSR of the ADC. From the design requirement, the maximum thermocouple voltage (V_{TC}) occurs at a thermocouple temperature (T_{TC}) of 1250°C. At this temperature, V_{TC} = 50.644 mV, as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature (T_{CJ}) of 0°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to -40°C. A K-type thermocouple at T_{TC} = 1250°C produces an output voltage of V_{TC} = 50.644 mV – (-1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of T_{CJ} = -40°C. The device offers a full-scale range of ±0.256 V and that is what is used in this application example.

The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. The temperature sensor mode is enabled by setting bit TS_MODE = 1 in the Config register. The accuracy of the overall temperature sensor depends on how accurately the ADS1118 can measure the cold junction, and hence, careful component placement and PCB layout considerations must be employed for designing an accurate thermocouple system. The ADS1118 Evaluation Module provides a good starting point and offers an example to achieve good cold-junction compensation performance. The ADS1118 Evaluation Module uses the same schematic as shown in Figure 50, except with only one thermocouple channel connected. Refer to the application note, *Precision Thermocouple Measurement With the ADS1118*, SBAA189, for details on how to optimize your component placement and layout to achieve good cold-junction compensation performance.

The calculation procedure to achieve cold-junction compensation can be done in several ways. A typical way is to interleave readings between the thermocouple inputs and the temperature sensor. That is, acquire one on-chip temperature result, T_{CJ} , for every thermocouple ADC voltage measured, V_{TC} . To account for the cold junction, first convert the temperature sensor reading within the ADS1118 to a voltage (V_{CJ}) that is proportional to the thermocouple currently being used. This process is generally accomplished by performing a reverse lookup on the table used for the thermocouple voltage-to-temperature conversion. Adding these two voltages yields the thermocouple-compensated voltage (V_{Actual}), where $V_{Actual} = V_{CJ} + V_{TC}$. V_{Actual} is then converted to a temperature (T_{Actual}) using the same NIST lookup table. A block diagram showing this process is given in Figure 51. Refer to the application note, *Precision Thermocouple Measurement With the ADS1118*, SBAA189, for a detailed explanation of this method.



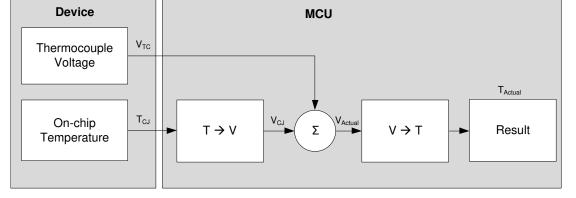


Figure 51. Software Flow Block Diagram

Figure 52 and Figure 53 show the measurement results. The measurements are taken at $T_A = T_{CJ} = 25^{\circ}$ C. A system offset calibration is performed at $T_{TC} = 25^{\circ}$ C that equates to $V_{TC} = 0$ V when $T_{CJ} = 25^{\circ}$ C. No gain calibration was performed during the measurements. The data in Figure 52 are taken using a precision voltage source as the input signal instead of a thermocouple. The solid black line in Figure 53 is the respective temperature measurement error and is calculated from the data in Figure 52 using the NIST tables. The solid black line in Figure 53 is the measurement error due to the ADC gain and nonlinearity error. The dashed blue lines in Figure 53 include the guard band for the temperature sensor inaccuracy (±0.5°C), in addition to the device gain and nonlinearity error. Note that the measurement results in Figure 52 and Figure 53 do not account for the thermocouple inaccuracy that must also be considered while designing a thermocouple measurement system.

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12 Power Supply Recommendations

The device requires a single power supply, VDD, to power both the analog and digital circuitry of the device.

12.1 Power-Supply Sequencing

Wait approximately 50 μ s after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

12.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. VDD must be decoupled with at least a 0.1- μ F capacitor, as shown in Figure 54. The 0.1- μ F bypass capacitor supplies the momentary bursts of extra current required from the supply when the ADS1118 is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

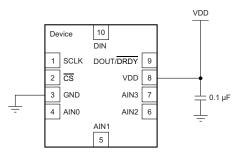


Figure 54. Power Supply Decoupling



13 Layout

13.1 Layout Guidelines

TI recommends employing best design practices when laying out a printed-circuit-board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 55. Although Figure 55 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

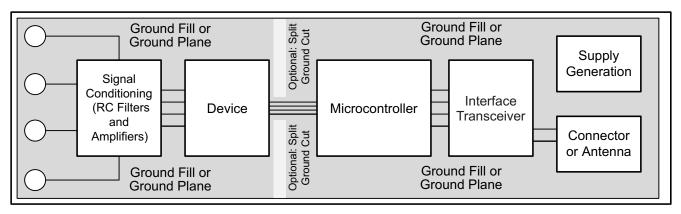


Figure 55. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the device as possible. A two-layer board is possible using common grounds for both analog and digital grounds. Additional layers can be added to simplify PCB trace routing. Ground fill may also reduce EMI and RFI issues.

TI also strongly recommends that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

Supply pins must be bypassed to ground with a low-ESR ceramic capacitor. The optimum placement of the bypass capacitors is as close as possible to the supply pins. The ground-side connections of the bypass capacitors must be low-impedance connections for optimum performance. The supply current flows through the bypass capacitor terminal first and then to the supply pin to make the bypassing most effective.

Analog inputs with differential connections must have a capacitor placed differentially across the inputs. The differential capacitors must be of high quality. The best ceramic chip capacitors are COG (NPO), which have stable properties and low noise characteristics. Thermally isolate a copper region around the thermocouple input connections to create a thermally-stable cold junction. Obtaining acceptable performance with alternate layout schemes is possible as long as the above guidelines are followed.



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13.2 Layout Example

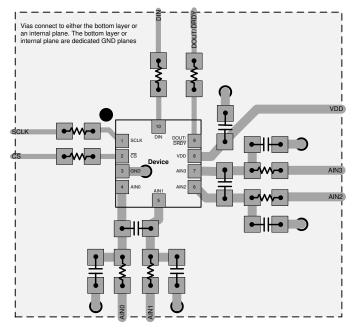


Figure 56. X2QFN Package

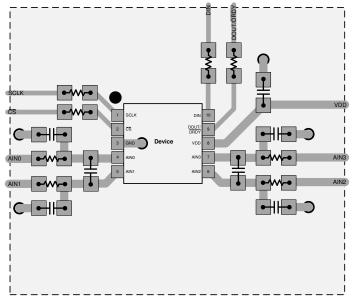


Figure 57. VSSOP Package

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14 デバイスおよびドキュメントのサポート

14.1 ドキュメントのサポート

14.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『Precision Thermocouple Measurement with the ADS1118』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『ADS1118EVM User Guide and Software Tutorial』ユーザー・ガイド(英語)
- テキサス・インスツルメンツ、『430BOOST-ADS1118 Booster Pack』ユーザー・ガイド(英語)
- テキサス・インスツルメンツ、『ADS1118 Boosterpack quick start』(英語)
- テキサス・インスツルメンツ、『A Glossary of Analog-to-Digital Specifications and Performance Characteristics』ア プリケーション・レポート(英語)

14.2 ドキュメントの更新通知を受け取る方法

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14.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

15 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable Device	Status	Package Type		Pins	-	Eco Plan	Lead finish/	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	Ball material	(3)		(4/5)	
							(6)				
ADS1118IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI	Samples
ADS1118IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI	Samples
ADS1118IRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ	Samples
ADS1118IRUGT	ACTIVE	X2QFN	RUG	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ADS1118 :

• Automotive : ADS1118-Q1

NOTE: Qualified Version Definitions:

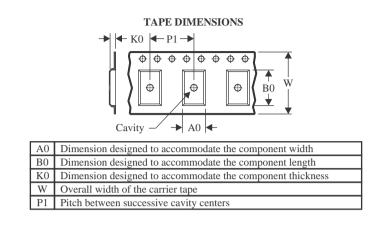
• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



TAPE AND REEL INFORMATION



*All dimensions are nominal



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1118IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1118IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1118IRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
ADS1118IRUGT	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1



PACKAGE MATERIALS INFORMATION

10-Oct-2024



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1118IDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
ADS1118IDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
ADS1118IRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
ADS1118IRUGT	X2QFN	RUG	10	250	210.0	185.0	35.0

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187, variation BA.



DGS0010A

EXAMPLE BOARD LAYOUT

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



DGS0010A

EXAMPLE STENCIL DESIGN

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

9. Board assembly site may have different recommendations for stencil design.



^{8.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

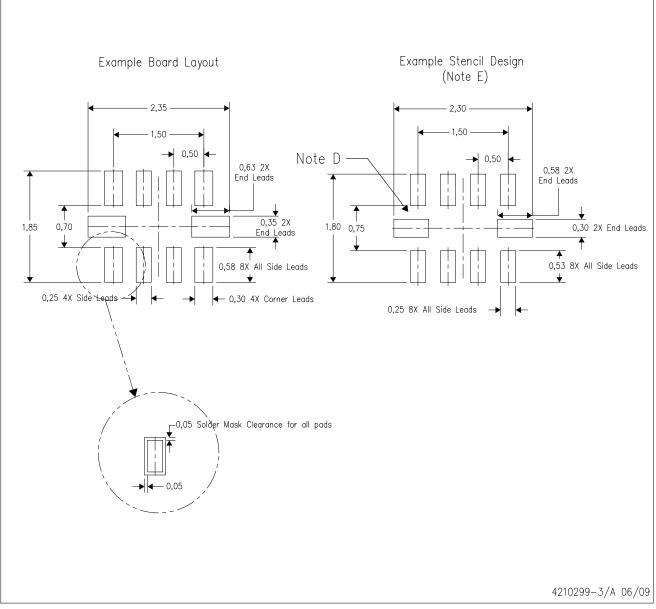
MECHANICAL DATA



B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO-288 variation X2EFD.



RUG (R-PQFP-N10)



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



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