

# ADC3908Dx および ADC3908Sx 8 ビット、25~125MSPS 低レイテンシ、低消費電力、小型、シングルおよびデュアルチャンネル ADC、入力バッファ内蔵

## 1 特長

- 最大 125MSPS のサンプリング レート
- レイテンシ: 1 クロック サイクル
- 低消費電力 (2 チャンネル):
  - 125MSPS で 90mW
  - 25MSPS で 56mW
  - PD モードで 3mW
- 小さい占有面積: 32-VQFN (4mm x 4mm)
- シングルまたはデュアル チャンネル ADC
- 内部基準電圧
- ミッシング コードなし、 $\pm 0.25$  LSB INL
- バッファ付き、差動、またはシングル エンド入力
- 入力帯域幅: 150MHz (3dB)
- 1.8V 単一電源
  - オプションの 3.3V<sub>IO</sub> 機能
- 産業用温度範囲: -40°C ~ 105°C
- パラレル (SDR、DDR) CMOS インターフェイス
- スペクトル性能 (FS<sub>CLK</sub> = 125MSPS、f<sub>IN</sub> = 5MHz):
  - 信号対雑音比: 49.8dBFS
  - SFDR: 60dBFS

## 2 アプリケーション

- 低レイテンシ制御ループ
- レーザー スキャナ
- 変位センサ
- 検出機器

## 3 概要

ADC3908Dx および ADC3908Sx は、超低消費電力、8 ビット、125MSPS の高速デュアルおよびシングル チャンネル A/D コンバータ ファミリです。待ち時間 (レイテンシ) がわずか 1 クロック サイクルと短いため、高速な制御ループを実現できます。ADC の消費電力はわずか 90mW (125MSPS 時) であり、サンプリング レートを下げることによって、消費電力を低減できます。

ADC3908Dx および ADC3908Sx は、パラレル DDR または SDR CMOS インターフェイスを使用してデータを出力します。また、+1.8V または +3.3V で駆動可能で、さまざまなレシーバ要件に対応できます。アナログ入出力インターフェイスは、ピン制御 (インターフェイス構成表) を使用して簡単に構成できます。本デバイスは、8 ビットと 10 ビットの分解能と各種速度グレードがそろったピン互換の ADC ファミリです。このデバイスは 32 ピンの VQFN パッケージで供給され、-40 ~ +105°C の工業用温度範囲に対応します。

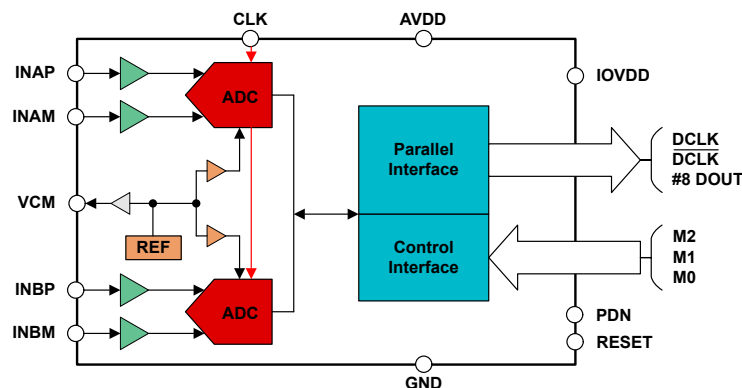
### パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
ADC3908D025, 'D06 5, 'D125 ADC3908S025, 'S06 5, 'S125	VQFN (32)	4mm x 4mm

- 詳細については、[セクション 11](#) を参照してください。
- パッケージ サイズ (長さ x 幅) は公称値であり、該当する場合はピンも含まれます。

### 製品情報

型番 (c = #CH; sss = MSPS)	分解能	サンプリング レート (MSPS)
ADC3910csss	10 ビット	25, 65, 125
ADC3908csss	8 ビット	25, 65, 125



ブロック図



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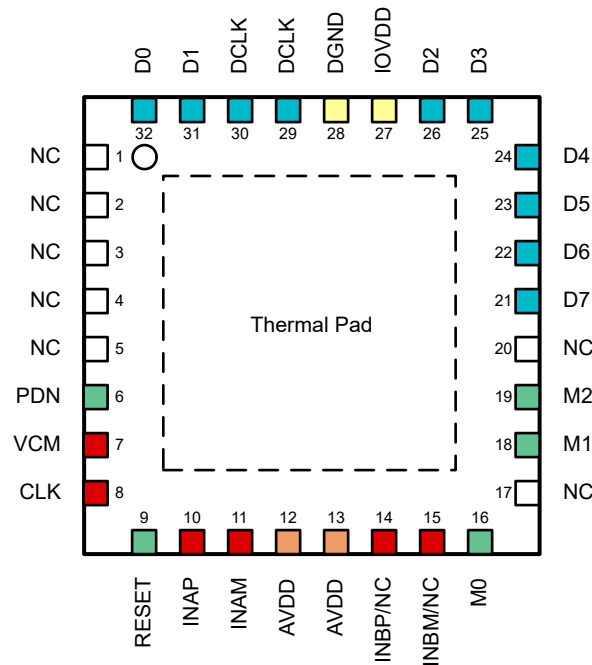
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## 4 Device Comparison

表 4-1. Device Comparison Table

Device	Resolution (Bits)	Channels	Sample Rate (MSPS)	Control Interface	Digital Features
ADC3910D125	10	2	125	SPI Control	Full Features
ADC3910S125	10	1	125	SPI Control	Full Features
ADC3910D065	10	2	65	SPI Control	Full Features
ADC3910S065	10	1	65	SPI Control	Full Features
ADC3910D025	10	2	25	SPI Control	Full Features
ADC3910S025	10	1	25	SPI Control	Full Features
ADC3908D125	8	2	125	Pin Control	Not available
ADC3908S125	8	1	125	Pin Control	Not available
ADC3908D065	8	2	65	Pin Control	Not available
ADC3908S065	8	1	65	Pin Control	Not available
ADC3908D025	8	2	25	Pin Control	Not available
ADC3908S025	8	1	25	Pin Control	Not available

## 5 Pin Configuration and Functions



A. AGND is soldered to the thermal pad

図 5-1. RSM (VQFN) Package, 32-Pin (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
<b>INPUT or REFERENCE</b>			
INAP	10	I	Positive analog input, channel A
INAM	11	I	Negative analog input, channel A
INBP/NC	14	I	Positive analog input, channel B (NC on single channel device)
INBM/NC	15	I	Negative analog input, channel B (NC on single channel device)
VCM	7	O	Common-mode voltage output for the analog inputs, 1.25 V
<b>CLOCK</b>			
CLK	8	I	Sampling clock input for the ADC
<b>CONFIGURATION</b>			
RESET	9	I	Hardware reset. Active high. This pin has an internal 60 kΩ pull-down resistor.
M0	16	I	Default, internal 40 kΩ pull-down resistor. Tie to GND for dual channel devices or AVDD for single channel devices. This pin is used to configure default operating conditions. <a href="#">Interface configuration table</a>
M1	18	I	Default, internal 40 kΩ pull-down resistor. This pin is used to configure default operating conditions. <a href="#">Interface configuration table</a>
M2	19	I	Default, internal 40 kΩ pull-down resistor. This pin is used to configure default operating conditions. <a href="#">Interface configuration table</a>
<b>DIGITAL INTERFACE</b>			

表 5-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
D0	32	O	Parallel CMOS digital lane output data.
D1	31	O	
D2	26	O	
D3	25	O	
D4	24	O	
D5	23	O	
D6	22	O	
D7	21	O	
DCLK	30	O	CMOS output for data bit clock.
DCLK	29	O	Inverse data bit clock for CMOS output data.
PDN	6	I	Default, pin has 60 kΩ pull-down. When PDN is pulled high device is put in a powerdown state.
<b>POWER SUPPLY</b>			
AVDD	12, 13	I	Analog 1.8 V power supply
GND	PowerPAD™	I	Analog Ground, 0 V
IOVDD	27	I	1.8 V power supply for digital interface
DGND	5, 28	I	Ground, 0 V for digital interface
<b>OTHER</b>			
NC	1, 2, 3, 4, 5, 17, 20	-	No connection. Connect to ground.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range 1.8 V, AVDD		-0.3	2.1	V
Supply voltage range 1.8 V to 3.3 V, IOVDD		-0.3	3.6	
Supply voltage range, GND, DGND		-0.3	0.3	
Voltage applied to input pins	INAP/M, INBP/M, CLK	-0.3	2.1	
	RESET, PDN, M0, M1, M2	-0.3	2.1	
Junction temperature, T <sub>J</sub>			125	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage range	Supply voltage range 1.8v	AVDD <sup>(1)</sup>	1.7	1.8	1.9	V
Supply voltage range		IOVDD <sup>(1)</sup>	1.7	1.8	1.9	V
Supply voltage range	Supply voltage range 3.3v	IOVDD <sup>(1)</sup>	3.2	3.3	3.4	V
T <sub>A</sub>	Operating free-air temperature		-40		105	°C
T <sub>J</sub>	Operating junction temperature				115 <sup>(2)</sup>	°C

- (1) Measured to GND.  
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADC39xx	UNIT
		RSM (QFN)	
		32 Pins	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	38.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	37.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics - Power Consumption

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $F_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$ , Internal 1.2 V reference, 5 pF output load, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ADC3908D025</b>						
$I_{AVDD}$	Analog supply current	$F_s = 25\text{ MSPS}$ , dual channel, DDR CMOS		28	31	mA
$I_{IOVDD}$	Digital supply current			3	9	mA
$P_{DIS}$	Power dissipation			56		mW
<b>ADC3908S025</b>						
$I_{AVDD}$	Analog supply current	$F_s = 25\text{ MSPS}$ , single channel, SDR CMOS		19	22	mA
$I_{IOVDD}$	Digital supply current			3	8	mA
$P_{DIS}$	Power dissipation			40		mW
<b>ADC3908D065</b>						
$I_{AVDD}$	Analog supply current	$F_s = 65\text{ MSPS}$ , dual channel, DDR CMOS		32	34	mA
$I_{IOVDD}$	Digital supply current			7	14	mA
$P_{DIS}$	Power dissipation			70		mW
<b>ADC3908S065</b>						
$I_{AVDD}$	Analog supply current	$F_s = 65\text{ MSPS}$ , single channel, SDR CMOS		21	24	mA
$I_{IOVDD}$	Digital supply current			6	13	mA
$P_{DIS}$	Power dissipation			49		mW
<b>ADC3908D125</b>						
$I_{AVDD}$	Analog supply current	$F_s = 125\text{ MSPS}$ , dual channel, DDR CMOS		38	40	mA
$I_{IOVDD}$	Digital supply current			12	21	mA
$P_{DIS}$	Power dissipation			90		mW
<b>ADC3908S125</b>						
$I_{AVDD}$	Analog supply current	$F_s = 125\text{ MSPS}$ , single channel, SDR CMOS		24	27	mA
$I_{IOVDD}$	Digital supply current			10	18	mA
$P_{DIS}$	Power dissipation			61		mW
<b>Power down</b>						
$P_{DIS}$	Power consumption in power down			3		mW

## 6.6 Electrical Characteristics - DC Specifications

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ , 50% clock duty cycle,  $AVDD = IOVDD = 1.8\text{ V}$ , Internal 1.2 V reference, and  $-1\text{ dBFS}$  differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC ACCURACY (25 MSPS)</b>						
No missing codes			8			bits
DNL	Differential nonlinearity		-0.35	$\pm 0.15$	+0.35	LSB
INL	Integral nonlinearity		-0.6	$\pm 0.25$	+0.6	LSB
$V_{OS\_ERR}$	Offset error		-2.75	$\pm 1$	+2.75	LSB
$V_{OS\_DRIFT}$	Offset drift over temperature			0.001		LSB/ $^\circ\text{C}$
$GAIN_{ERR}$	Gain error	Internal Reference		$\pm 0.8$		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	Internal Reference		-102		ppm/ $^\circ\text{C}$
<b>DC ACCURACY (65 MSPS)</b>						
No missing codes			8			bits

## 6.6 Electrical Characteristics - DC Specifications (続き)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ , 50% clock duty cycle,  $AVDD = IOVDD = 1.8\text{ V}$ , Internal 1.2 V reference, and  $-1\text{-dBFS}$  differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DNL	Differential nonlinearity		-0.35	$\pm 0.15$	+0.35	LSB
INL	Integral nonlinearity		-0.6	$\pm 0.25$	+0.6	LSB
$V_{OS\_ERR}$	Offset error		-2.75	$\pm 1$	-2.75	LSB
$V_{OS\_DRIFT}$	Offset drift over temperature			0.001		LSB/ $^\circ\text{C}$
$GAIN_{ERR}$	Gain error	Internal Reference		$\pm 0.8$		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	Internal Reference		-102		ppm/ $^\circ\text{C}$
<b>DC ACCURACY (125 MSPS)</b>						
No missing codes			8			bits
DNL	Differential nonlinearity		-0.35	$\pm 0.15$	+0.35	LSB
INL	Integral nonlinearity		-0.6	$\pm 0.25$	+0.6	LSB
$V_{OS\_ERR}$	Offset error		-2.75	$\pm 1$	2.75	LSB
$V_{OS\_DRIFT}$	Offset drift over temperature			0.001		LSB/ $^\circ\text{C}$
$GAIN_{ERR}$	Gain error	Internal Reference		$\pm 0.8$		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	Internal Reference		-102		ppm/ $^\circ\text{C}$
<b>ADC ANALOG INPUT (INAP/M, INBP/M)</b>						
FS	Input full scale	Differential	1.9			V <sub>pp</sub>
		Single-ended	0.95			V <sub>pp</sub>
$C_{IN}$	Differential input Capacitance	$F_{IN} = 100\text{ kHz}$	7			pF
$V_{CM}$	Input common mode voltage		$V_{OCM} - 50\text{mV}$	1.275	$V_{OCM} + 50\text{mV}$	V
$V_{OCM}$	Output common mode voltage		1.25			V
BW	Analog Input Bandwidth (-3dB)		150			MHz
<b>CLOCK INPUT</b>						
Input clock frequency	ADC3908D125, ADC3908S125		5		125	MHz
	ADC3908D065, ADC3908S065		5		65	MHz
	ADC3908D025, ADC3908S025		5		25	MHz
$V_{IH}$	High level input voltage		$AVDD - 0.3$	1.8		V <sub>pp</sub>
$V_{IL}$	Low level input voltage			0	$AVSS + 0.3$	V
$C_{IN}$	Input capacitance		0.5			pF
Clock duty cycle			45	50	55	%
<b>DIGITAL INPUTS (RESET, PDN, M0, M1, M2)</b>						
$V_{IH}$	High level input voltage		1.4			V
$V_{IL}$	Low level input voltage				0.4	V
$I_{IH}$	High level input current		90		150	$\mu\text{A}$
$I_{IL}$	Low level input current		-150	-90		$\mu\text{A}$
$C_i$	Input capacitance		1.5			pF
<b>DIGITAL CMOS OUTPUTS (D0:D07)</b>						
Output data rate		per CMOS output pin			250	Mbps
$V_{OH}$	High level output voltage	$I_{LOAD} = -400\text{ uA}$	$IOVDD - 0.1$	$IOVDD$		V

## 6.6 Electrical Characteristics - DC Specifications (続き)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ , 50% clock duty cycle,  $AVDD = IOVDD = 1.8\text{ V}$ , Internal 1.2 V reference, and -1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL}$	Low level output voltage	$I_{LOAD} = 400\ \mu\text{A}$			0.1	V



## 6.7 Electrical Characteristics - AC Specifications (25 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $FS_{CLK} = 25\text{ MSPS}$ ,  $F_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$ , Internal 1.2 V reference, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	$f_{IN} = 10\text{ MHz}$ , $A_{IN} = -20\text{ dBFS}$		-120.8		dBFS/Hz
SNR	Signal to noise ratio, excluding DC, HD2 to HD5	$f_{IN} = 1.1\text{ MHz}$		49.9		dBFS
		$f_{IN} = 5\text{ MHz}$	48	49.9		
		$f_{IN} = 10\text{ MHz}$		49.9		
		$f_{IN} = 20\text{ MHz}$		49.9		
SINAD	Signal to noise and distortion ratio, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		49.6		dBFS
		$f_{IN} = 5\text{ MHz}$		49.7		
		$f_{IN} = 10\text{ MHz}$		49.7		
		$f_{IN} = 20\text{ MHz}$		49.7		
ENOB	Effective number of bits, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		8.0		Bit
		$f_{IN} = 5\text{ MHz}$		8.0		
		$f_{IN} = 10\text{ MHz}$		8.0		
		$f_{IN} = 20\text{ MHz}$		8.0		
THD	Total Harmonic Distortion (First five harmonics)	$f_{IN} = 1.1\text{ MHz}$		-61		dBc
		$f_{IN} = 5\text{ MHz}$		-63		
		$f_{IN} = 10\text{ MHz}$		-63		
		$f_{IN} = 20\text{ MHz}$		-64		
SFDR	Spur free dynamic range including second and third harmonic	$f_{IN} = 1.1\text{ MHz}$		63		dBFS
		$f_{IN} = 5\text{ MHz}$	60	65		
		$f_{IN} = 10\text{ MHz}$		64		
		$f_{IN} = 20\text{ MHz}$		64		
SPUR	Spur free dynamic range (excluding DC, HD2, HD3)	$f_{IN} = 1.1\text{ MHz}$		67		dBFS
		$f_{IN} = 5\text{ MHz}$	63	68		
		$f_{IN} = 10\text{ MHz}$		68		
		$f_{IN} = 20\text{ MHz}$		68		
IMD3	Two tone inter-modulation distortion	$f_{IN} = 8/10\text{ MHz}$ , $A_{IN} = -7\text{ dBFS/tone}$		-91		dBc
XTALK	Channel-to-channel crosstalk	Aggressor = 1.1 MHz		107		dBFS
		Aggressor = 10 MHz		97		
		Aggressor = 20 MHz		93		

## 6.8 Electrical Characteristics - AC Specifications (65 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $FS_{CLK} = 65\text{ MSPS}$ ,  $F_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$ , Internal 1.2 V reference, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	$f_{IN} = 10\text{ MHz}$ , $A_{IN} = -20\text{ dBFS}$		-125.0		dBFS/Hz
SNR	Signal to noise ratio, excluding DC, HD2 to HD5	$f_{IN} = 1.1\text{ MHz}$		49.8		dBFS
		$f_{IN} = 5\text{ MHz}$	47	49.8		
		$f_{IN} = 10\text{ MHz}$		49.8		
		$f_{IN} = 20\text{ MHz}$		49.8		
		$f_{IN} = 40\text{ MHz}$		49.8		
		$f_{IN} = 70\text{ MHz}$		49.8		
SINAD	Signal to noise and distortion ratio, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		49.6		dBFS
		$f_{IN} = 5\text{ MHz}$		49.7		
		$f_{IN} = 10\text{ MHz}$		49.7		
		$f_{IN} = 20\text{ MHz}$		49.7		
		$f_{IN} = 40\text{ MHz}$		49.6		
		$f_{IN} = 70\text{ MHz}$		49.6		
ENOB	Effective number of bits, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		8.0		Bit
		$f_{IN} = 5\text{ MHz}$		8.0		
		$f_{IN} = 10\text{ MHz}$		8.0		
		$f_{IN} = 20\text{ MHz}$		8.0		
		$f_{IN} = 40\text{ MHz}$		8.0		
		$f_{IN} = 70\text{ MHz}$		8.0		
THD	Total Harmonic Distortion (First five harmonics)	$f_{IN} = 1.1\text{ MHz}$		-61		dBc
		$f_{IN} = 5\text{ MHz}$		-63		
		$f_{IN} = 10\text{ MHz}$		-63		
		$f_{IN} = 20\text{ MHz}$		-64		
		$f_{IN} = 40\text{ MHz}$		-62		
		$f_{IN} = 70\text{ MHz}$		-61		
SFDR	Spur free dynamic range including second and third harmonic	$f_{IN} = 1.1\text{ MHz}$		62		dBFS
		$f_{IN} = 5\text{ MHz}$	60	64		
		$f_{IN} = 10\text{ MHz}$		64		
		$f_{IN} = 20\text{ MHz}$		65		
		$f_{IN} = 40\text{ MHz}$		63		
		$f_{IN} = 70\text{ MHz}$		62		
SPUR	Spur free dynamic range (excluding DC, HD2, HD3)	$f_{IN} = 1.1\text{ MHz}$		68		dBFS
		$f_{IN} = 5\text{ MHz}$	61	68		
		$f_{IN} = 10\text{ MHz}$		68		
		$f_{IN} = 20\text{ MHz}$		68		
		$f_{IN} = 40\text{ MHz}$		68		
		$f_{IN} = 70\text{ MHz}$		68		
IMD3	Two tone inter-modulation distortion	$f_{IN} = 8/10\text{ MHz}$ , $A_{IN} = -7\text{ dBFS/ tone}$		-91		dBc
XTALK	Channel-to-channel crosstalk	Aggressor = 1.1 MHz		106		dBFS
		Aggressor = 10 MHz		102		
		Aggressor = 20 MHz		97		

## 6.9 Electrical Characteristics - AC Specifications (125 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $FS_{CLK} = 125\text{ MSPS}$ ,  $f_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$ , Internal 1.2 V reference, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	$f_{IN} = 10\text{ MHz}$ , $A_{IN} = -20\text{ dBFS}$		-127.8		dBFS/Hz
SNR	Signal to noise ratio, excluding DC, HD2 to HD5	$f_{IN} = 1.1\text{ MHz}$		49.8		dBFS
		$f_{IN} = 5\text{ MHz}$	48	49.8		
		$f_{IN} = 10\text{ MHz}$		49.8		
		$f_{IN} = 20\text{ MHz}$		49.8		
		$f_{IN} = 40\text{ MHz}$		49.8		
		$f_{IN} = 70\text{ MHz}$		49.8		
SINAD	Signal to noise and distortion ratio, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		49.6		dBFS
		$f_{IN} = 5\text{ MHz}$		49.5		
		$f_{IN} = 10\text{ MHz}$		49.5		
		$f_{IN} = 20\text{ MHz}$		49.6		
		$f_{IN} = 40\text{ MHz}$		49.7		
		$f_{IN} = 70\text{ MHz}$		49.4		
ENOB	Effective number of bits, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		8.0		Bit
		$f_{IN} = 5\text{ MHz}$		8.0		
		$f_{IN} = 10\text{ MHz}$		8.0		
		$f_{IN} = 20\text{ MHz}$		8.0		
		$f_{IN} = 40\text{ MHz}$		8.0		
		$f_{IN} = 70\text{ MHz}$		8.0		
THD	Total Harmonic Distortion (First five harmonics)	$f_{IN} = 1.1\text{ MHz}$		-61		dBc
		$f_{IN} = 5\text{ MHz}$		-59		
		$f_{IN} = 10\text{ MHz}$		-60		
		$f_{IN} = 20\text{ MHz}$		-61		
		$f_{IN} = 40\text{ MHz}$		-64		
		$f_{IN} = 70\text{ MHz}$		-59		
SFDR	Spur free dynamic range including second and third harmonic	$f_{IN} = 1.1\text{ MHz}$		62		dBFS
		$f_{IN} = 5\text{ MHz}$	56	60		
		$f_{IN} = 10\text{ MHz}$		61		
		$f_{IN} = 20\text{ MHz}$		63		
		$f_{IN} = 40\text{ MHz}$		65		
		$f_{IN} = 70\text{ MHz}$		60		
SPUR	Spur free dynamic range (excluding DC, HD2, HD3)	$f_{IN} = 1.1\text{ MHz}$		68		dBFS
		$f_{IN} = 5\text{ MHz}$	61	68		
		$f_{IN} = 10\text{ MHz}$		68		
		$f_{IN} = 20\text{ MHz}$		68		
		$f_{IN} = 40\text{ MHz}$		68		
		$f_{IN} = 70\text{ MHz}$		68		
IMD3	Two tone inter-modulation distortion	$f_{IN} = 8/10\text{ MHz}$ , $A_{IN} = -7\text{ dBFS/ tone}$		-86		dBc
XTALK	Channel-to-channel crosstalk	Aggressor = 1.1 MHz		102		dBFS
		Aggressor = 10 MHz		90		
		Aggressor = 20 MHz		98		

## 6.10 Timing Requirements

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, Internal 1.2 V reference, 5 pF output load, and  $-1\text{-dBFS}$  differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
<b>ADC TIMING SPECIFICATIONS</b>						
$t_{AD}$	Aperture Delay			0.5		ns
$t_A$	Aperture Jitter	square wave clock with fast edges		250		fs
$t_{ACQ}$	Signal acquisition period, referenced to sampling clock falling edge			$-T_S/5$		Sampling Clock Period
$t_{CONV}$	Signal conversion period, referenced to sampling clock falling edge	$F_S = 25\text{ MSPS}$		5.5		ns
		$F_S = 65\text{ MSPS}$		5.5		ns
		$F_S = 125\text{ MSPS}$		5.5		ns
Wake up time	Time to valid data after coming out of power down. Internal reference.			30		us
ADC Latency	Signal input to data output	DDR		1		ADC clock cycles
		SDR		1		
<b>INTERFACE TIMING - DDR CMOS</b>						
$t_{PD}$	Propagation delay: sampling clock falling edge to DCLK rising edge			$T_S/4 + 3$		ns
$t_{DE}$	DCLK edge to previous data transition	$F_S = 25\text{ MSPS}$		-10	-9	ns
		$F_S = 65\text{ MSPS}$		-3.8	-3.4	
		$F_S = 125\text{ MSPS}$		-2	-1.8	
$t_{DL}$	DCLK edge to next data transition	$F_S = 25\text{ MSPS}$		9	10	ns
		$F_S = 65\text{ MSPS}$		3.4	3.8	
		$F_S = 125\text{ MSPS}$		1.8	2	
<b>INTERFACE TIMING - SDR CMOS</b>						
$t_{PD}$	Propagation delay: sampling clock falling edge to DCLK rising edge			$T_S/4 + 3$		ns
$t_{DE}$	DCLK edge to previous data transition	$F_S = 25\text{ MSPS}$		-20	-18	ns
		$F_S = 65\text{ MSPS}$		-7.6	-6.9	
		$F_S = 125\text{ MSPS}$		-4	-3.6	
$t_{DV}$	DCLK edge to next data transition	$F_S = 25\text{ MSPS}$		18	20	ns
		$F_S = 65\text{ MSPS}$		6.9	7.7	
		$F_S = 125\text{ MSPS}$		3.6	4	

## 6.11 Output Interface Timing Diagram

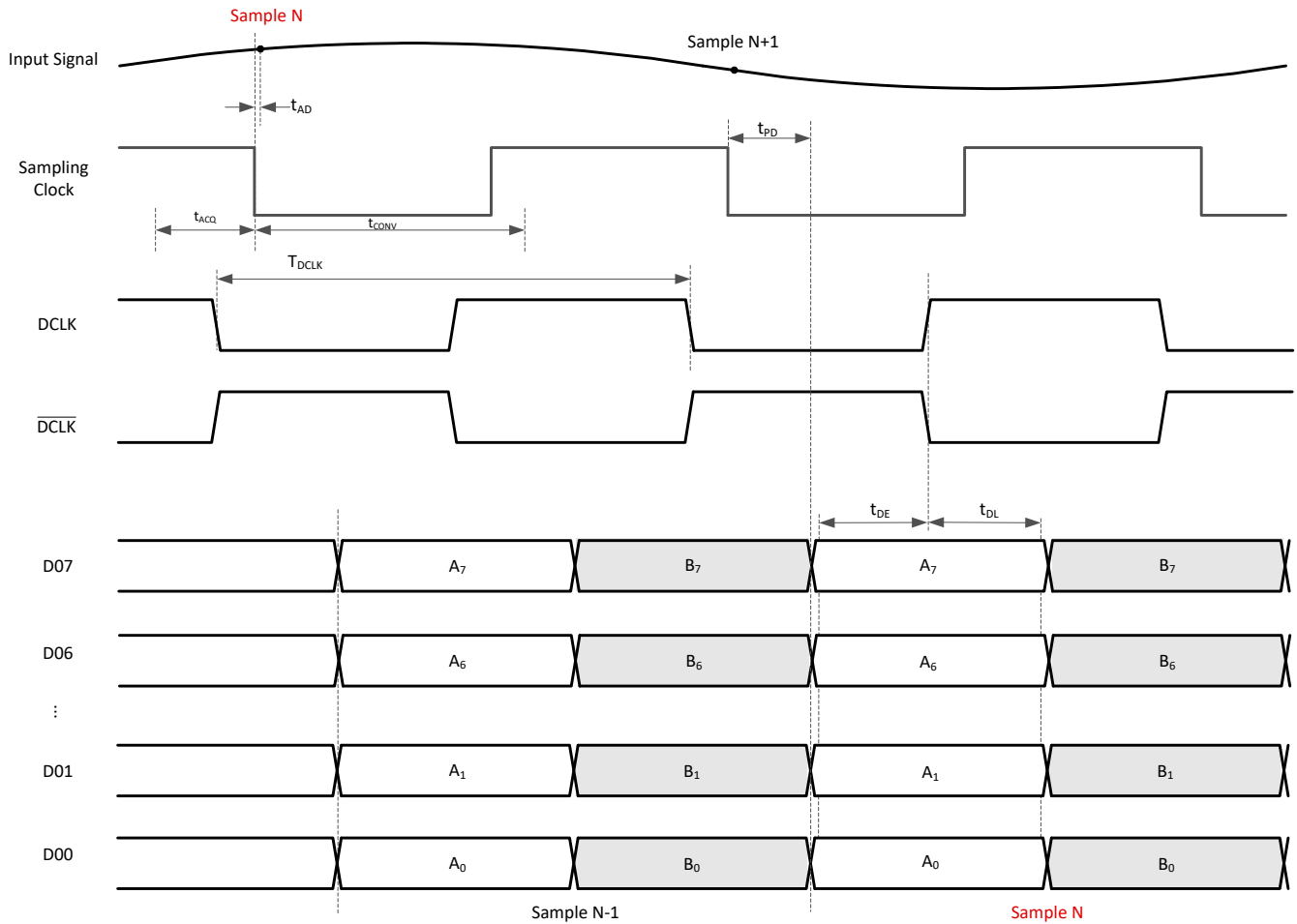


図 6-1. Timing Diagram: Dual CH, DDR (Default: 8 Lanes)

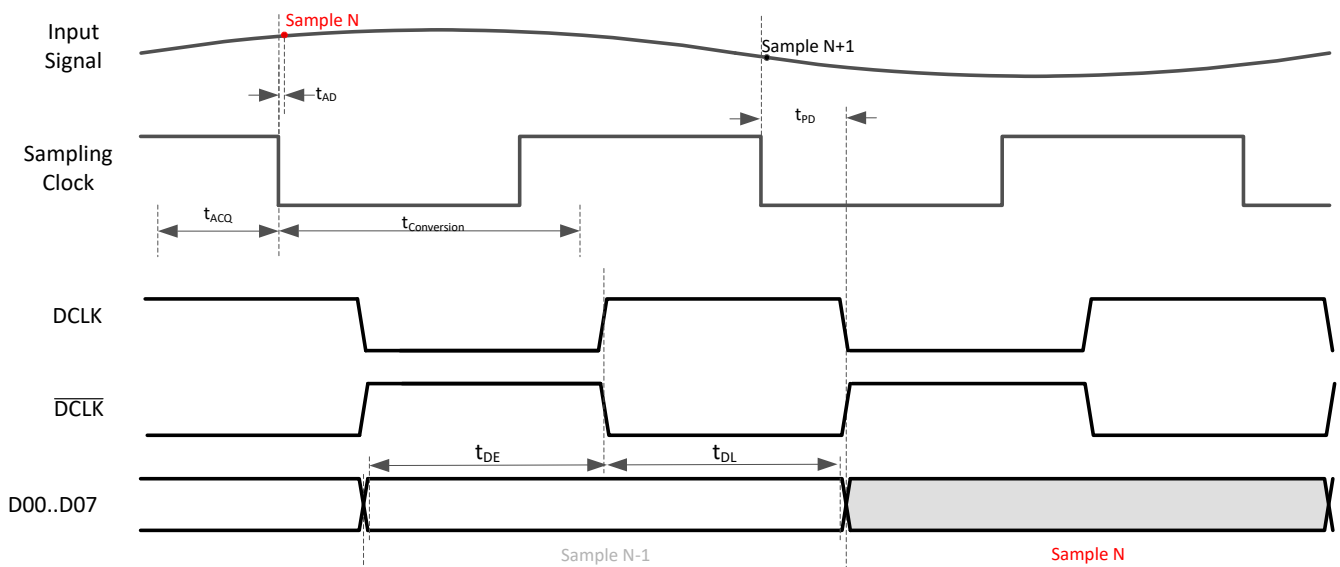
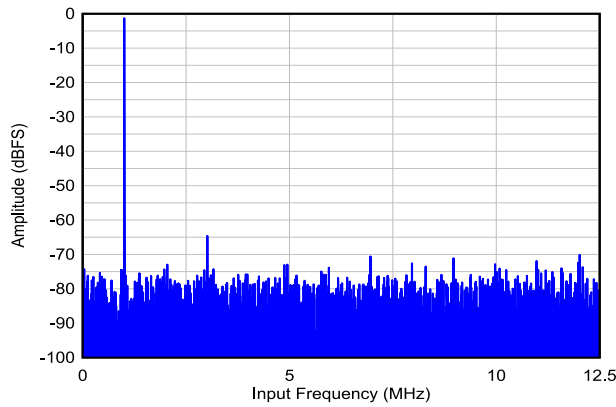


図 6-2. Timing Diagram: Single CH (CHA), SDR (Default: 8 Lanes)

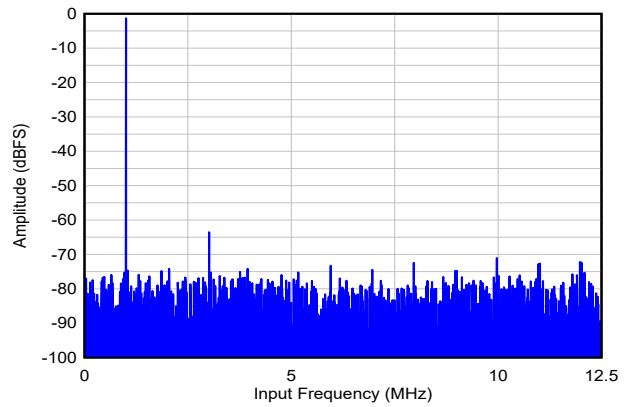
## 6.12 Typical Characteristics: 25MSPS

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



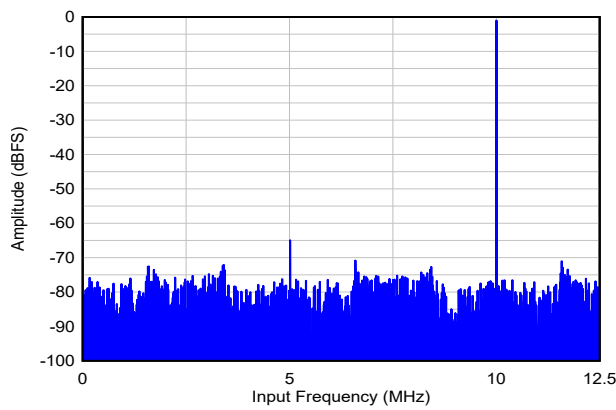
SNR = 49.8dBFS, SFDR = 63dBc, Non HD23 = 69dBFS

6-3. Single Tone FFT at  $F_{IN} = 1\text{MHz}$



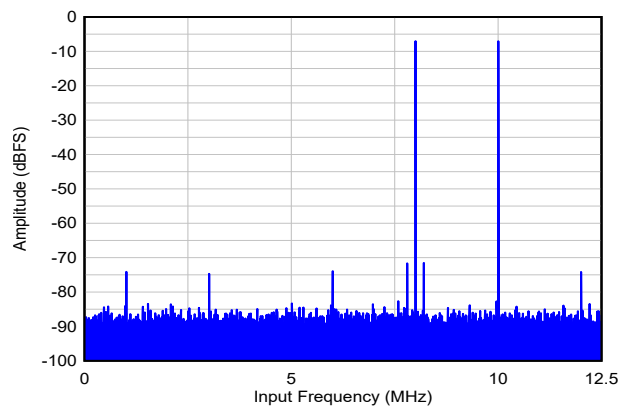
SNR = 49.7dBFS, SFDR = 62dBc, Non HD23 = 70dBFS

6-4. Single Tone FFT at  $F_{IN} = 1\text{MHz}$ , Single-ended Input



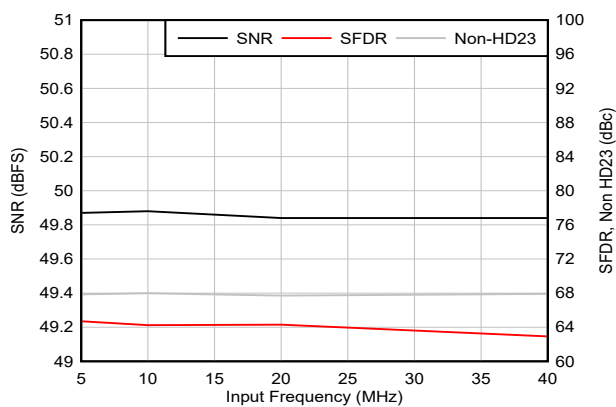
SNR = 49.7dBFS, SFDR = 64dBc, Non HD23 = 70dBFS

6-5. Single Tone FFT at  $F_{IN} = 10\text{MHz}$

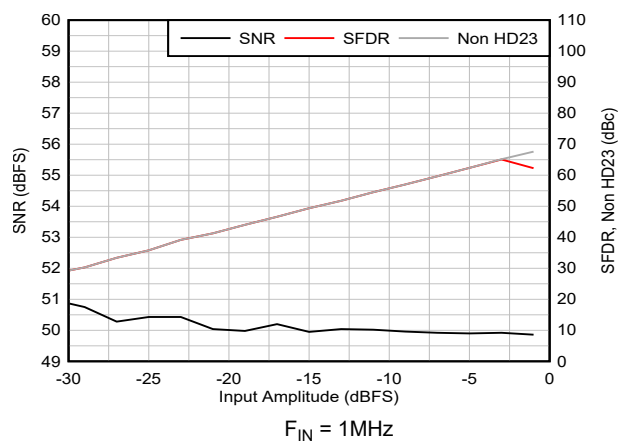


$A_{IN} = -7\text{dBFS}/\text{tone}$ ,  $\text{IMD3} = -95\text{dBc}$

6-6. Two Tone FFT at  $F_{IN} = 8/10\text{MHz}$



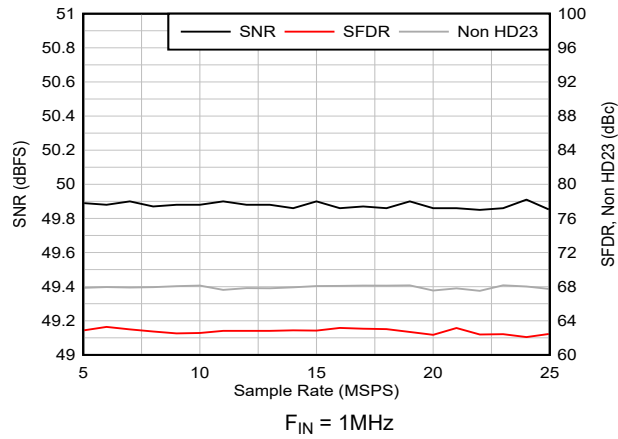
6-7. AC Performance vs Input Frequency



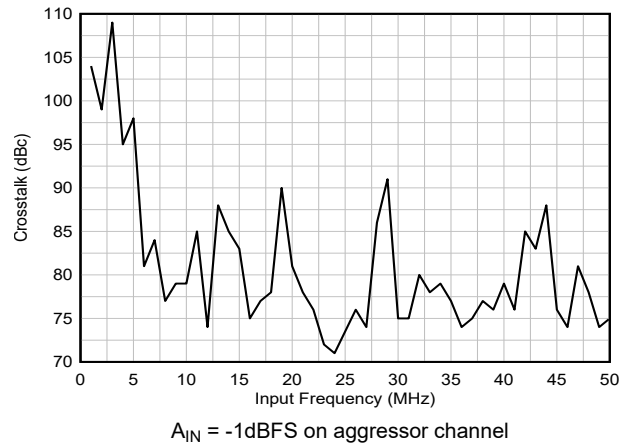
6-8. AC Performance vs Input Amplitude

## 6.12 Typical Characteristics: 25MSPS (continued)

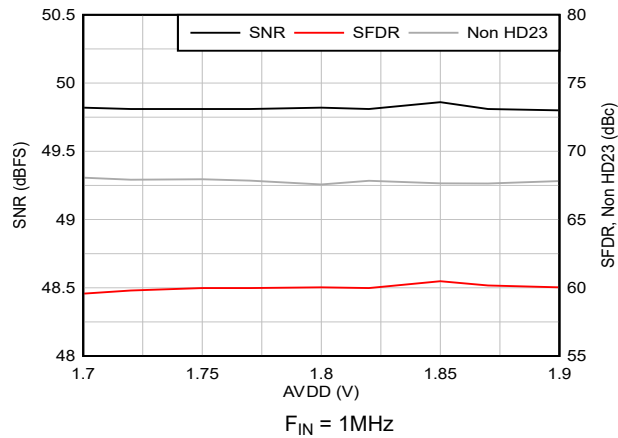
Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



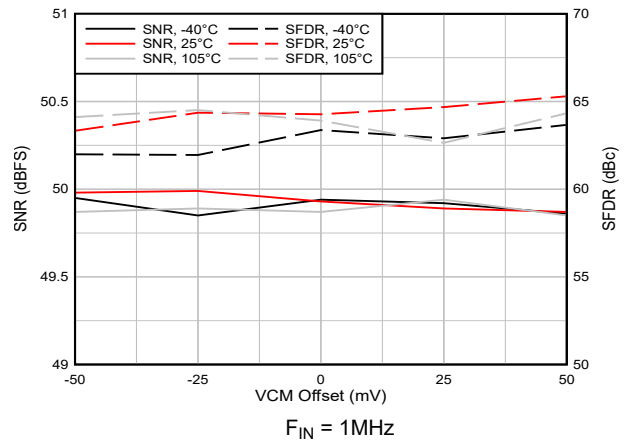
**6-9. AC Performance vs Sampling Rate**



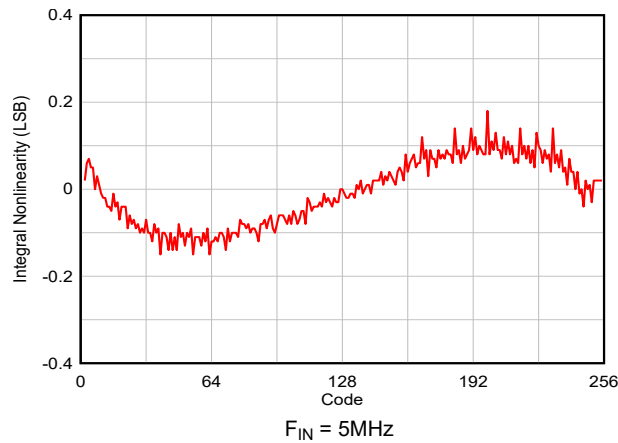
**6-10. Crosstalk vs Input Frequency**



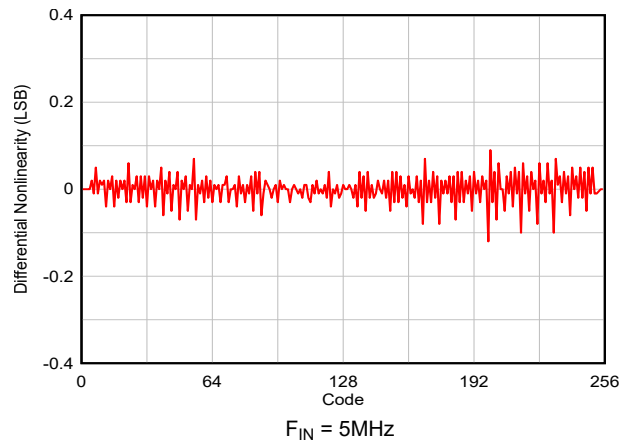
**6-11. AC Performance vs AVDD**



**6-12. AC Performance vs VCM vs Temperature**



**6-13. INL vs ADC Code**



**6-14. DNL vs ADC Code**

## 6.12 Typical Characteristics: 25MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.

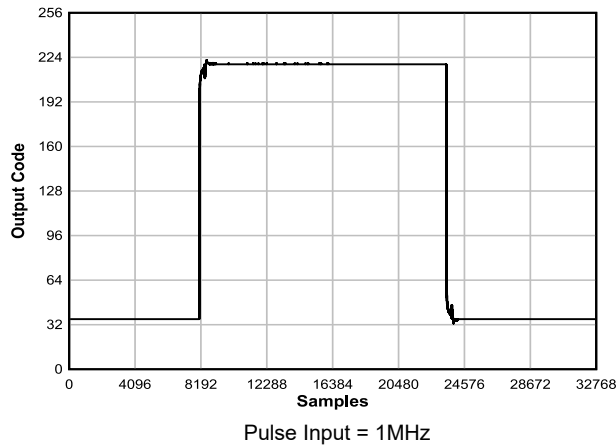


图 6-15. Pulse Response

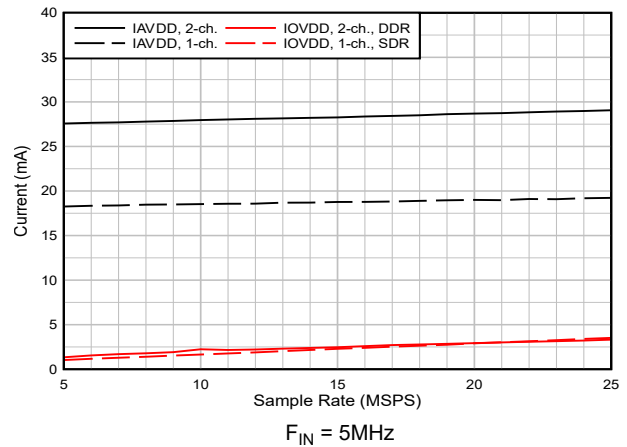


图 6-16. Current vs Sampling Rate

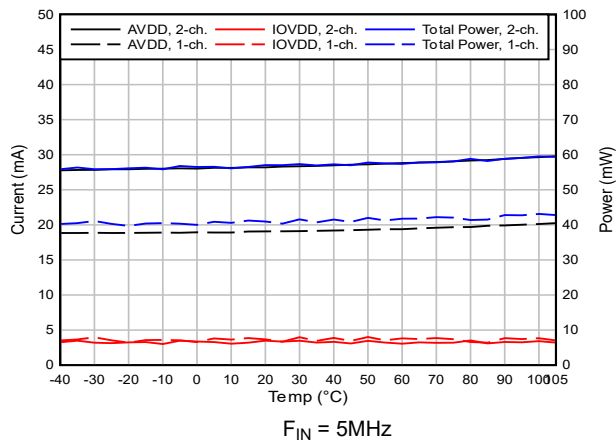


图 6-17. Current vs Temperature

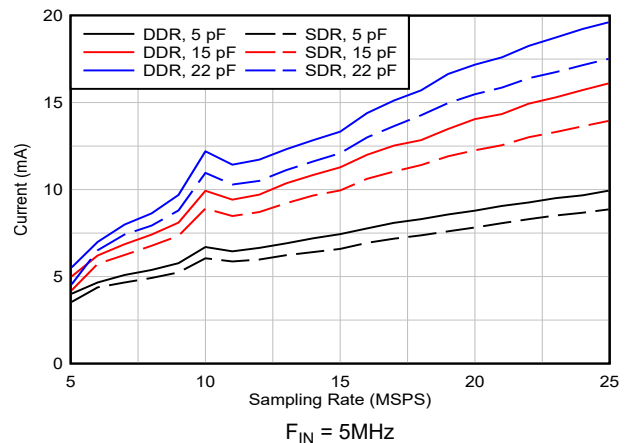
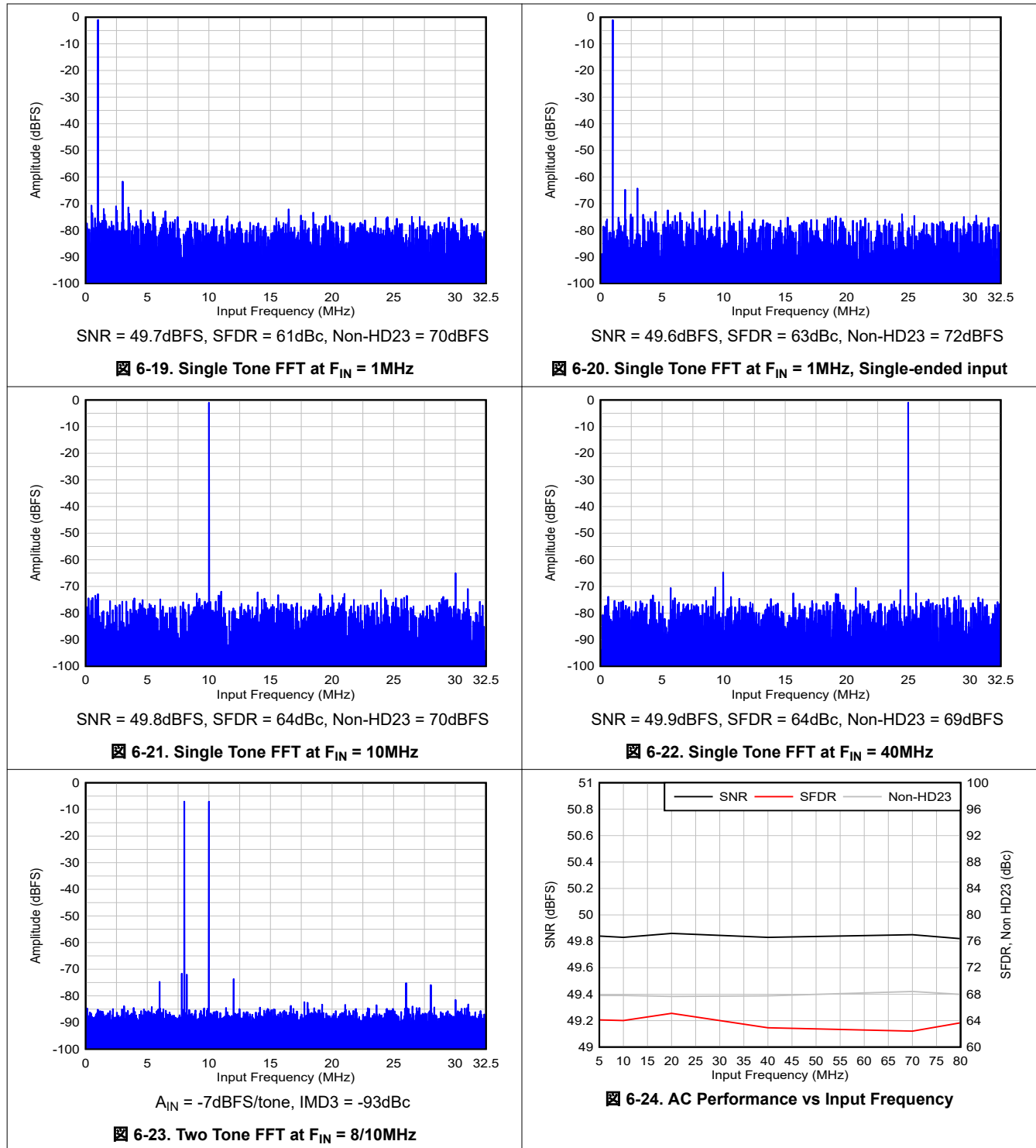


图 6-18.  $I_{IOVDD}$  Current vs Load Capacitance



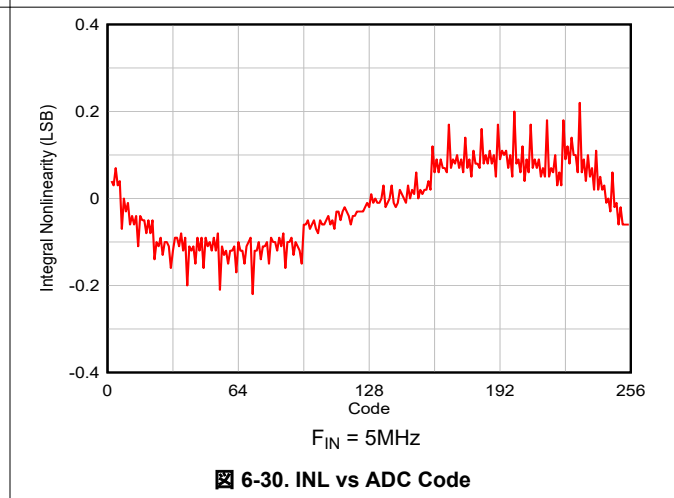
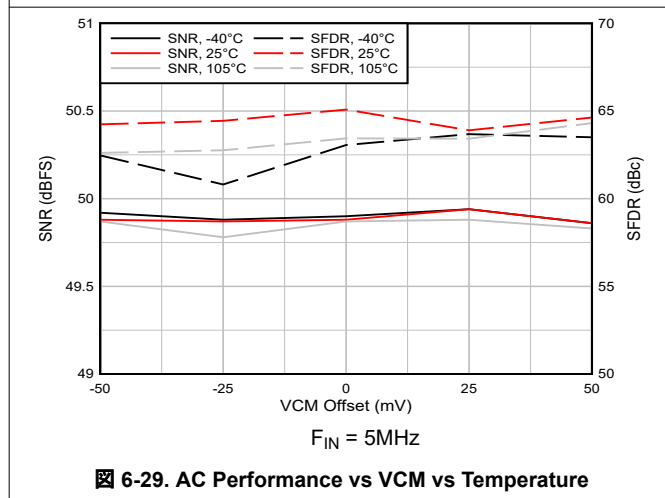
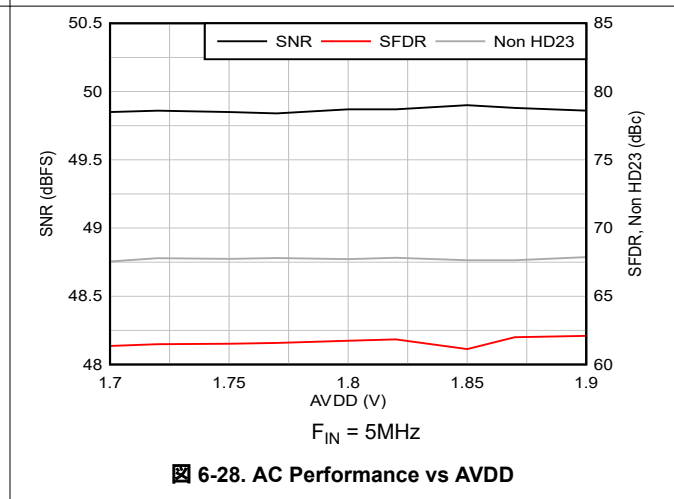
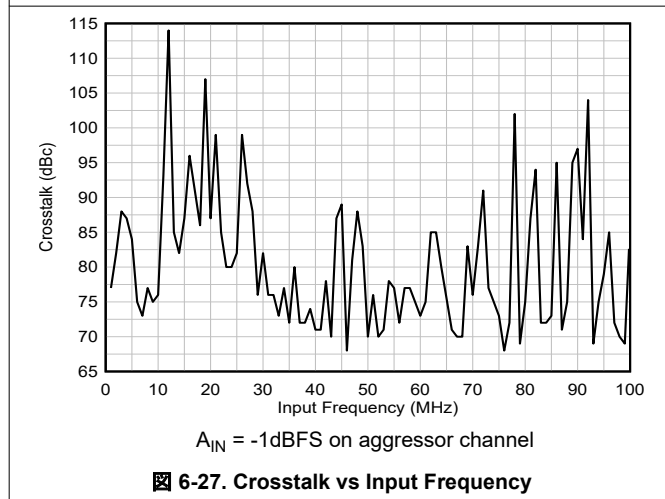
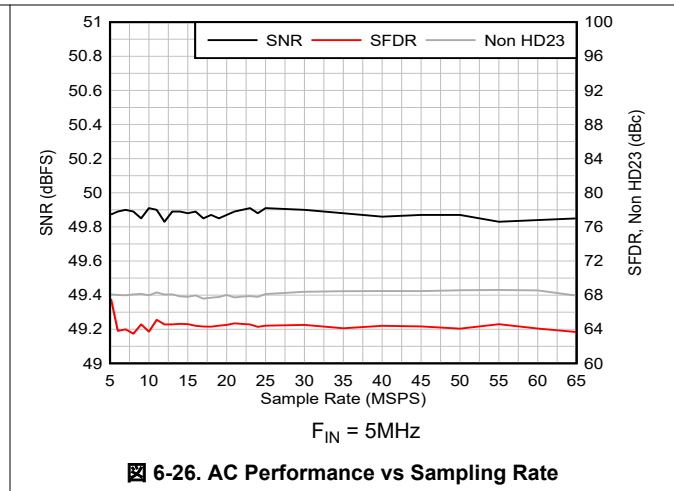
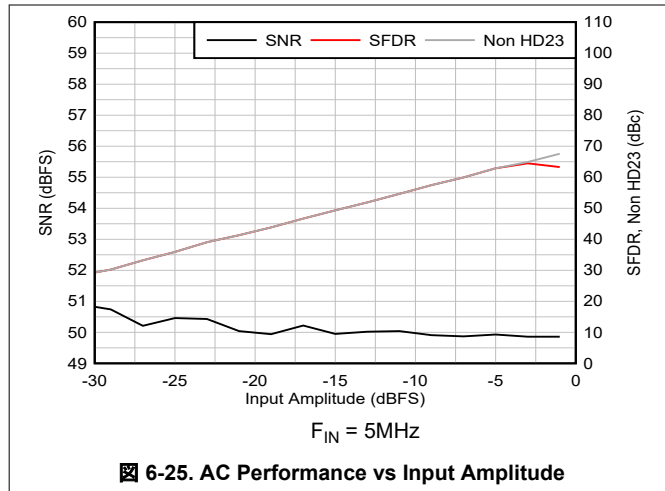
### 6.13 Typical Characteristics - 65MSPS

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 65 MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



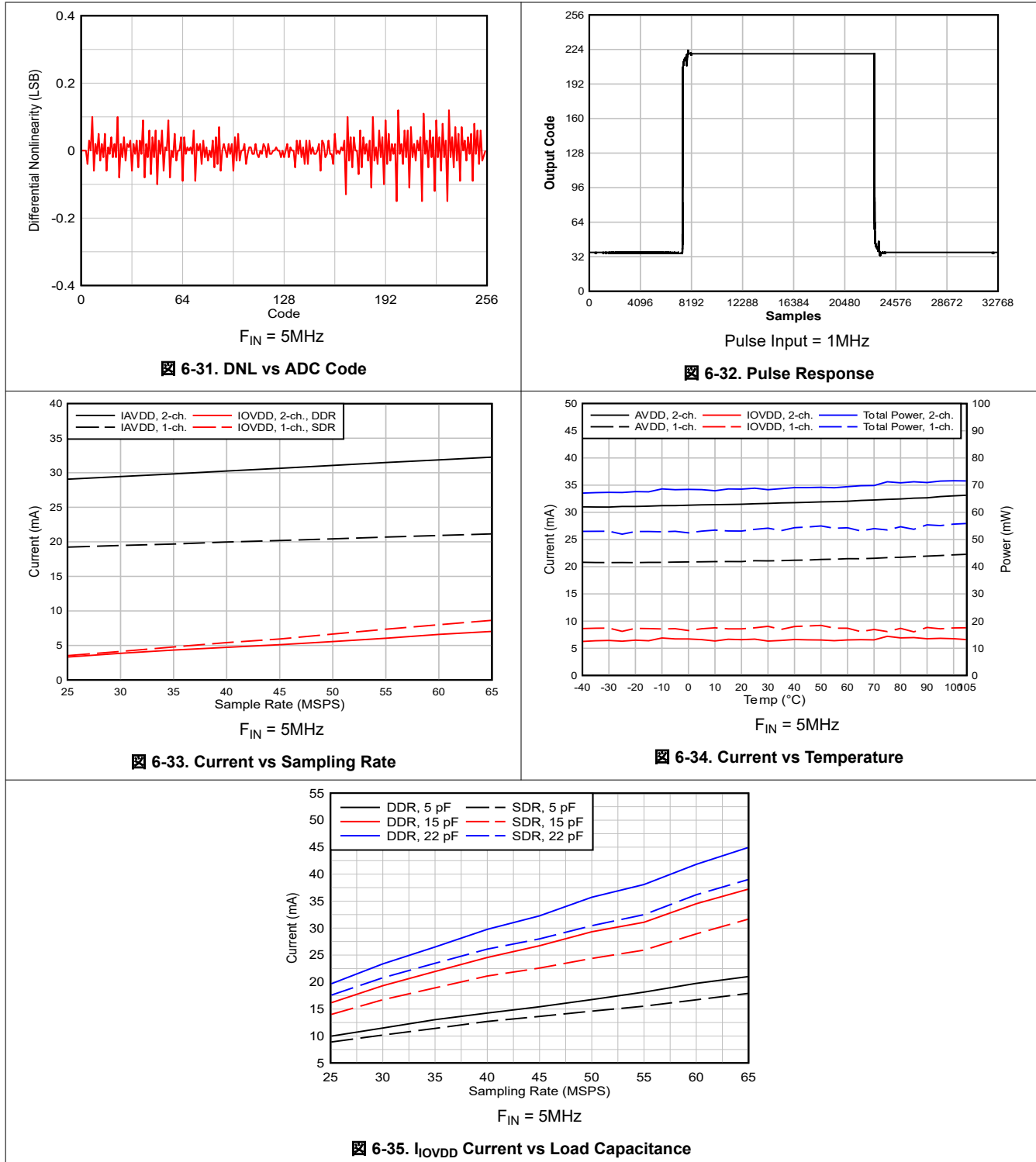
### 6.13 Typical Characteristics - 65MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 65 MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



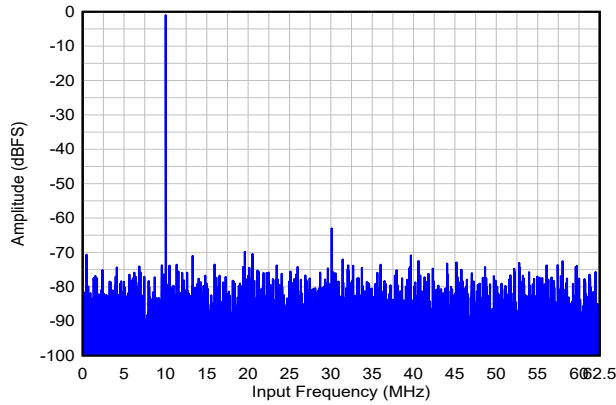
### 6.13 Typical Characteristics - 65MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 65 MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



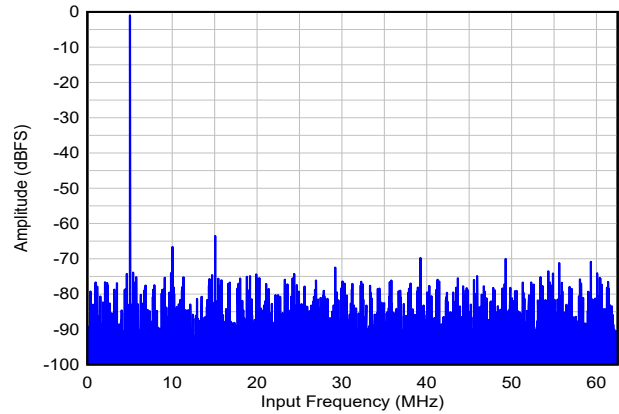
## 6.14 Typical Characteristics - 125MSPS

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



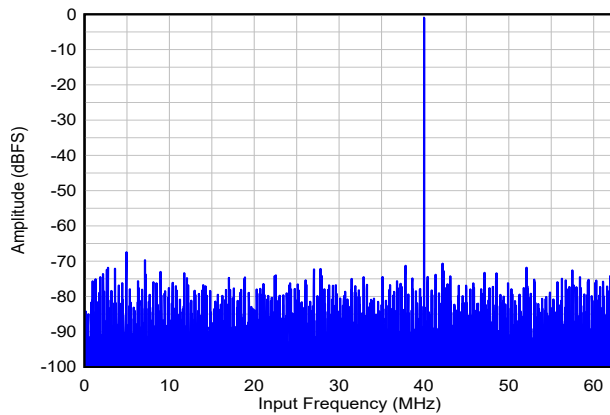
SNR = 49.8dBFS, SFDR = 62dBc, Non-HD23 = 69dBFS

6-36. Single Tone FFT at  $F_{IN} = 10\text{MHz}$



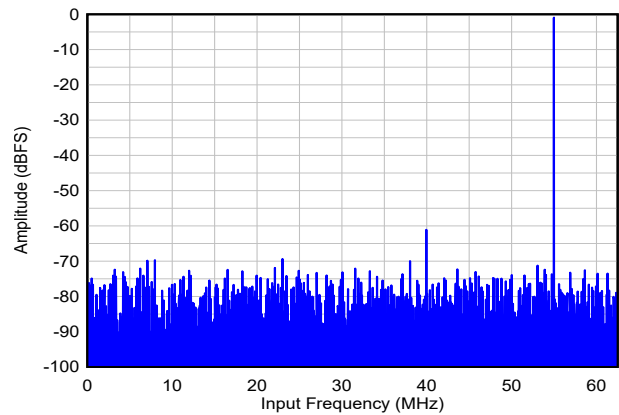
SNR = 49.5dBFS, SFDR = 63dBc, Non-HD23 = 69dBFS

6-37. Single Tone FFT at  $F_{IN} = 5\text{MHz}$ , Single-ended input



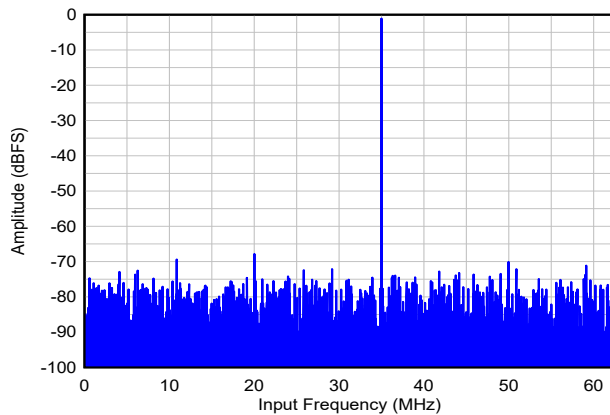
SNR = 49.8dBFS, SFDR = 66dBc, Non-HD23 = 69dBFS

6-38. Single Tone FFT at  $F_{IN} = 40\text{MHz}$



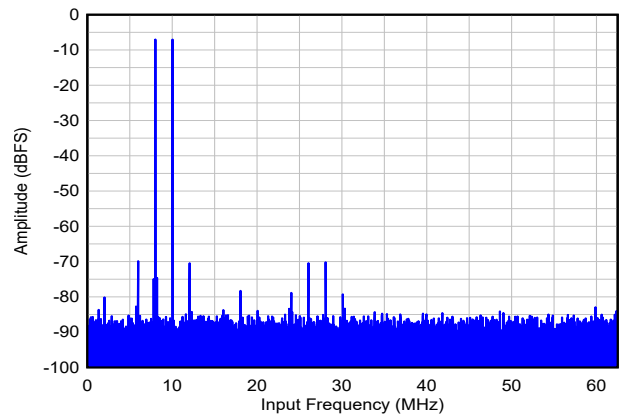
SNR = 49.8dBFS, SFDR = 60dBc, Non-HD23 = 68dBFS

6-39. Single Tone FFT at  $F_{IN} = 70\text{MHz}$



SNR = 49.8dBFS, SFDR = 67dBc, Non-HD23 = 68dBFS

6-40. Single Tone FFT at  $F_{IN} = 90\text{MHz}$

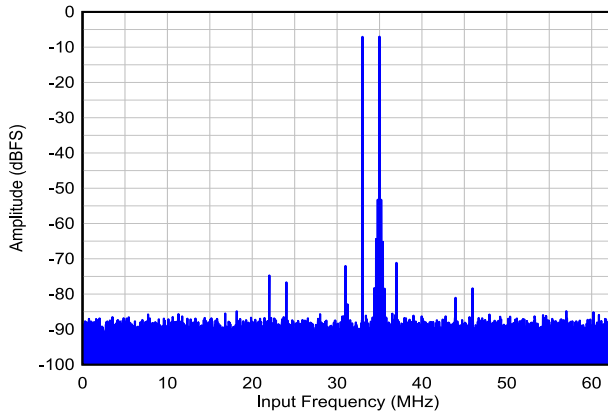


$A_{IN} = -7\text{dBFS}/\text{tone}$ , IMD3 = -87dBc

6-41. Two Tone FFT at  $F_{IN} = 8/10\text{MHz}$

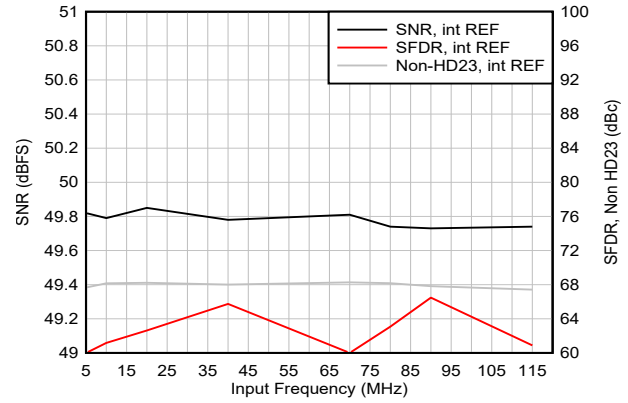
## 6.14 Typical Characteristics - 125MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.

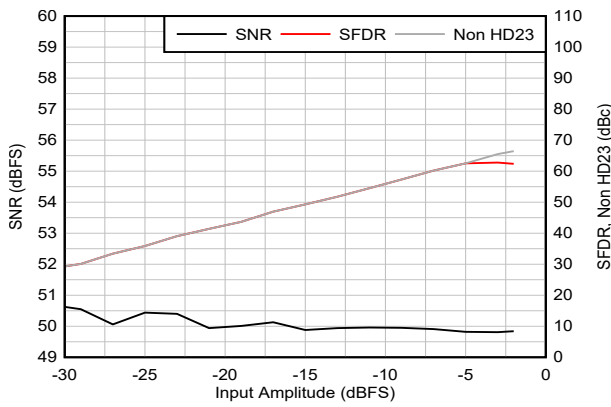


$A_{IN} = -7\text{dBFS}/\text{tone}$ ,  $\text{IMD3} = -87\text{dBc}$

**6-42. Two Tone FFT at  $F_{IN} = 90/92\text{MHz}$**

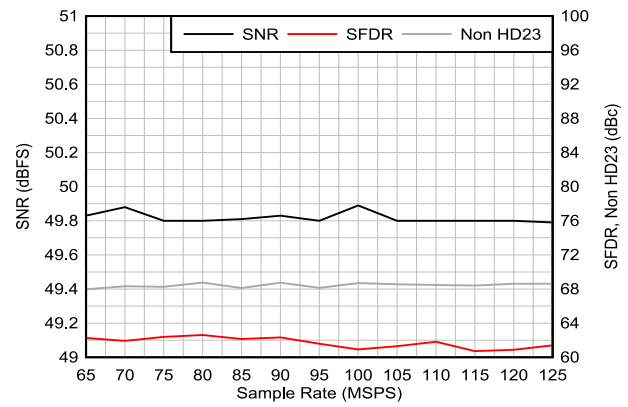


**6-43. AC Performance vs Input Frequency**



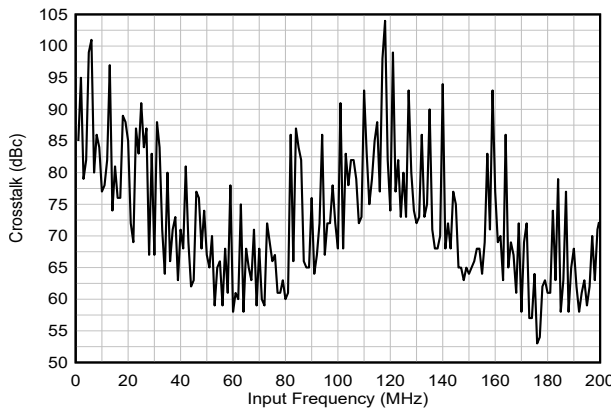
$F_{IN} = 5\text{MHz}$

**6-44. AC Performance vs Input Amplitude**



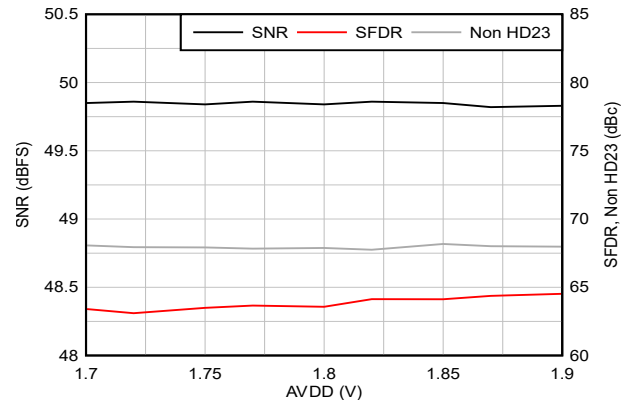
$F_{IN} = 10\text{MHz}$

**6-45. AC Performance vs Sampling Rate**



$A_{IN} = -1\text{dBFS}$  on aggressor channel

**6-46. Crosstalk vs Input Frequency**

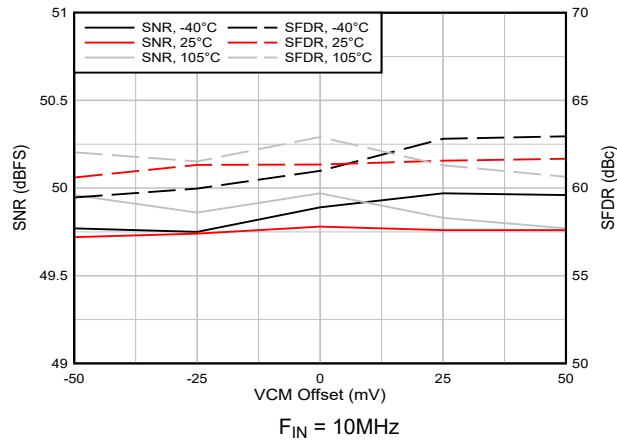


$F_{IN} = 5\text{MHz}$

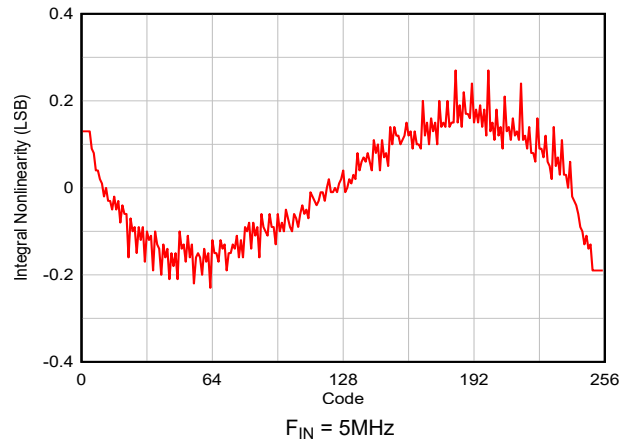
**6-47. AC Performance vs AVDD**

## 6.14 Typical Characteristics - 125MSPS (continued)

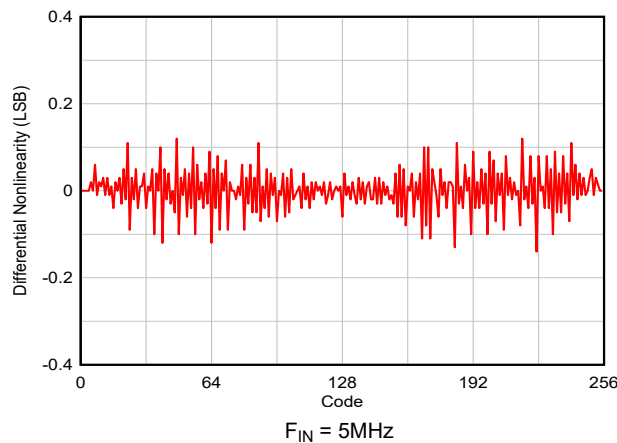
Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



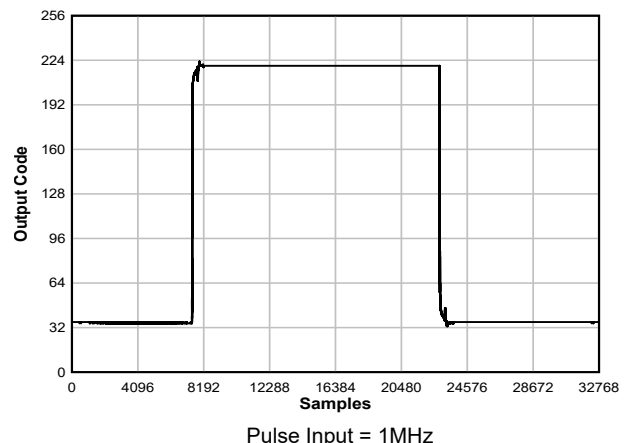
6-48. AC Performance vs VCM vs Temperature



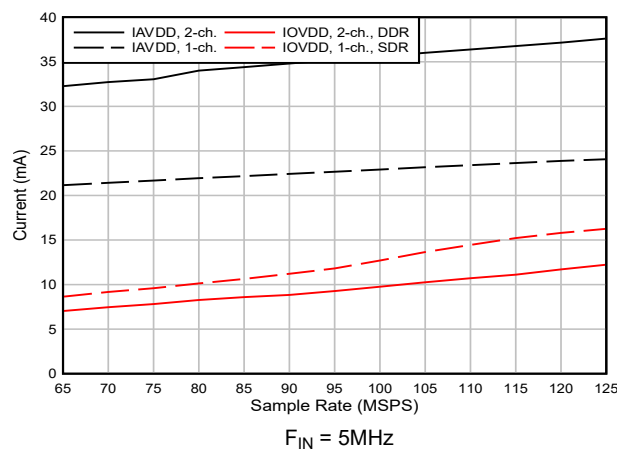
6-49. INL vs ADC Code



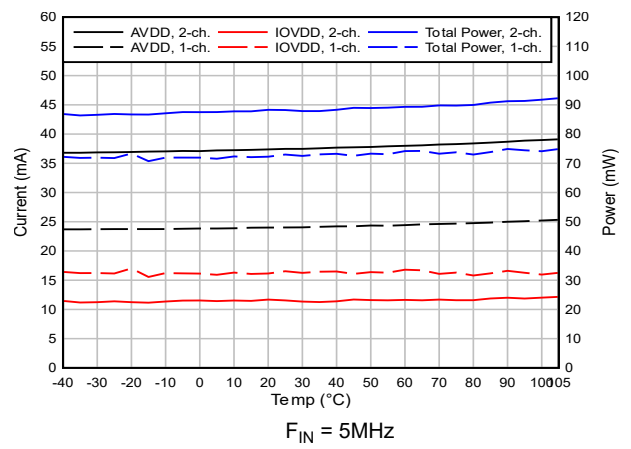
6-50. DNL vs ADC Code



6-51. Pulse Response



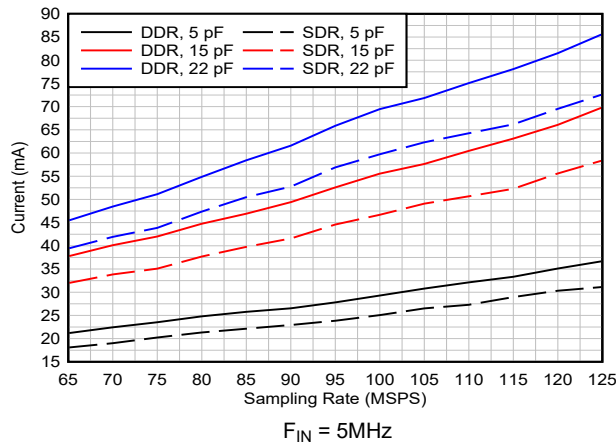
6-52. Current vs Sampling Rate



6-53. Current vs Temperature

### 6.14 Typical Characteristics - 125MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AV_{DD} = IO_{VDD} = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



**6-54.  $I_{IOVDD}$  Current vs Load Capacitance**

## 7 Detailed Description

### 7.1 Overview

The ADC3908Dx および ADC3908Sx is a low noise, ultra-low power 8-bit high-speed single and dual channel ADC family supporting sampling rates up to 125MSPS. With the inherent low latency architecture, the digital output result is available after only one clock cycle. The ADC has buffered analog inputs which eases design by isolating the input from the ADC sampling operation. The ADC3908Dx および ADC3908Sx is equipped with an on-chip internal reference buffer and supports either single ended or differential input signaling.

The CMOS output data interface is configured as parallel DDR for dual channel devices and SDR for single channel devices with the option of 1.8V or 3.3V logic. The device supports 2's Complement or Offset Binary format options. The ADC3908Dx および ADC3908Sx offers  $\overline{\text{DCLK}}$  as an alternate data clock for receivers that can not capture on the DCLK falling edge when using DDR interface. 表 7-1 shows the pin mapping to supply.

表 7-1. Device Pin to Supply Mapping

Power Supply	Device Pins
AVDD	CLK, INxP M, RESET, M0, M1, M2, PDN
IOVDD	D0-D7, DCLK, $\overline{\text{DCLK}}$

### 7.2 Functional Block Diagram

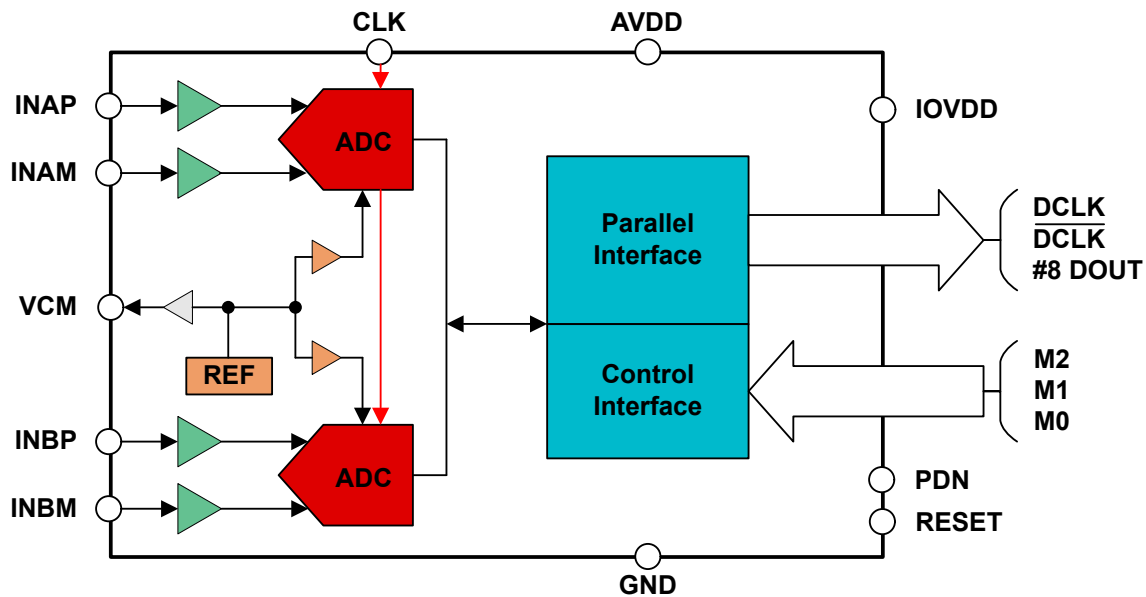
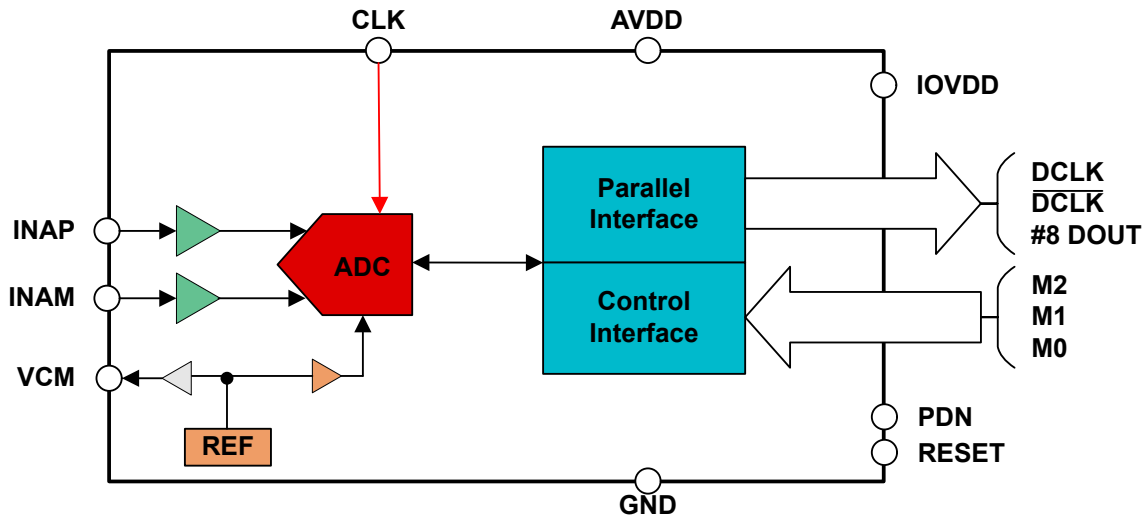


図 7-1. Dual Channel Device





7-2. Single Channel Device

## 7.3 Feature Description

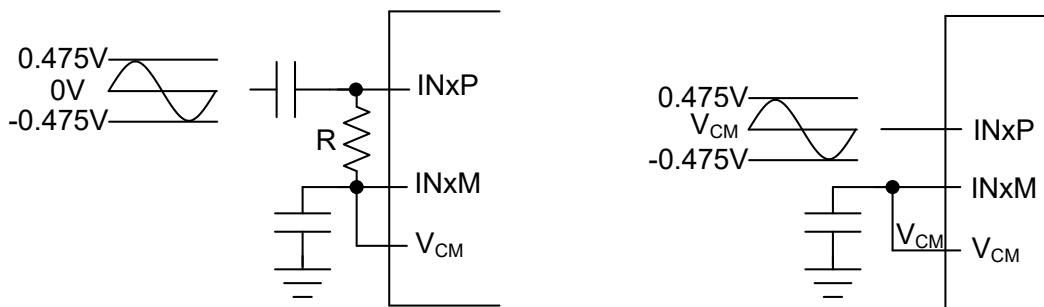
### 7.3.1 Analog Input

The analog inputs of ADC3908Dx および ADC3908Sx supports differential and single-ended configuration, with support for AC coupling and DC coupling. Analog inputs are designed for an input common mode voltage of 1.25V which must be provided externally on each input pin. DC-coupled input signals must have a common mode voltage that meets the device input common mode voltage range.

The ADC3908Dx および ADC3908Sx has buffered analog inputs which eases design by isolating the input from the ADC sampling operation.

#### 7.3.1.1 Single Ended Input

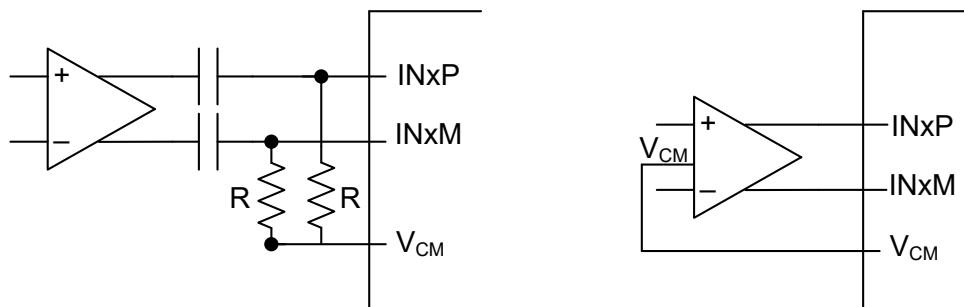
The ADC3908Dx および ADC3908Sx can be configured to operate in single ended mode using just the positive signal input. This operating mode must be enabled via pin control ([Interface configuration table](#)). The single ended signal is connected to the positive input of the ADC and negative input must be biased to  $V_{CM}$  as shown in [図 7-3](#).



**図 7-3. Single ended analog input: AC coupled (left) and DC coupled (right)**

#### 7.3.1.2 Differential Input

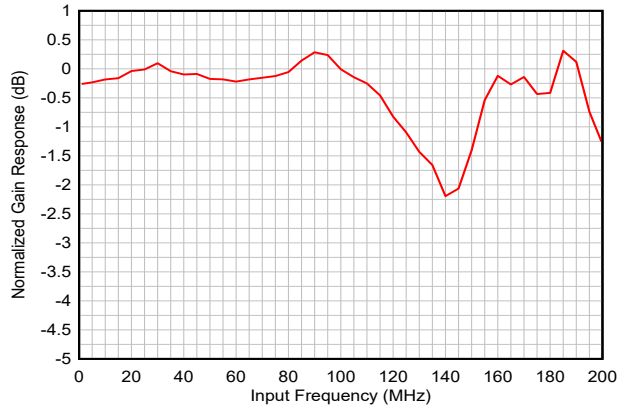
The ADC3908Dx および ADC3908Sx supports differential mode with a swing of  $1.9V_{PP}$  as shown in [図 7-4](#). This operating mode must be enabled via pin control ([Interface configuration table](#)).



**図 7-4. Differential analog input: AC coupled (left) and DC coupled (right)**

#### 7.3.1.3 Analog Input Bandwidth

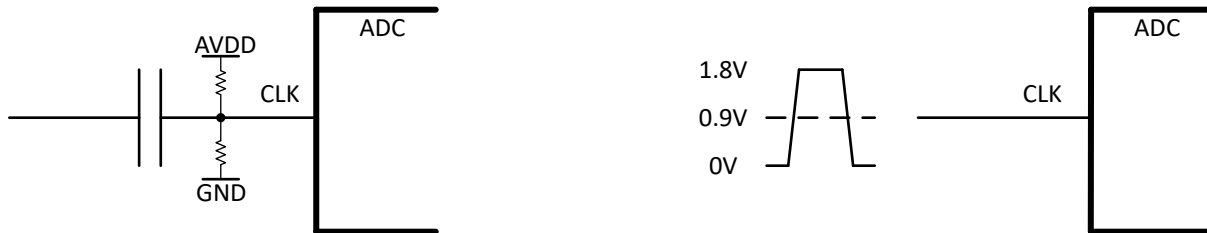
[図 7-5](#) shows the analog full power input bandwidth. The -3dB bandwidth is approximately 150MHz.



**7-5. ADC Analog Input Bandwidth Response**

### 7.3.2 Sampling Clock Input

The ADC3908Dx および ADC3908Sx has a single-ended sampling clock input. To maximize the ADC SNR performance, the external sampling clock should have low jitter with a high slew rate. The ADC3908Dx および ADC3908Sx can be AC or DC coupled externally. When AC coupling, sampling clock needs to have a resistor divider such that the center voltage is around 0.9V and when DC coupling the sampling clock, center voltage needs to be around 0.9V as shown in [Figure 7-6](#).



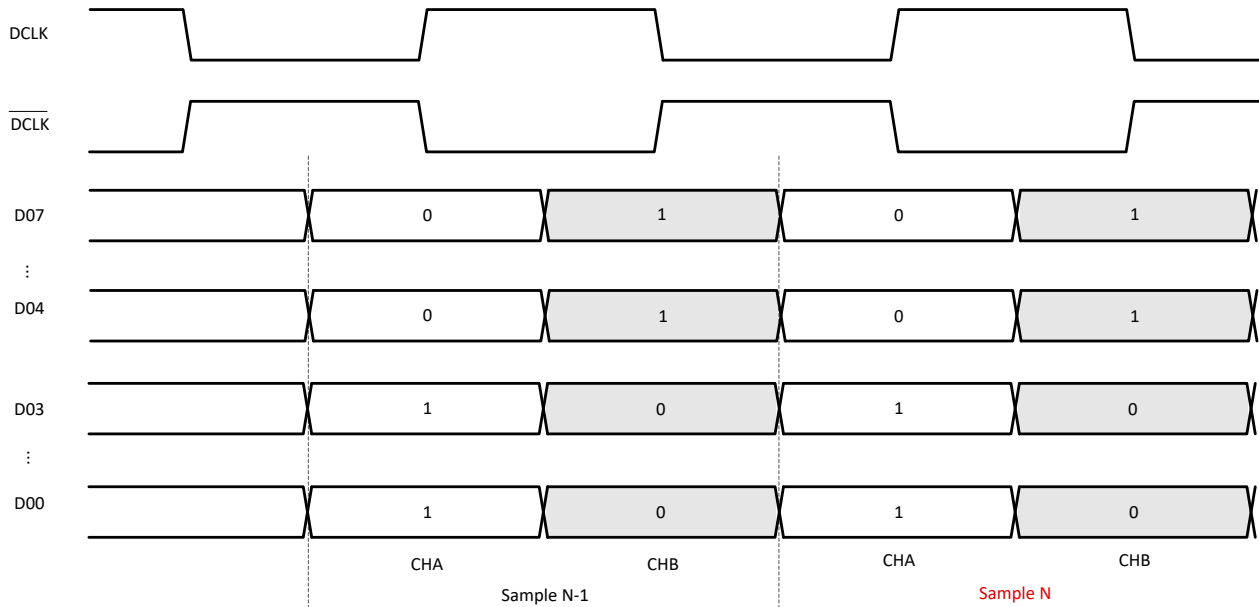
**Figure 7-6. Sampling clock configuration: AC coupled (left) and DC coupled (right)**

### 7.3.3 Digital Interface

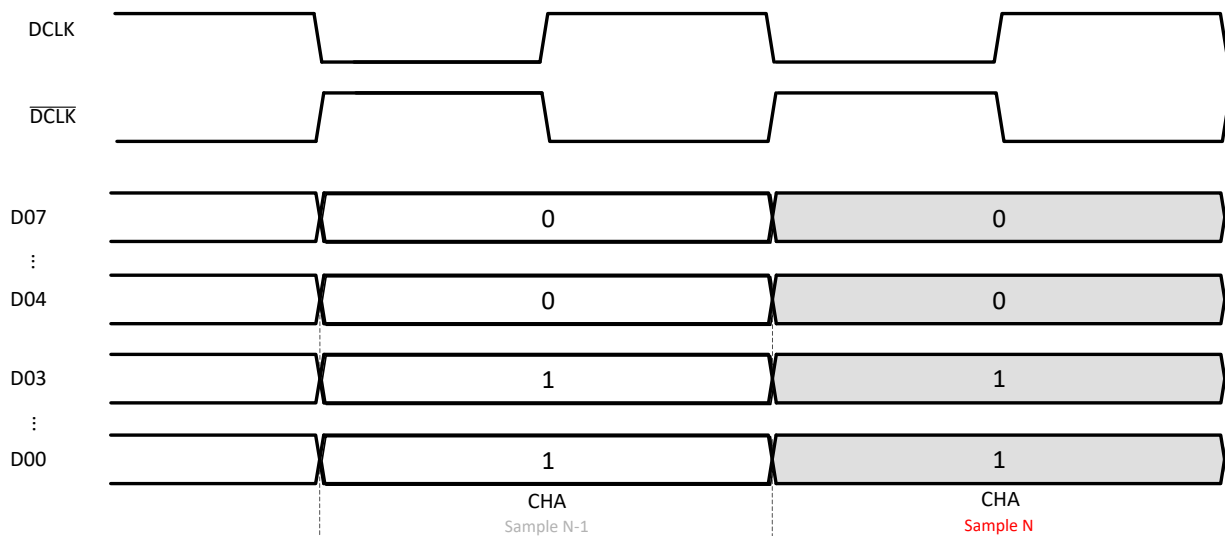
The ADC3908Dx および ADC3908Sx family supports parallel CMOS output modes - DDR (double data rate) and SDR (single data rate) output formats for dual and single channel devices, respectively. The output data can be configured to 2's complement (default) or offset binary via pin control ([Interface configuration table](#)). The device generates an output data clock and inverse data clock. For receivers that cannot use falling edge of data clock, inverse data clock can be used to clock data.

#### 7.3.3.1 Test Pattern

The ADC3908Dx および ADC3908Sx has a static test pattern that can be enabled via pin control (see [Interface Configuration Table](#)). The test pattern splits each channel data into two groups, upper (D7:D4) and lower (D3:D0) bits. Each group has a value of all zeros or a value of all 1s. [図 7-7](#) shows how test pattern is implemented for dual channel. [図 7-8](#) shows how test pattern is implemented for single channel.



**図 7-7. Dual Channel, Test Pattern**



**図 7-8. Single Channel, Test Pattern**

### 7.3.3.2 Interface Configuration using Pin Control

The ADC3908Dx および ADC3908Sx analog input and output interface is configured via pin control only. Pins M0, M1, and M2 can either be pulled high to AVDD, pulled low to GND or intermediate voltages in between. [Interface Configuration Table](#) shows configuration options.

表 7-2. Interface Configuration

Pin Name	Description	GND	0.5V	1V	AVDD
M0	CMOS interface	DDR (dual channel only)			SDR (single channel only)
M1	Output data	ADC data			Test Pattern
M2	Analog input	Differential input		Single-ended input	
	Output data format	2's Complement	Offset binary	2's Complement	Offset binary

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

In normal operating mode, the entire ADC full scale range gets converted to a digital output with 8-bit resolution. The output is available in as little as 1 clock cycle on the digital CMOS outputs.

### 7.4.2 Power Down

The ADC3908Dx および ADC3908Sx can be put into power down mode when PDN pin is pulled high.

## 8 Application Information Disclaimer

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Typical Application

A digitizer is a typical time domain application for the ADC3908D125. The front end circuitry is similar to several other systems such as oscilloscopes, distance meters, laser scanners or other hand held test equipment.

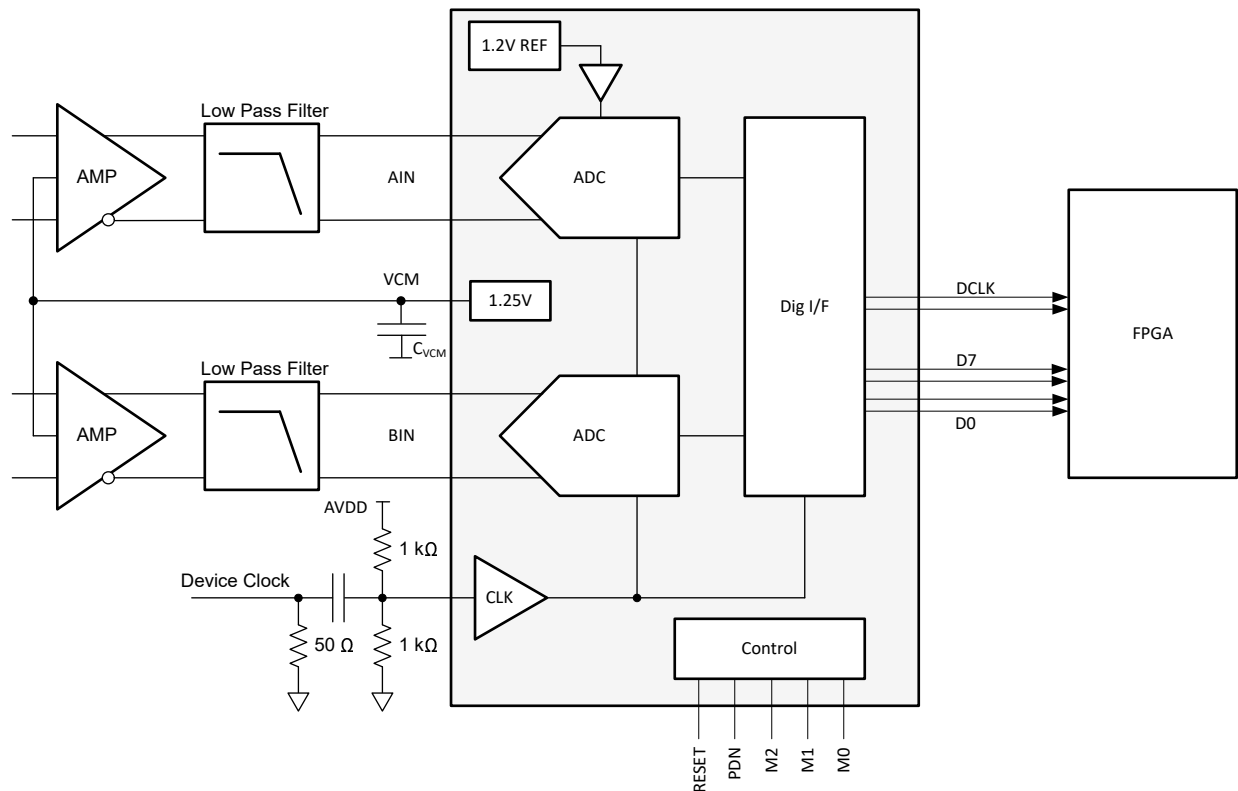


図 8-1. Typical configuration for a time domain digitizer

#### 8.1.1 Design Requirements

Time domain applications cover a wide range of frequencies from low input frequencies at or near DC in the 1st Nyquist zone. If a low input frequency is supported, then the input has to be DC coupled and the ADC driven by a fully differential amplifier (FDA).

The ADC performance is highly dependent on the quality of the external clock source. A higher ADC sampling rate is desirable to relax the external anti-aliasing filter. For optimum performance, the analog inputs must be driven differentially.

表 8-1. Design key care abouts

FEATURE	DESCRIPTION
Signal Bandwidth	DC to 30MHz
Input Driver	Single ended to differential signal conversion and DC coupling



**表 8-1. Design key care abouts (続き)**

FEATURE	DESCRIPTION
Clock Source	External clock with low jitter

When designing the amplifier/filter driving circuit, the ADC input full-scale voltage needs to be taken into consideration. For example, the ADC3908D125 input full-scale is 1.9 V<sub>PP</sub>. When factoring in approximately 1dB for insertion loss of the filter, then the amplifier needs to deliver close to 2.1 V<sub>PP</sub>. The amplifier distortion performance degrades with a larger output swing and considering the ADC common mode input voltage the amplifier may not be able to deliver the full swing. The device ADC3908D125 provides an output common mode voltage of 1.25V and the THS4541 for example can only swing within 250mV of its negative supply. A unipolar 3.3V amplifier power supply limits the maximum voltage swing to approximately 2.8V<sub>PP</sub>. Hence, if a larger output swing is required (factoring in filter insertion loss) then a negative supply for the amplifier is needed to eliminate that limitation. Additionally, input voltage protection diodes may be needed to protect the ADC from over-voltage events.

**表 8-2. Output voltage swing of THS4541 vs power supply**

DEVICE	MIN OUTPUT VOLTAGE	MAX SWING WITH 3.3V/ 0V SUPPLY
THS4541	V <sub>S-</sub> + 250mV	2.8V <sub>PP</sub>

## 8.1.2 Detailed Design Procedure

### 8.1.2.1 Input Signal Path

The THS4541 provides a good low power option to drive the ADC inputs. 表 8-3 provides an overview of the THS4541 with power consumption and usable frequency.

**表 8-3. Fully Differential Amplifier Options**

DEVICE	CURRENT (IQ) PER CHANNEL	USABLE FREQUENCY RANGE
THS4541	10mA	< 70MHz

The low pass filter design (topology, filter order) is driven by the application. However, when designing the low pass filter, the optimum load impedance for the amplifier must also be taken into consideration.

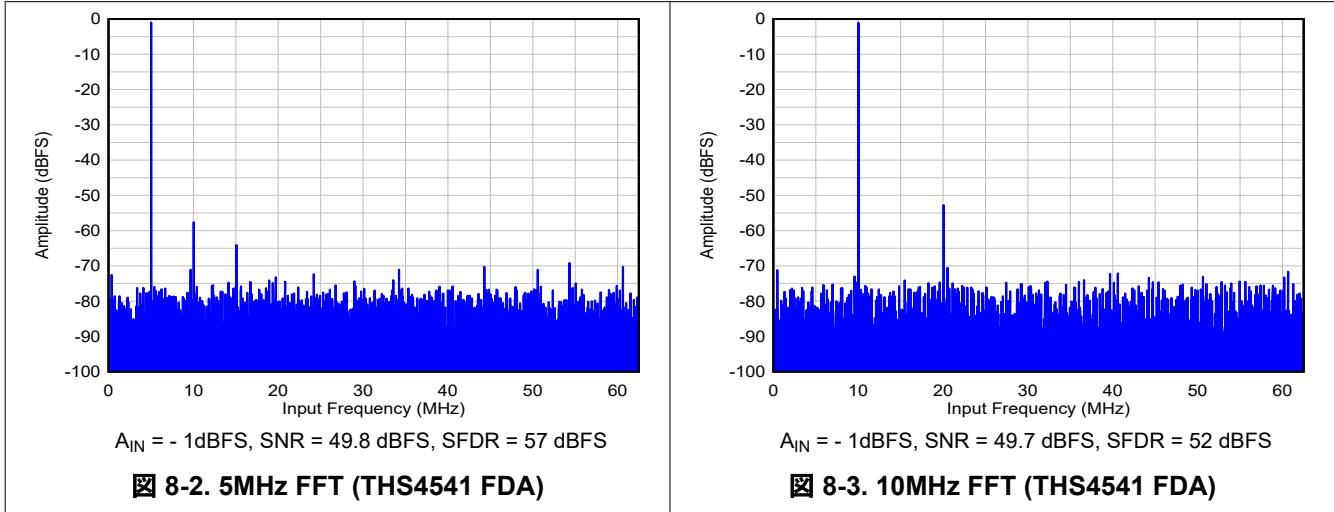
### 8.1.2.2 Sampling Clock

Applications operating with low input frequencies (such as DC to 20MHz) typically are less sensitive to performance degradation due to clock jitter. The internal ADC aperture jitter improves with faster rise and fall times (that is, square wave vs sine wave).

Termination of the clock input needs to be considered for long clock traces.

### 8.1.3 Application Curves

The following FFT plots show the performance of THS4541 driving the ADC3908D125 operated at 125MSPS with a full-scale input at -1dBFS.



## 8.2 Initialization Set Up

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin.

1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied the internal band gap reference powers up and settle out in approximately 2ms.
2. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses and the internal power up calibration is initiated. The calibration takes approximately 2,000 clock cycles.
3. Begin programming using the device control pins.

### 8.3 Power Supply Recommendations

The ADC requires two different power-supplies. The AVDD rail provides power for the internal analog and digital circuits and the ADC itself while the IOVDD rail powers the digital interface. Power sequencing is not required.

The AVDD power supply must be low noise to achieve data sheet performance. In applications operating near DC, the  $1/f$  noise contribution of the power supply also needs to be considered. The ADC is designed for very good PSRR which aids with the power supply filter design.

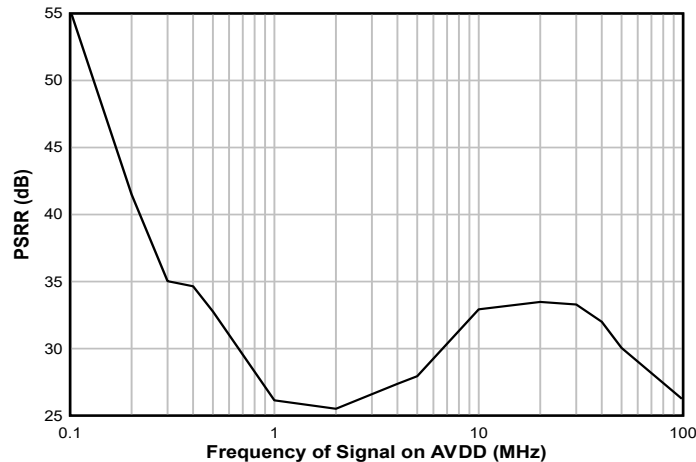


図 8-4. Power supply rejection ratio (PSRR) vs frequency

There are two recommended power-supply architectures:

1. Step down using high-efficiency switching converters, followed by a second stage of regulation using a low noise LDO to provide switching noise reduction and improved voltage accuracy.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken to make sure switching noise is minimized to prevent degraded ADC performance.

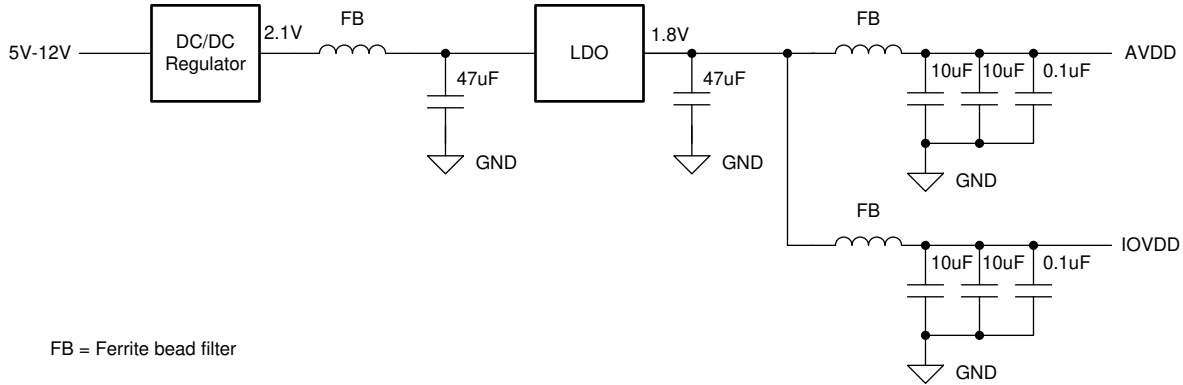
TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS62821, and similar devices.

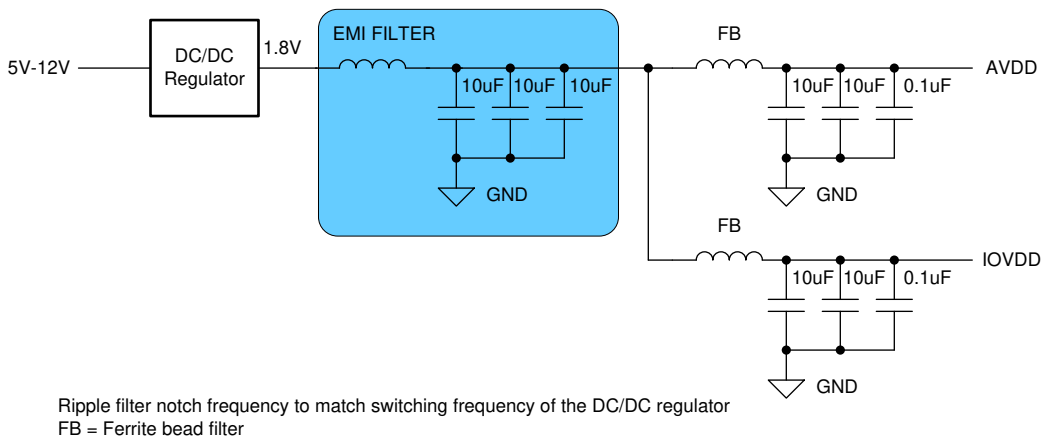
Recommended low dropout (LDO) linear regulators include the TPS7A4701, TPS7A90, LP5901, and similar devices.

For the switch regulator only approach, the ripple filter must be designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Note the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. 図 8-5 and 図 8-6 illustrate the two approaches.

AVDD and IOVDD supply voltages should not be shared to prevent digital switching noise from coupling into the analog signal chain.



**図 8-5. Example: LDO Linear Regulator Approach**



**図 8-6. Example: Switcher-Only Approach**

## 8.4 Layout

### 8.4.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
  - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
2. Digital output interface
  - Traces should be as short as possible to reduce capacitive load seen by the CMOS outputs.
  - Series resistance should be used to reduce instantaneous current demand and improve signal integrity.
3. Power and ground connections
  - Provide low resistance connection paths to all power and ground pins.
  - Use power and ground planes instead of traces.
  - Avoid narrow, isolated paths which increase the connection resistance.
  - Use a signal/ground/power circuit board stackup to maximize coupling between the ground and power plane.

### 8.4.2 Layout Example

The following screen shot shows the top layer of the [ADC3910D125EVM](#).

- Signal inputs are routed as different signal and along with clock input on the top layer avoiding vias.
- Serial CMOS output interface lanes with isolation resistor.
- Bypass caps are close to the VREF pin on the top layer avoiding vias.

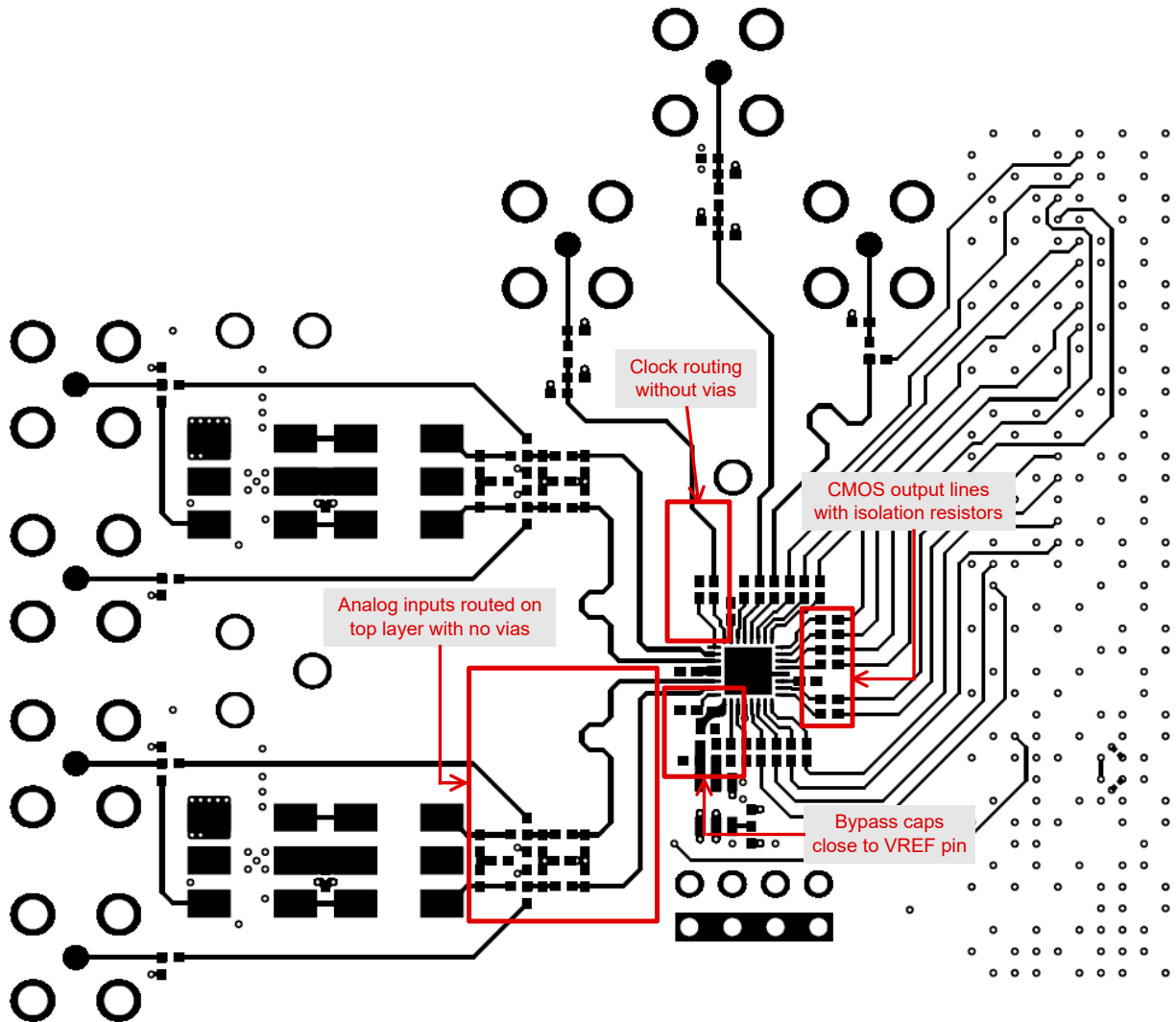


図 8-7. Layout Example: top layer of ADC3910D125EVM

## 9 Device and Documentation Support

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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### 9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2024	*	Initial Release

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC3908D025IRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398D1	<a href="#">Samples</a>
ADC3908D025IRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398D1	<a href="#">Samples</a>
ADC3908D065IRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398D2	<a href="#">Samples</a>
ADC3908D065IRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398D2	<a href="#">Samples</a>
ADC3908D125IRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398D3	<a href="#">Samples</a>
ADC3908D125IRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398D3	<a href="#">Samples</a>
ADC3908S025IRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398S1	<a href="#">Samples</a>
ADC3908S025IRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398S1	<a href="#">Samples</a>
ADC3908S065IRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398S2	<a href="#">Samples</a>
ADC3908S065IRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398S2	<a href="#">Samples</a>
ADC3908S125IRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398S3	<a href="#">Samples</a>
ADC3908S125IRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ398S3	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC3908D025IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908D025IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908D065IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908D065IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908D125IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908D125IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908S025IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908S025IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908S065IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908S065IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908S125IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3908S125IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC3908D025IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3908D025IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3908D065IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3908D065IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3908D125IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3908D125IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3908S025IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3908S025IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3908S065IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3908S065IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3908S125IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3908S125IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

**RSM 32**

**VQFN - 1 mm max height**

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A

# RSM0032B



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



### NOTES:

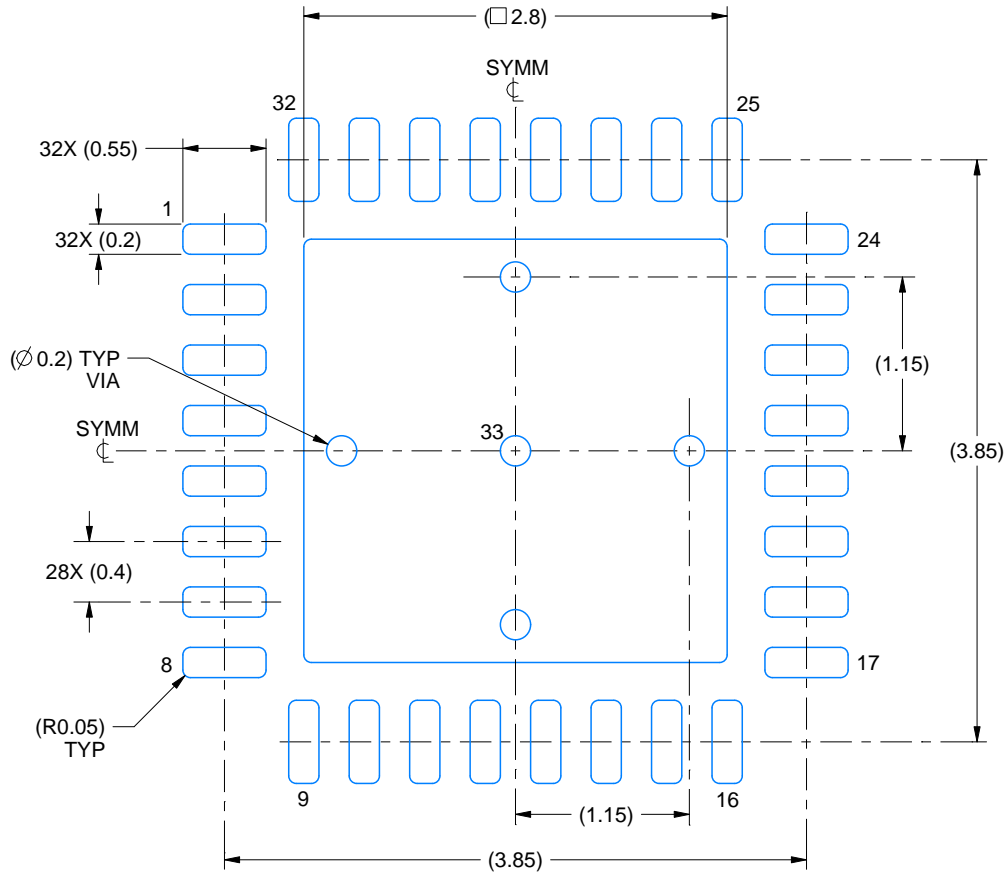
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

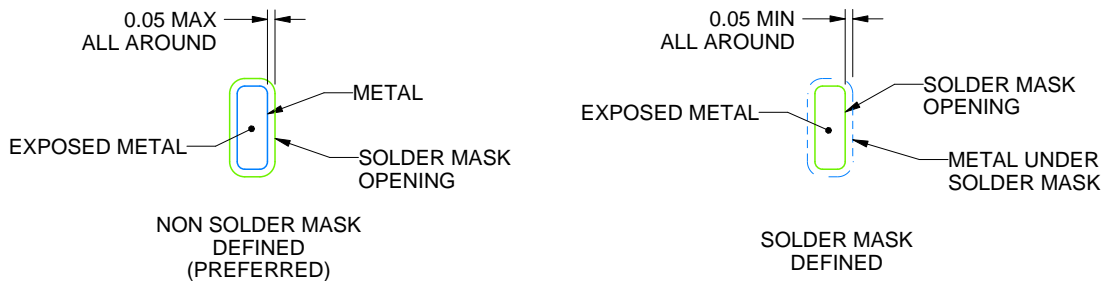
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

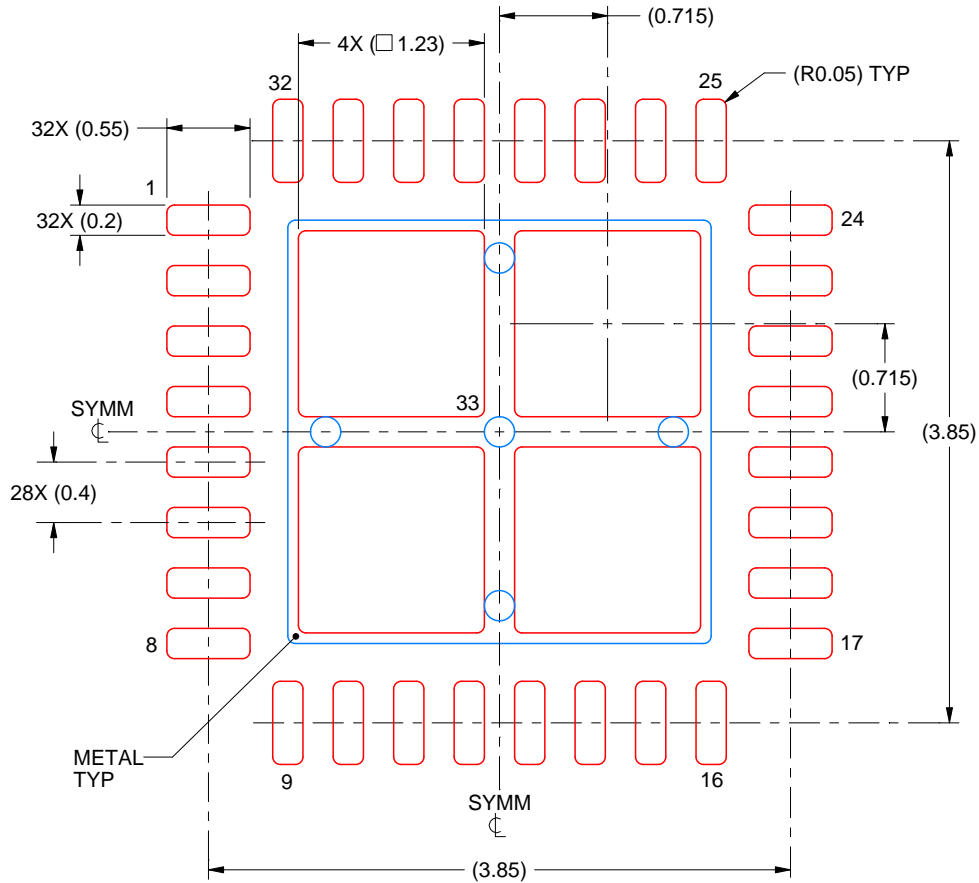
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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